ADVANTAGES OF ENHANCED RECEIVER FAILSAFE FEATURES

IN RS-485/RS-422 SERIAL TRANSCEIVERS

1.0   INTRODUCTION

RS-485/RS-422 receiver failsafe keeps the data bus in a known state when there are no active drivers on the bus. The Exar RS-485/RS-422 transceivers offer two different types of receiver failsafe: standard and enhanced. This application note will discuss how the enhanced receiver failsafe feature can help customers with failsafe problems while terminated.

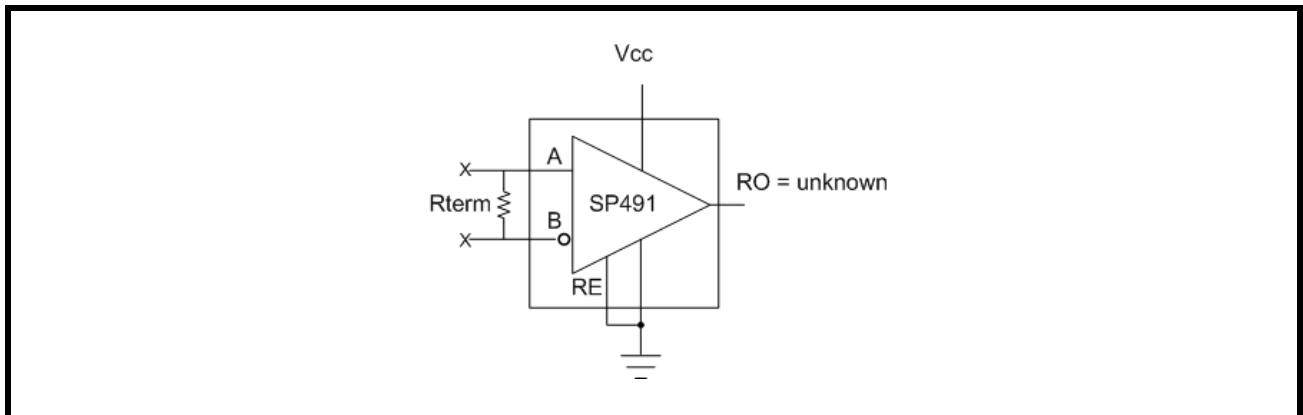## 2.0   STANDARD RECEIVER FAILSAFE

RS-485/RS-422 devices such as Exar's SP491 offer a standard receiver failsafe. The standard receiver failsafe feature for this device will provide a logic high at the receiver output when the receiver inputs are open circuit or floating. For example, when the data cable is disconnected, the receiver output will keep the line in a known high state. Standard receiver failsafe has an internal weak biasing network that will force the open inputs to >200mV thus resulting in a logic high output. Figure 1 shows the receiver configuration for failsafe logic high output.

FIGURE 1. OPEN INPUT RECEIVER FAILSAFE
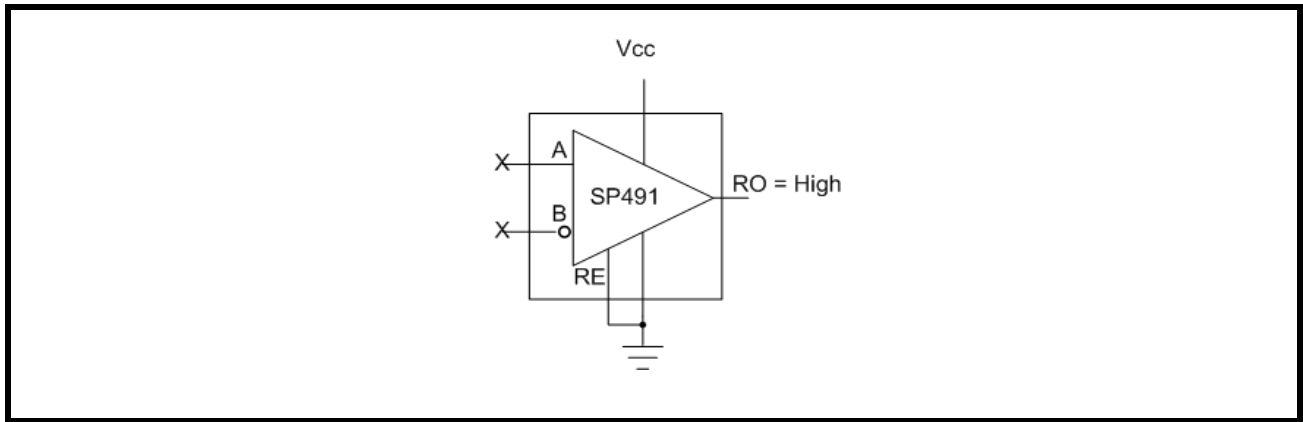
  Some applications operating at high speeds incorporate a termination resistor at the ends of the bus to prevent signal reflections. The termination resistor value should match the characteristic impedance of the data cable. In a majority of applications, the termination resistor is typically 120 ohms. When a termination resistor is connected between receiver inputs "A" and "B" the standard receiver failsafe feature will not operate properly (see Figure 2).

FIGURE 2. TERMINATED RECEIVER INPUT

This has been a common problem with many standard failsafe receiver devices. The termination resistor causes a potential difference of 0V because the internal biasing circuit is not strong enough to overcome the termination load. The receiver sensitivity, as per RS-485 specifications, is +/-200mV (see Figure 3).

FIGURE 3. RECEIVER SENSITIVITY
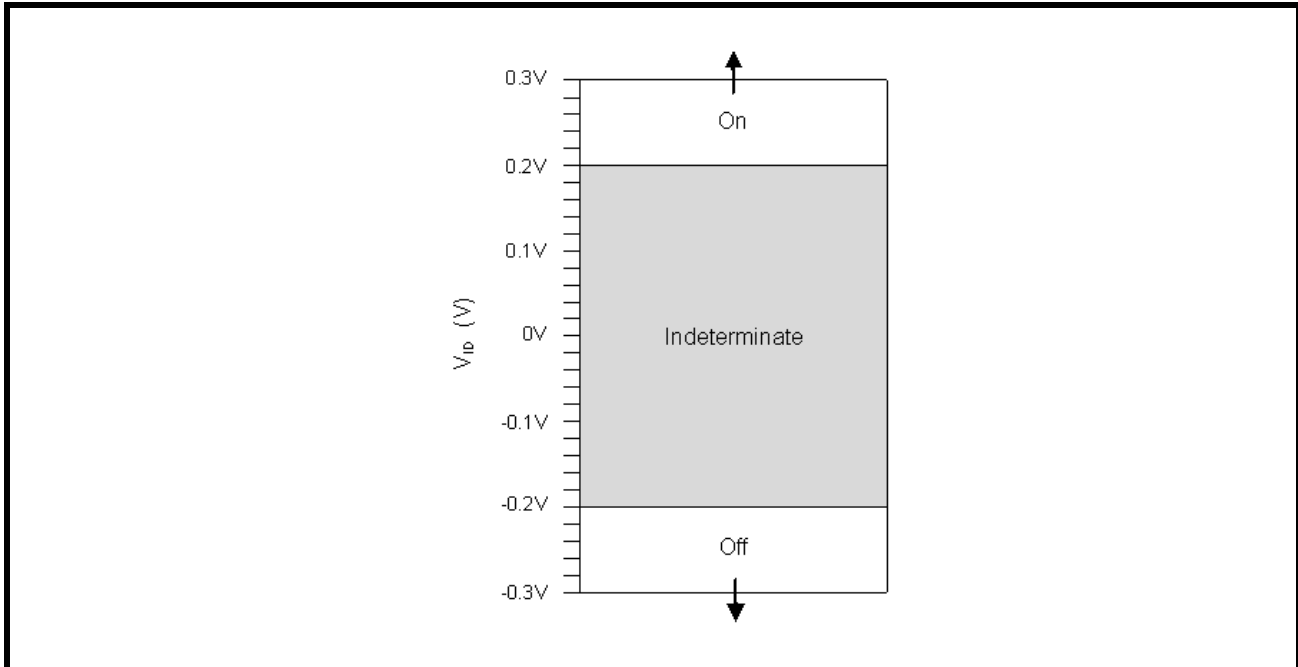
A potential difference of 0V is within the indeterminate range of sensitivity. This may result in an unknown state. Under this condition, many may find the receiver output state on some devices to be good while others bad. In fact, some devices with enough noise present may produce an oscillating clock pulse at output. One solution to this terminated failsafe problem is to include an external biasing network that will provide a >+200mV potential difference across the termination resistor at receiver input. This external biasing network is a simple pull-up resistor from "A" input to Vcc and a pull-down resistor from "B" input to GND (See figure 4). The values of the pull-up/down resistors are selected to provide at least 200mV across "A" and "B" inputs.

FIGURE 4. TERMINATED RECEIVER INPUT WITH BIASING NETWORK
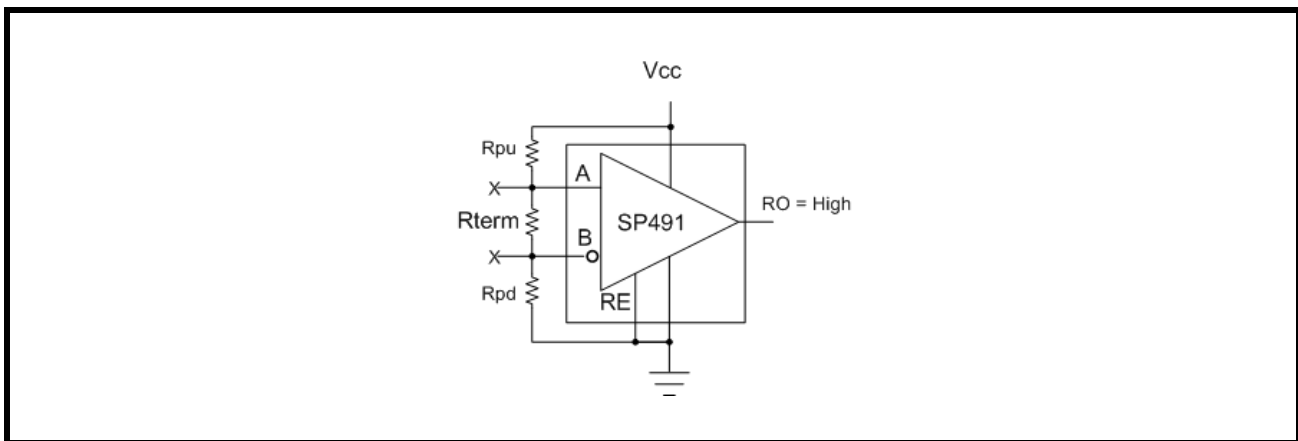
3.0   ENHANCED RECEIVER FAILSAFE

Exar has developed several new families of RS-485/RS-422 transceivers, SP1486, SP3080-3088, SP3495-3497, XR3170-3178 and XR5486-5488 with an enhanced receiver failsafe feature. This enhanced receiver failsafe provides failsafe for three different conditions: open input, shorted input and un-driven terminated lines.

This feature is very useful for terminated applications in that no external biasing network is required for proper failsafe operation. Many of Exar's original RS-485 transceivers with standard failsafe may be upgraded to a pin compatible design using SP1486, SP3080-3088, SP3495-3497, XR3170-3178 and XR5486-5488 products. The SP3086E is pin compatible to SP491. The SP3086E receiver offers an enhanced failsafe feature and has a negative input threshold (see figure 5).

FIGURE 5. ENHANCED RECEIVER FAILSAFE SENSITIVITY
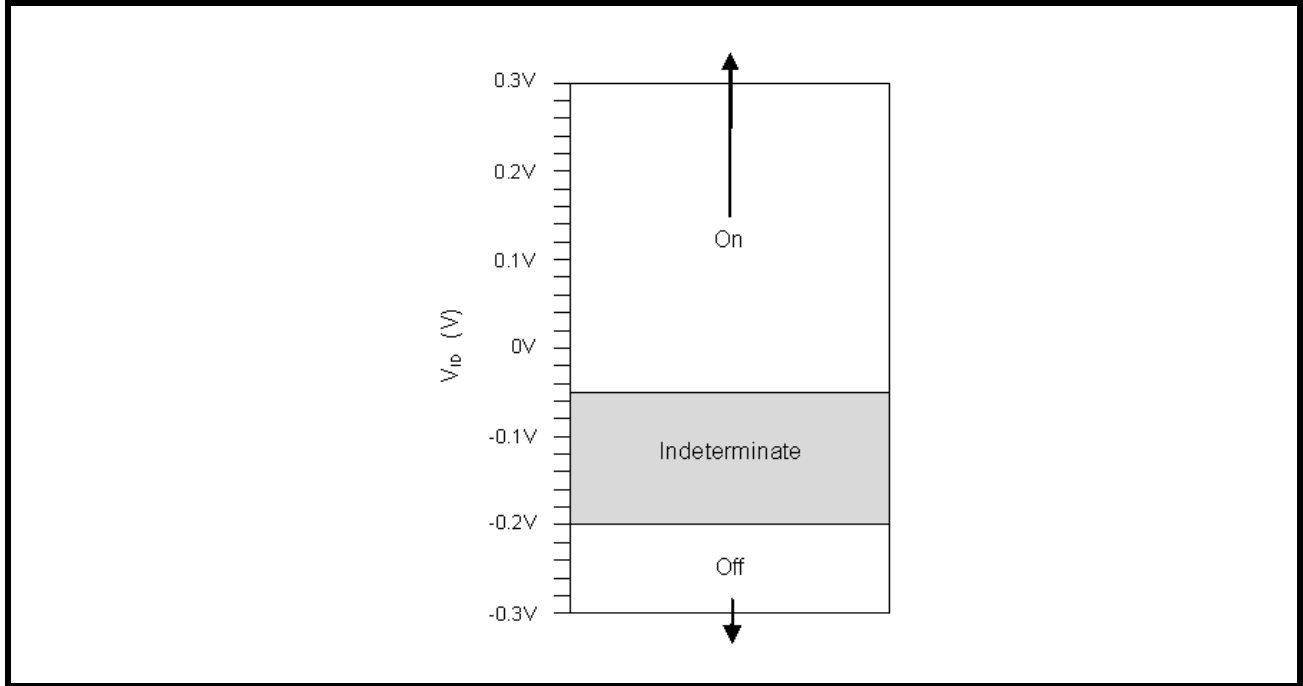
When the connected driver is disabled while the receiver input is terminated the potential difference at receiver input will be 0V. Since the enhanced receiver failsafe device has a negative threshold the output will still be logic high when the differential voltage is 0V. Figures 6, 7 and 8 show the three different conditions for enhanced receiver failsafe logic high output.
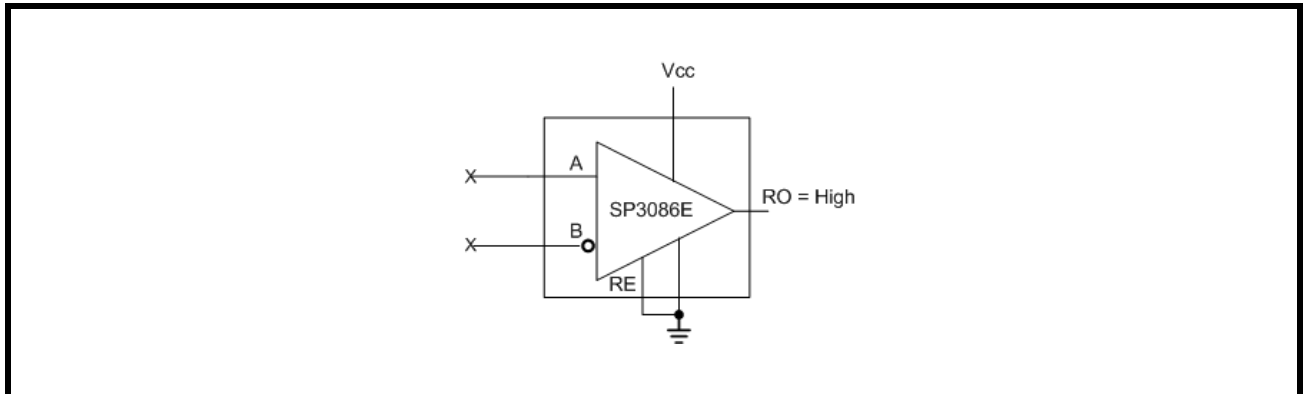
FIGURE 6. OPEN INPUT
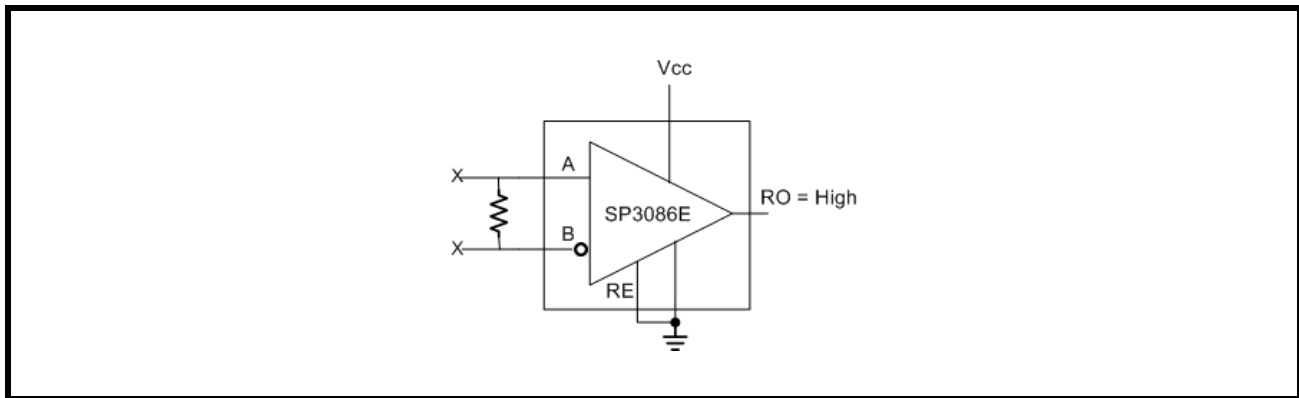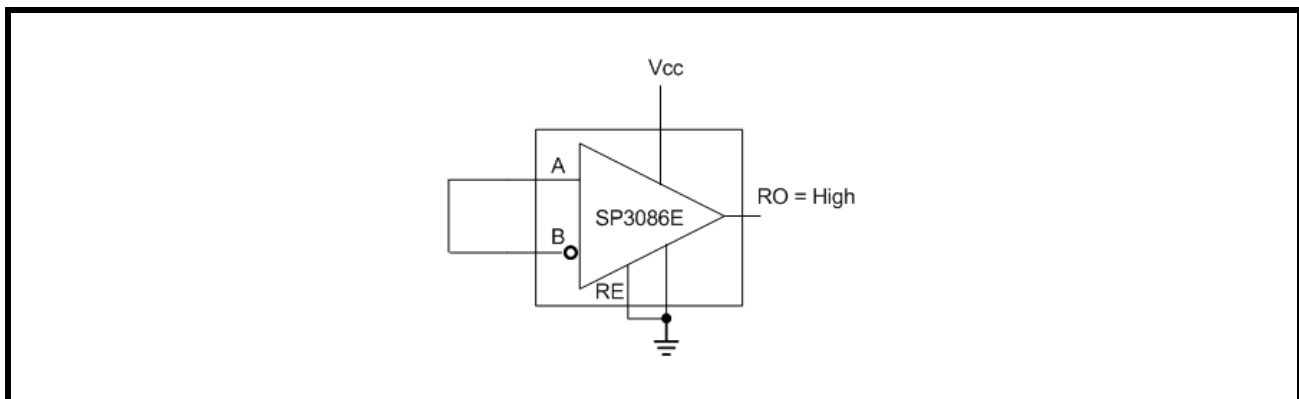
FIGURE 7. UN-DRIVEN TERMINATED INPUT

FIGURE 8. SHORTED INPUT

4.0 EXAR TRANSCEIVERS WITH ENHANCED RECEIVER FAILSAFE

TABLE 1: ENHANCED RECEIVER FAILSAFE TRANSCEIVERS

PART NUMBER	VCC	MAXIMUM DATA RATE	PACKAGE
SP1486E	5.0V	20Mbps	8-pin NSOIC
SP4082E	5.0V	115kbps	8-pin NSOIC
SP3495E	3.3V	32Mbps	8-pin NSOIC
SP3496E	3.3V	32Mbps	8-pin NSOIC
SP3497E	3.3V	32Mbps	14-pin NSOIC
SP3070E	3.3V	250kbps	14-pin NSOIC
SP3071E	3.3V	250kbps	8-pin NSOIC
SP3072E	3.3V	250kbps	8-pin NSOIC
SP3073E	3.3V	500kbps	14-pin NSOIC
SP3074E	3.3V	500kbps	8-pin NSOIC
SP3075E	3.3V	500kbps	8-pin NSOIC
SP3076E	3.3V	16Mbps	14-pin NSOIC
SP3077E	3.3V	16Mbps	8-pin NSOIC
SP3078E	3.3V	16Mbps	8-pin NSOIC
SP3080E	5.0V	115kbps	14-pin NSOIC
SP3081E	5.0V	115kbps	8-pin NSOIC
SP3082E	5.0V	115kbps	8-pin NSOIC
SP3083E	5.0V	500kbps	14-pin NSOIC
SP3084E	5.0V	500kbps	8-pin NSOIC
SP3085E	5.0V	500kbps	8-pin NSOIC
SP3086E	5.0V	20Mbps	14-pin NSOIC
SP3087E	5.0V	20Mbps	8-pin NSOIC
SP3088E	5.0V	20Mbps	8-pin NSOIC
XR3170E	3.3V	250kbps	14-pin NSOIC
XR3171E	3.3V	250kbps	8-pin NSOIC
XR3172E	3.3V	250kbps	8-pin NSOIC
XR3173E	3.3V	500kbps	14-pin NSOIC
XR3174E	3.3V	500kbps	8-pin NSOIC
XR3175E	3.3V	500kbps	8-pin NSOIC
XR3176E	3.3V	20Mbps	14-pin NSOIC
XR3177E	3.3V	20Mbps	8-pin NSOIC
XR3178E	3.3V	20Mbps	8-pin NSOIC
XR5486E	5.0V	52Mbps	14-pin NSOIC
XR5487E	5.0V	52Mbps	8-pin NSOIC
XR5488E	5.0V	52Mbps	8-pin NSOIC

5.0   TECHNICAL SUPPORT

Technical questions about this application note should be e-mailed to uarttechsupport@exar.com.

NOTICE