



# AC701 PCIe Design Creation

April 2015

XTP227

# Revision History

Date	Version	Description
04/30/14	11.0	Regenerated for 2015.1.
11/24/14	10.0	Regenerated for 2014.4.
10/08/14	9.0	Regenerated for 2014.3.
06/09/14	8.0	Regenerated for 2014.2.
04/16/14	7.0	Regenerated for 2014.1. AR54939 fixed.
12/18/13	6.0	Regenerated for 2013.4.
11/21/13	5.1	Minor updates.
10/23/13	5.0	Regenerated for 2013.3. Added AR54939.
06/19/13	4.0	Regenerated for 2013.2. AR55494 and AR55711 fixed.
04/03/13	3.0	Regenerated for 2013.1. AR54232 fixed. Added AR55494 and AR55711.
02/04/13	2.1	As per AR54044, added 2012.4 device pack. Added AR53561, AR54232, and AR54223.
12/18/12	2.0	Regenerated for 2012.4. AR52487 fixed. AR52660 fixed.
10/23/12	1.0	Initial Version. Added AR52487. Added AR44635. Added AR52660.

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# Overview

- Artix-7 PCIe x4 Gen 2 Capability
- Xilinx AC701 Board
- Software Requirements
- AC701 Setup
- Generate x4 Gen 2 PCIe Core
  - Modify PCIe Core
  - Compile Example Design
  - Generate PCIe MCS File
  - Program SPI Flash with PCIe Design
- Running the PCIe x4 Gen 2 Design
- References

# Artix-7 PCIe x4 Gen 2 Capability

## ► AC701 Supports PCIe Gen 1 and Gen 2 Capability

- x4, x2, or x1 Gen 1 and Gen 2 lane width

## ► LogiCORE PIO Example Design

- AC701 PCIe Design Files (2015.1 C) ZIP file
- Available through <http://www.xilinx.com/ac701>

## ► 7 Series Integrated Block for PCI Express

- See [PG054](#) for details

# **Artix-7 PCIe x4 Gen 2 Capability**

## **➤ Integrated Block for PCI Express**

- PCI Express Base 2.0 Specification

## **➤ Configurable for Endpoint or Root Port Applications**

- AC701 configured for Endpoint Applications

## **➤ GTX Transceivers implement a fully compliant PHY**

## **➤ Large range of maximum payload size**

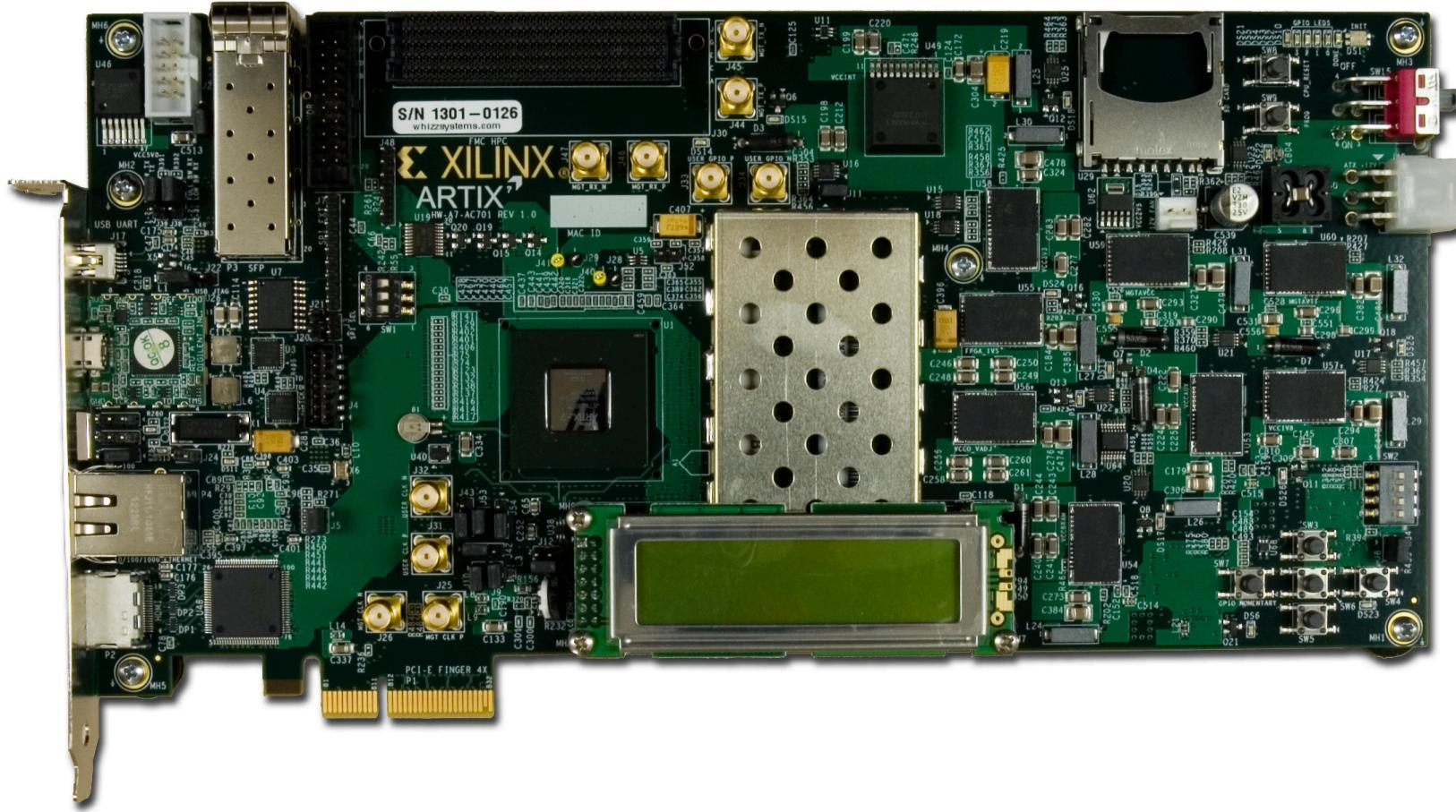
- 128 / 256 / 512 / 1024 bytes

## **➤ Configurable BAR spaces**

- Up to 6 x 32 bit, 3 x 64 bit, or a combination
- Memory or IO
- BAR and ID filtering

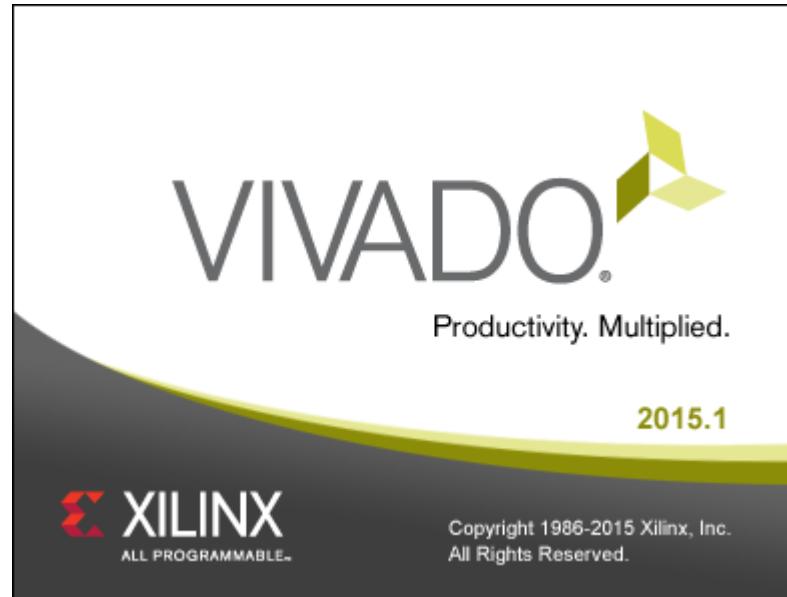
## **➤ Management and Statistics Interface**

# Xilinx AC701 Board



# Vivado Software Requirements

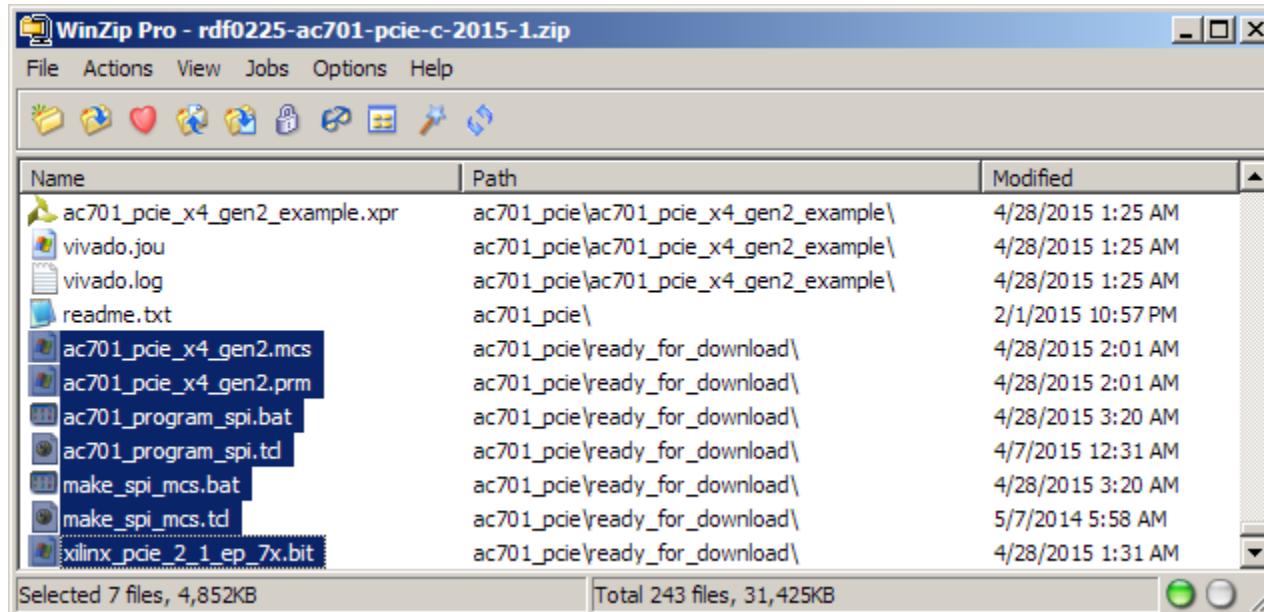
- Xilinx Vivado Design Suite 2015.1, Design Edition



# Setup for the AC701 PCIe Designs

► Open the AC701 PCIe Design Files (2015.1 C) zip file, and extract these files to your C:\ drive:

- ac701\_pcnie\ready\_for\_download\\*
- Available through <http://www.xilinx.com/ac701>



# PciTree Software Requirement

## ► PciTree Bus Viewer

- Free [download](#)
- HLP.SYS must be copied to  
C:\WINDOWS\system32\drivers  
directory



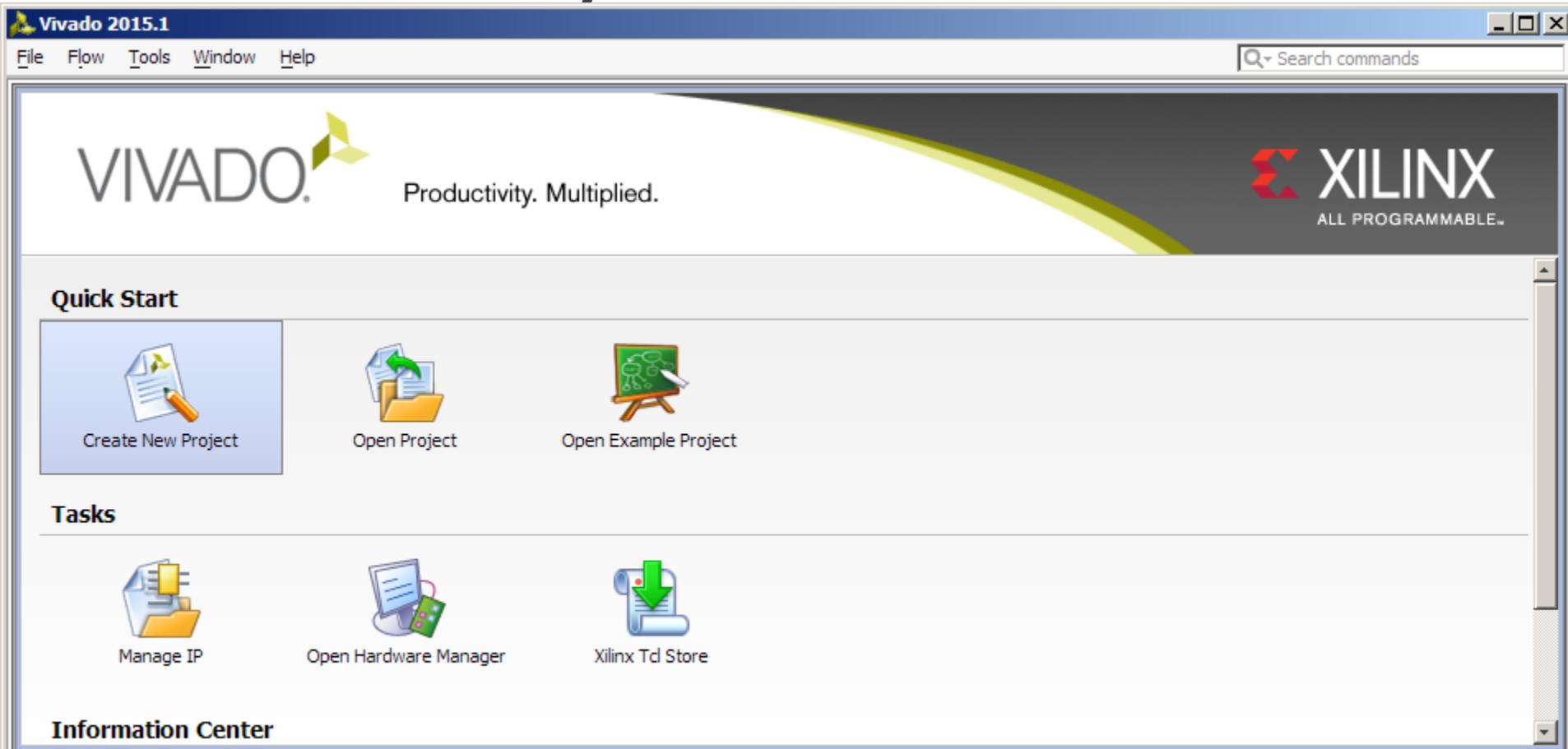
# **Generate x4 Gen 2 PCIe Core**

# Generate x4 Gen 2 PCIe Core

## ► Open Vivado

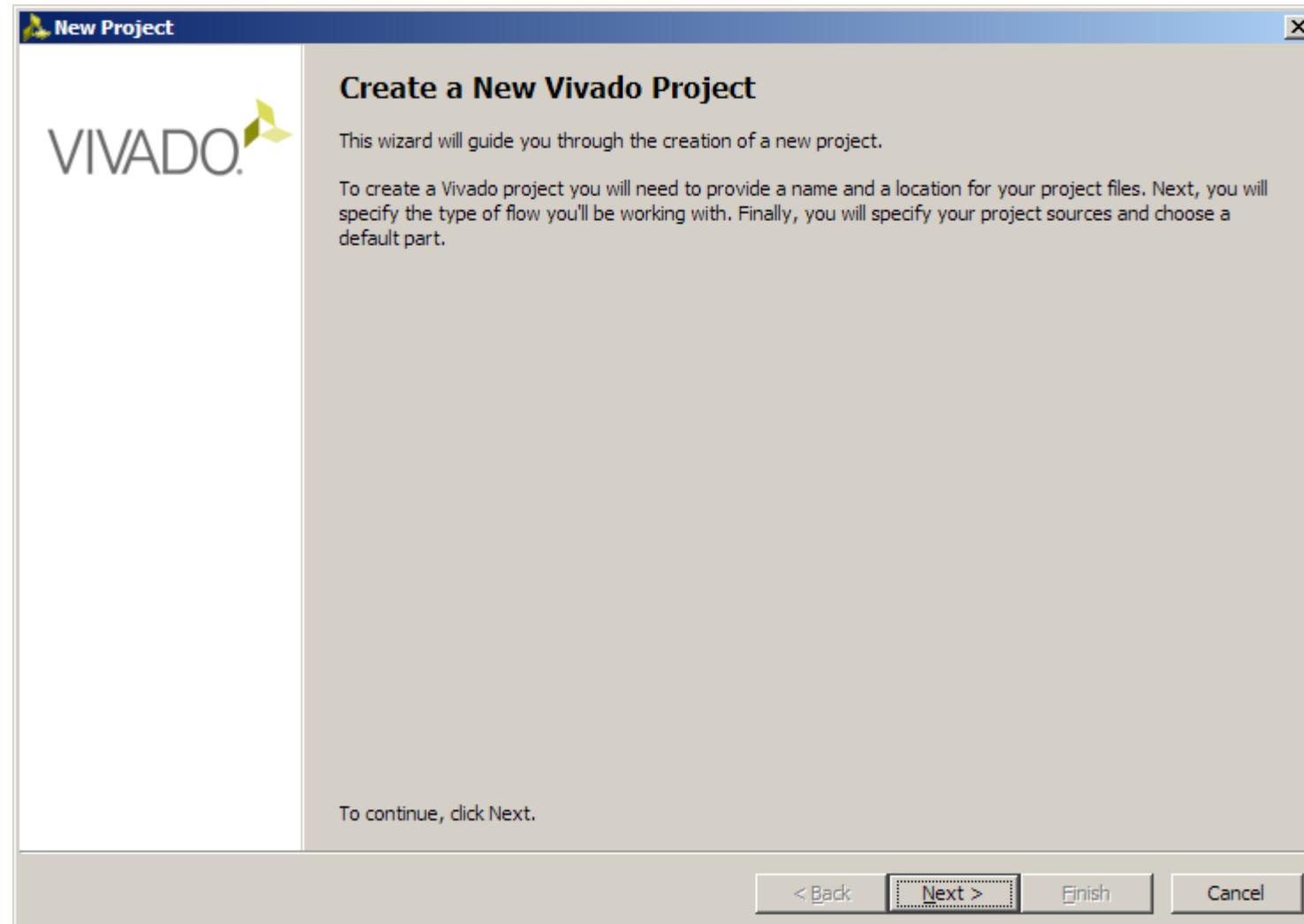
Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

## ► Select Create New Project



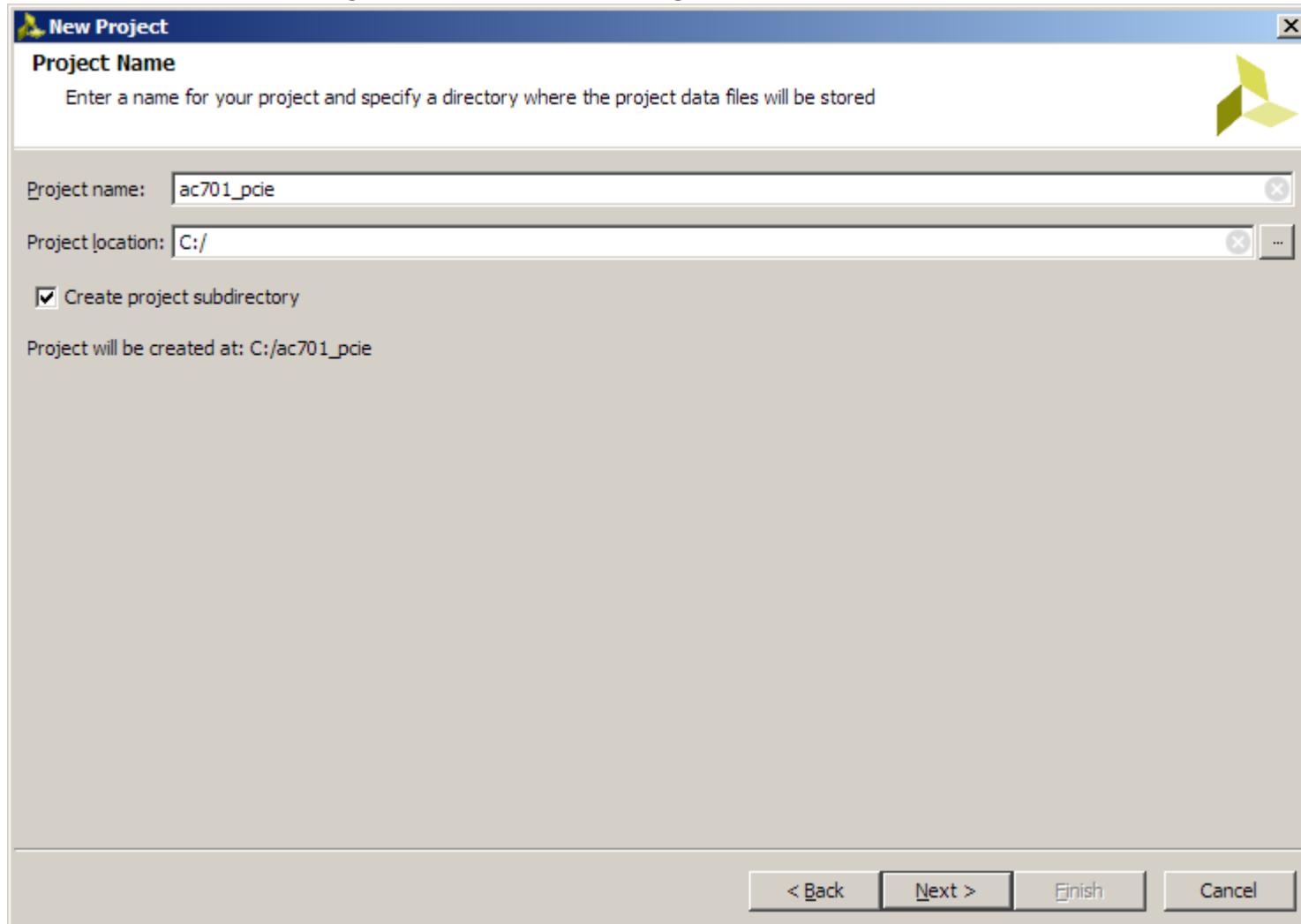
# Generate x4 Gen 2 PCIe Core

► Click Next



# Generate x4 Gen 2 PCIe Core

- Set the Project name and location to ac701\_pcnie and C:\
  - Check Create Project Subdirectory



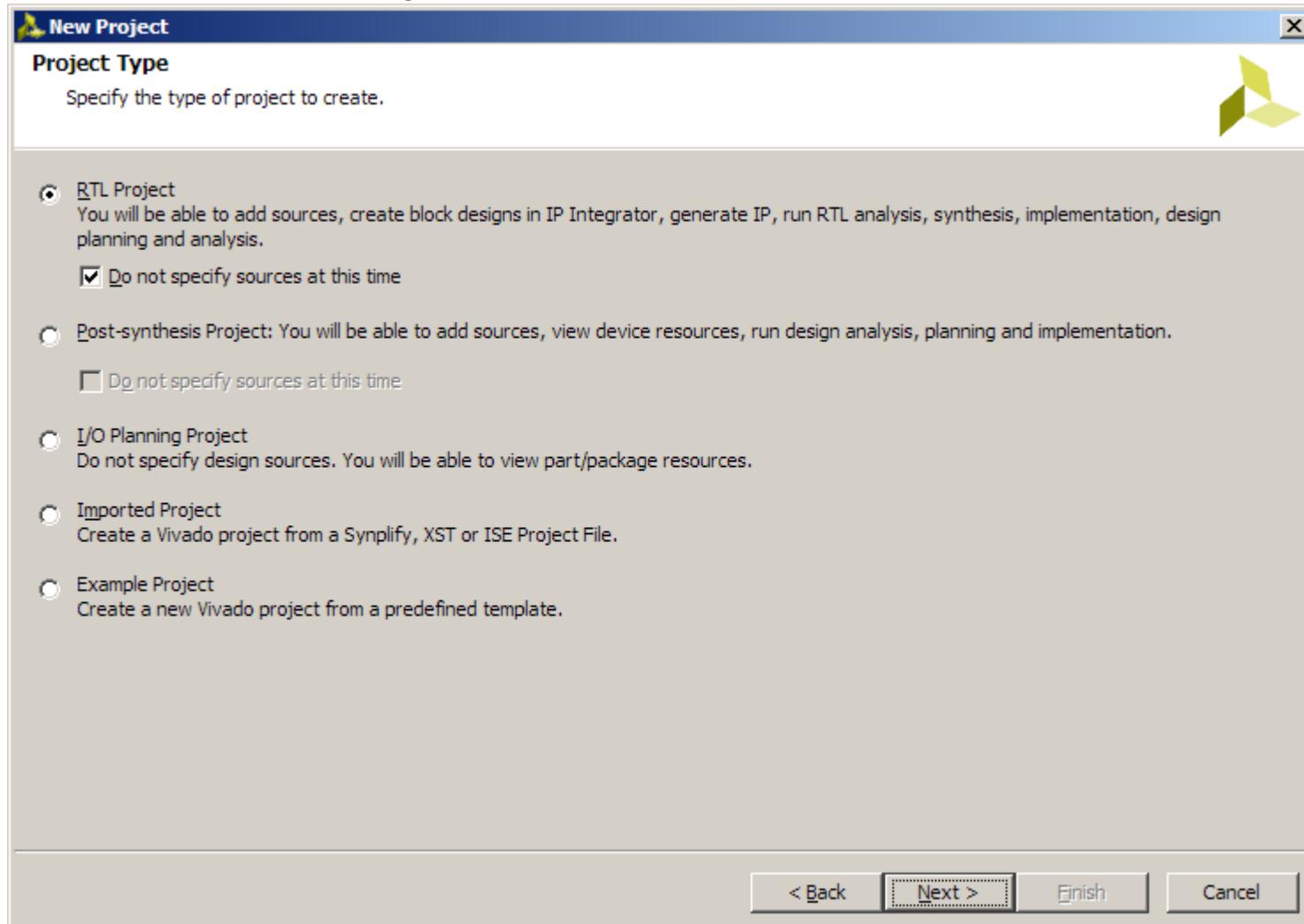
Note: Vivado generally requires forward slashes in paths

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# Generate x4 Gen 2 PCIe Core

## ► Select RTL Project

- Select **Do not specify sources at this time**



# Generate x4 Gen 2 PCIe Core

## ► Select the AC701 Board

The screenshot shows the 'New Project' dialog with the title 'Default Part'. The instructions say 'Choose a default Xilinx part or board for your project. This can be changed later.' Below this, there are three dropdown filters: 'Select: Parts' (selected), 'Boards', 'Filter', 'Vendor: All', 'Display Name: All', and 'Board Rev: Latest'. A 'Reset All Filters' button is also present. A search bar with a magnifying glass icon is below the filters. The main area displays a table of evaluation boards:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3	200
<b>Artix-7 AC701 Evaluation Platform</b>	xilinx.com	1.1	xc7a200tffg676-2	676	1.2	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcku040-ffva1156-2-e	1,156	1.0	520
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.2	700
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.6	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.2	362

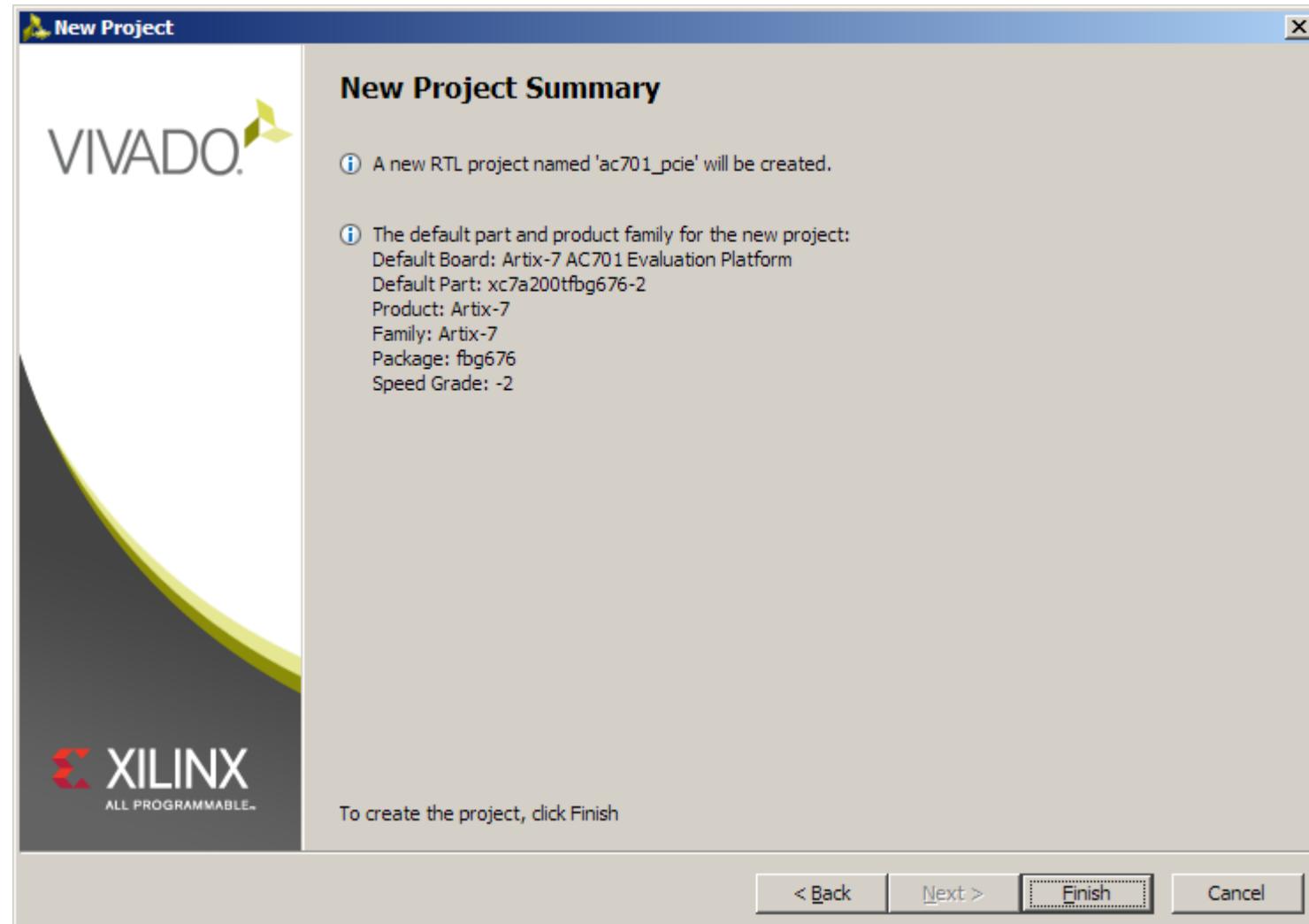
At the bottom are navigation buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

Note: Presentation applies to the AC701

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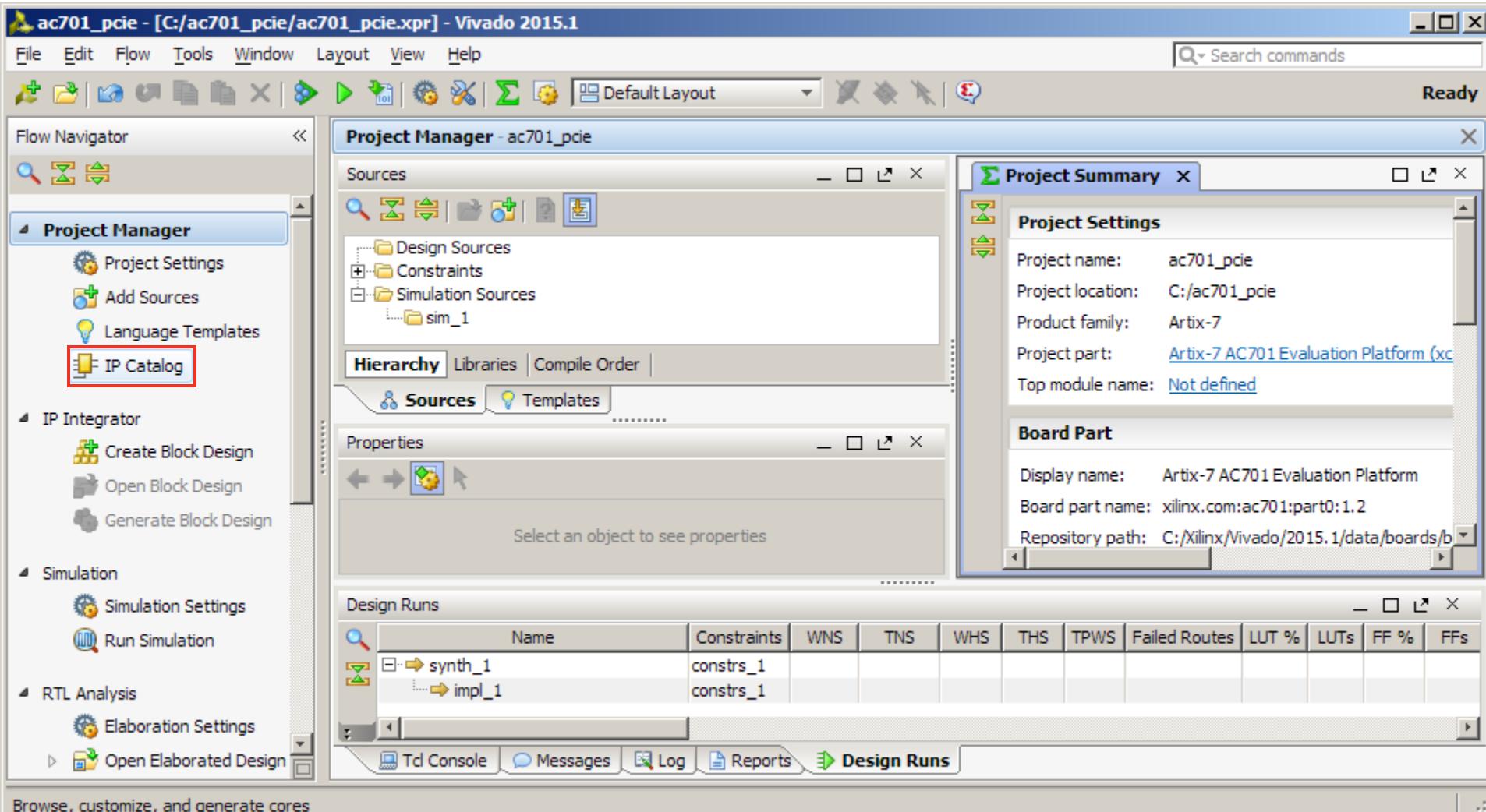
# Generate x4 Gen 2 PCIe Core

► Click Finish



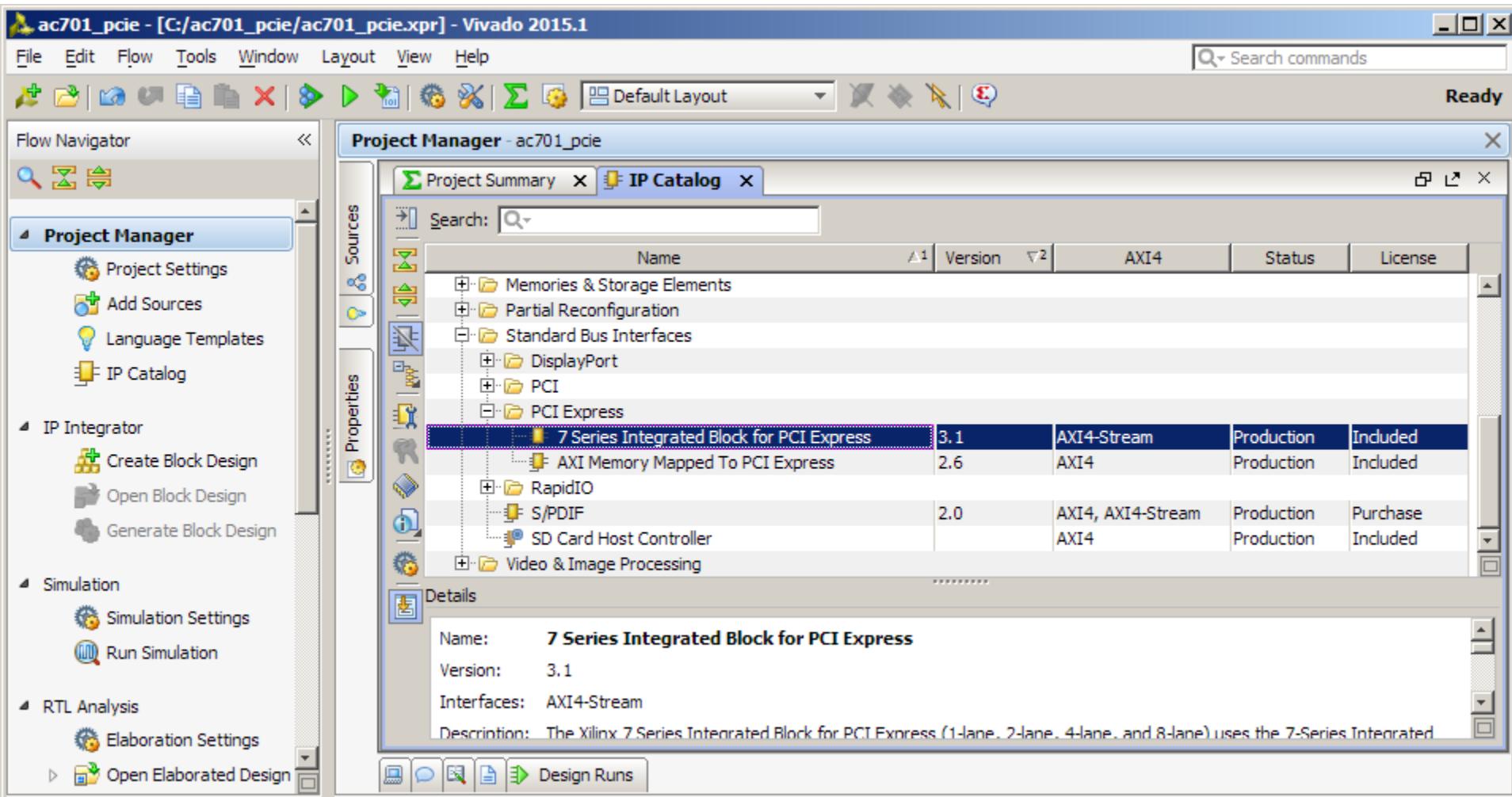
# Generate x4 Gen 2 PCIe Core

► Click on IP Catalog



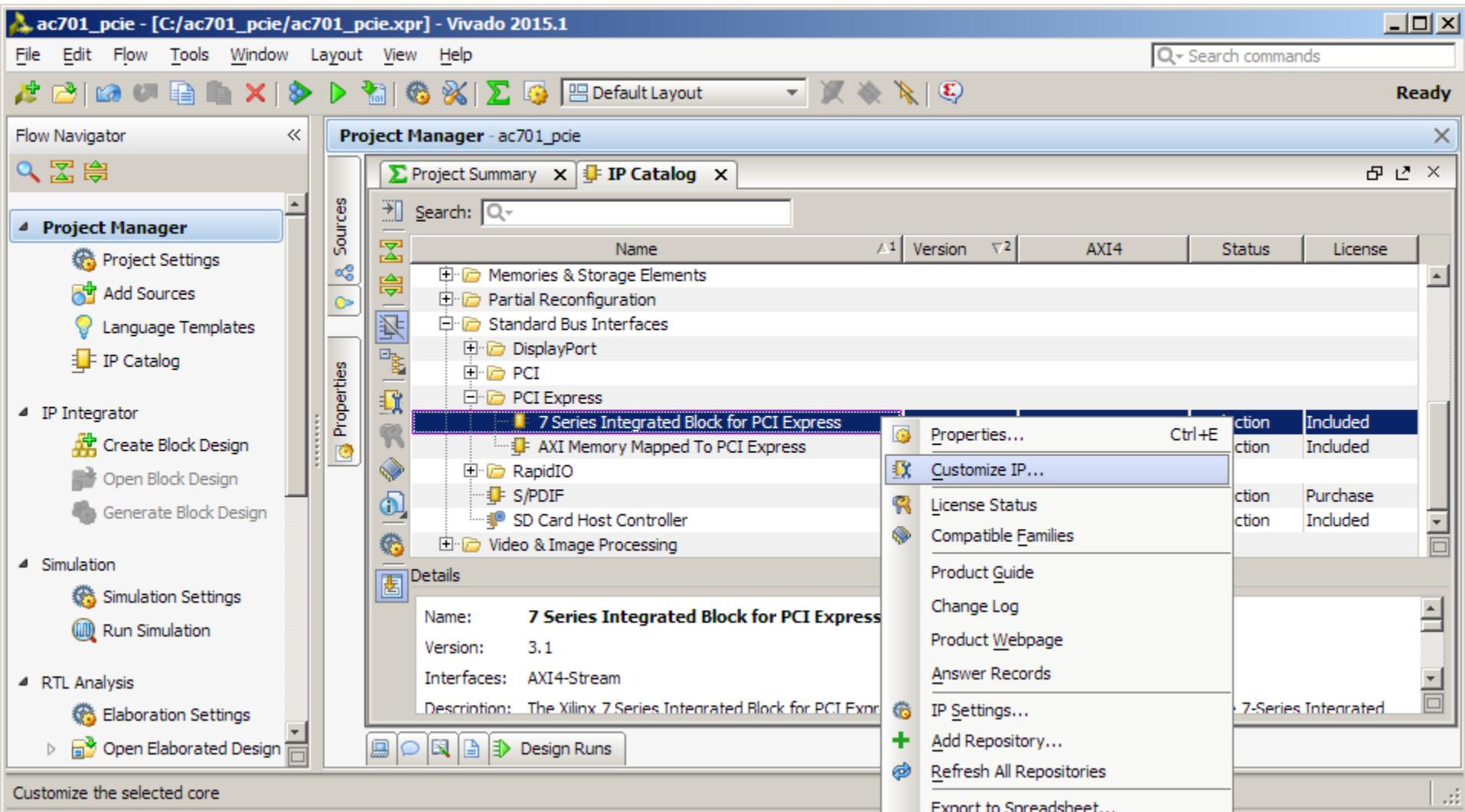
# Generate x4 Gen 2 PCIe Core

- ▶ Select 7 Series Integrated Block for PCI Express, v3.1 under Standard Bus Interfaces



# Generate x4 Gen 2 PCIe Core

- Right click on 7 Series Integrated Block for PCI Express
  - Select Customize IP



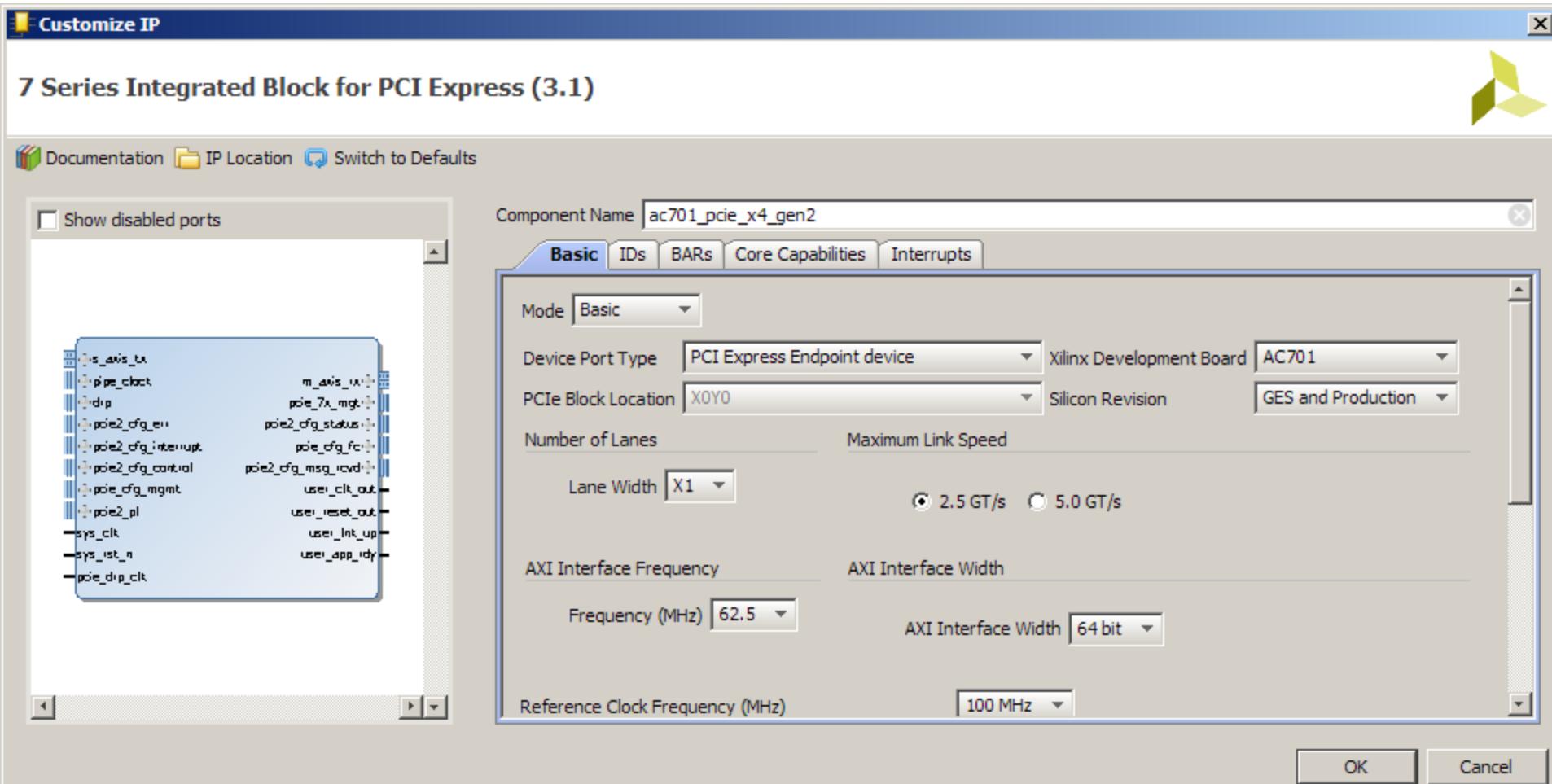
Note: Presentation applies to the AC701

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# Generate x4 Gen 2 PCIe Core

► Under the Basic tab,

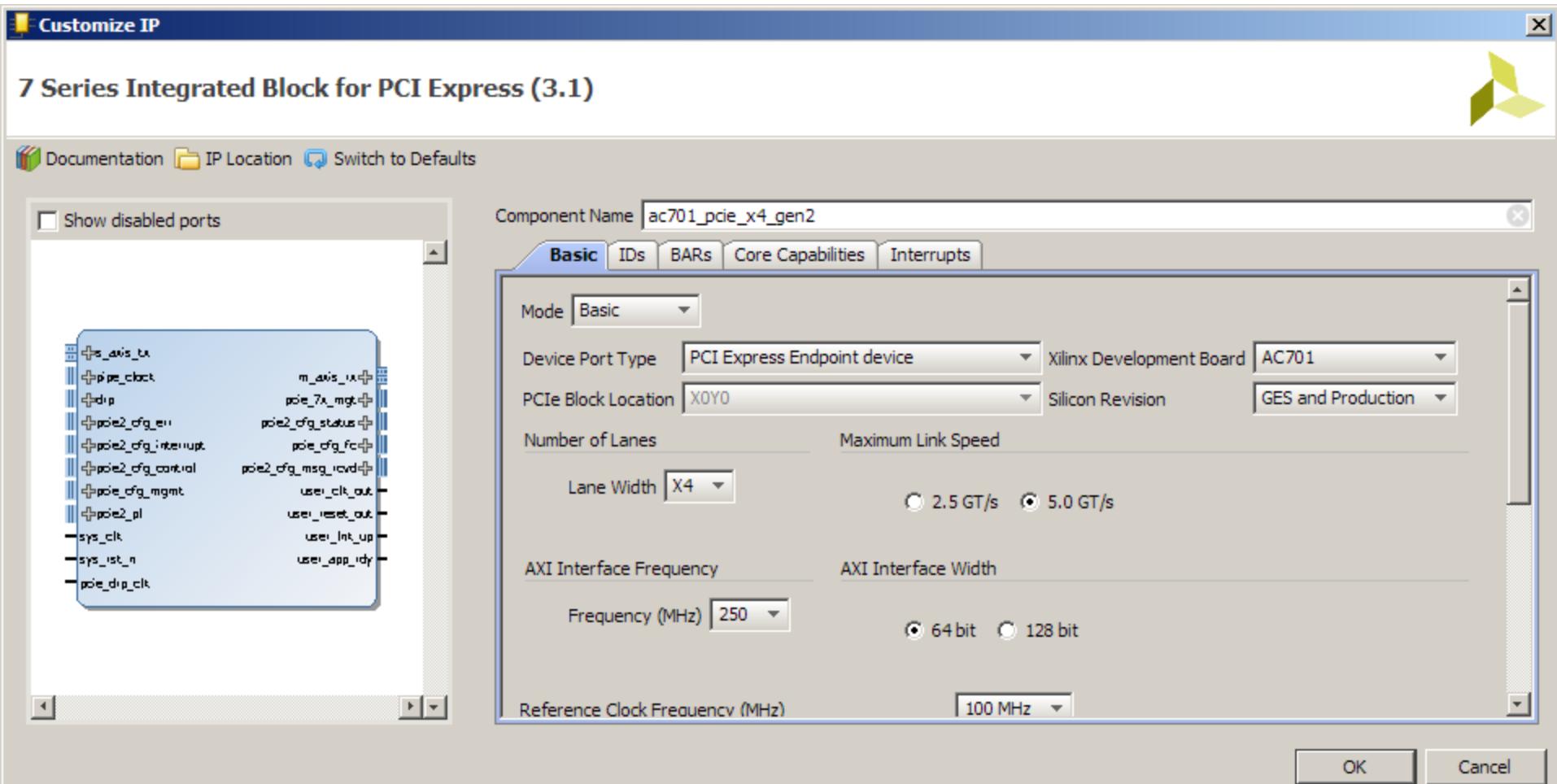
- Set Component name to **ac701\_pcie\_x4\_gen2**
- Set Development Board to **AC701**
- Set Silicon to **GES and Production**



# Generate x4 Gen 2 PCIe Core

## ► Under the Basic tab,

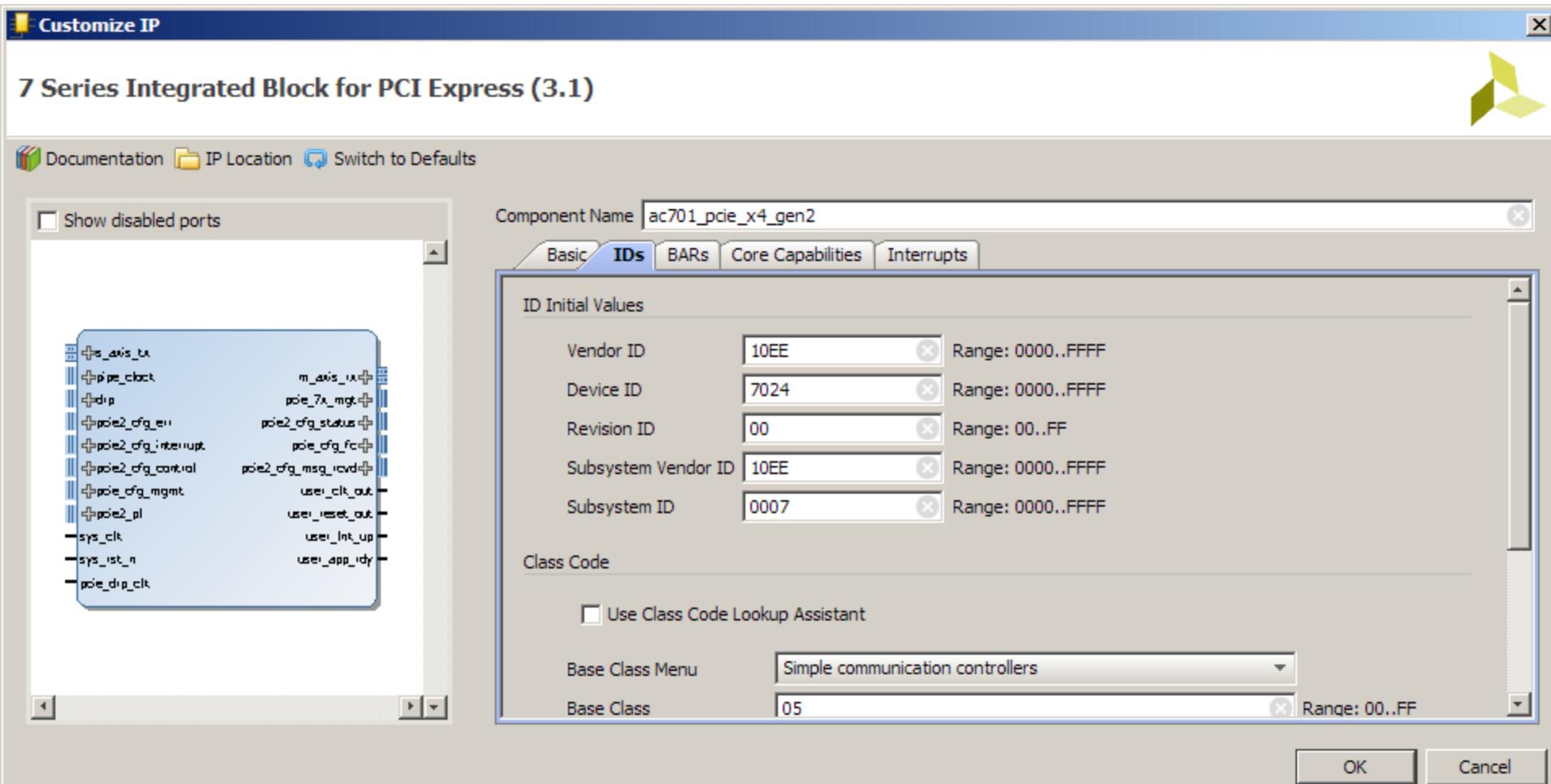
- Set the Lane Width to **X4**
- Set the Max Link Speed to **5 GT/s**
- Set the Ref Clock to **100 MHz**



# Generate x4 Gen 2 PCIe Core

## ► Under the IDs tab, note the ID Initial Values

- Vendor ID = **10EE**; Device ID = **7024**; Revision ID = **00**
- Subsystem Vendor ID = **10EE**; Subsystem ID = **0007**

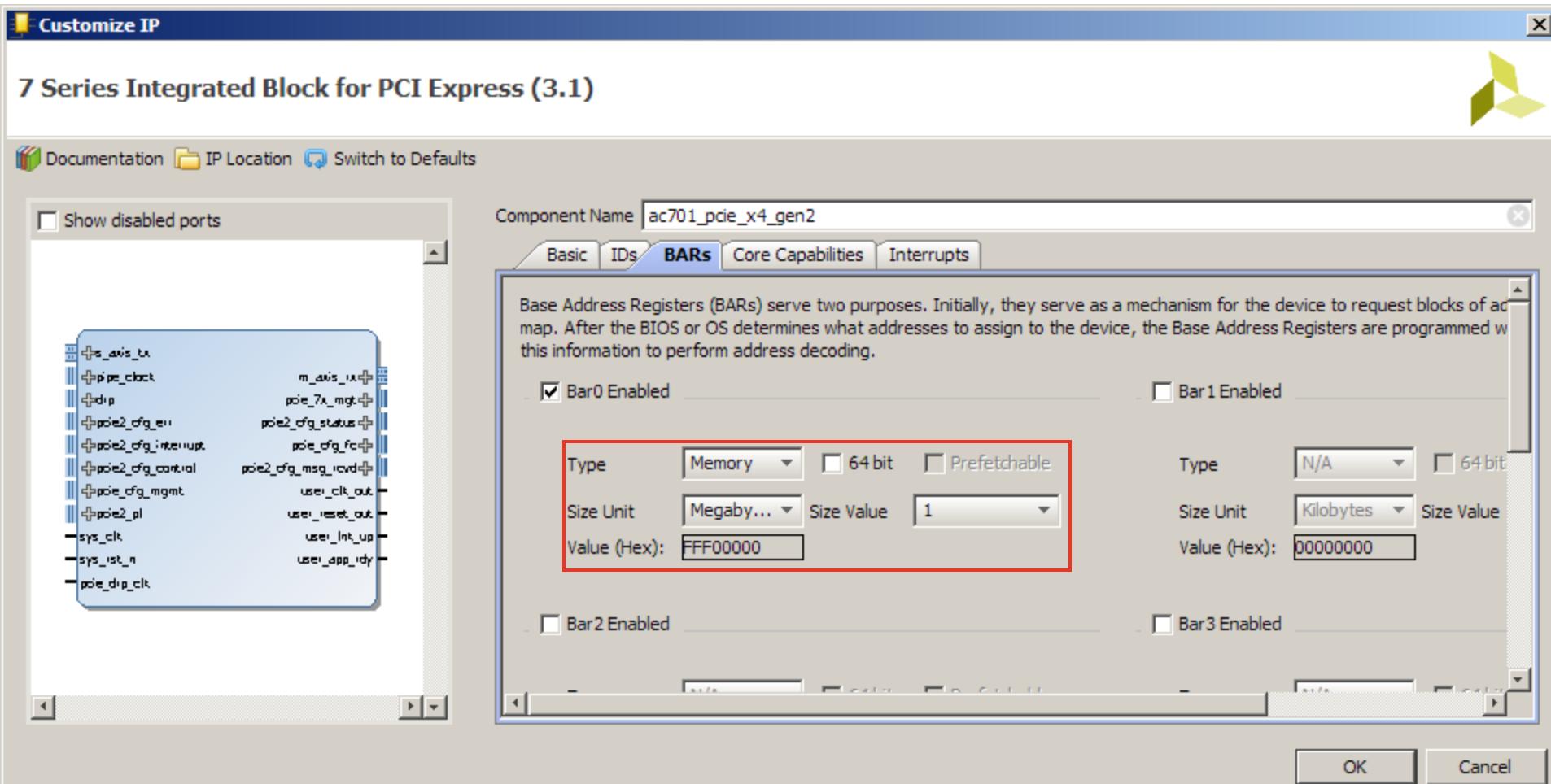


# Generate x4 Gen 2 PCIe Core

► Under the BARs tab, set BAR 0

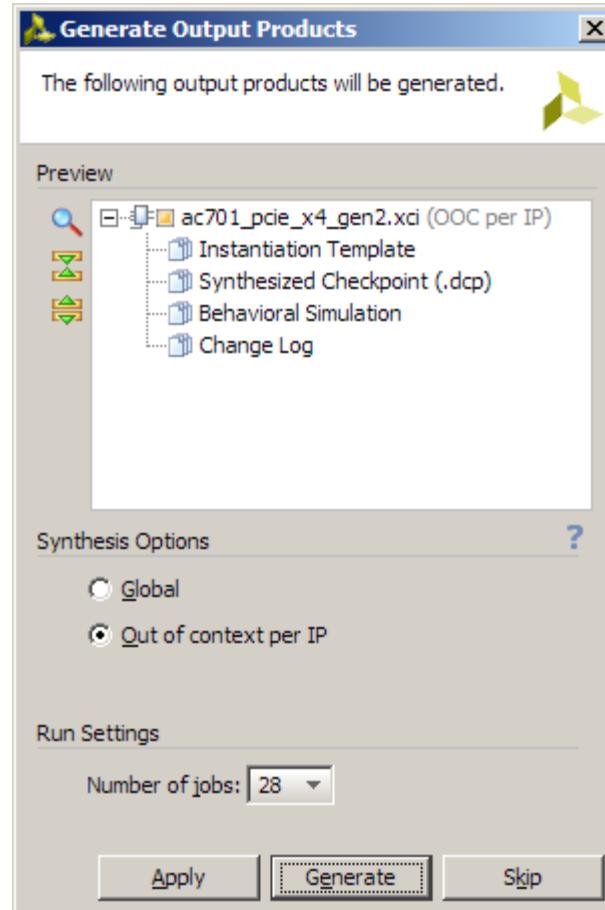
- Set to 1 Megabytes

► Click OK



# Generate x4 Gen 2 PCIe Core

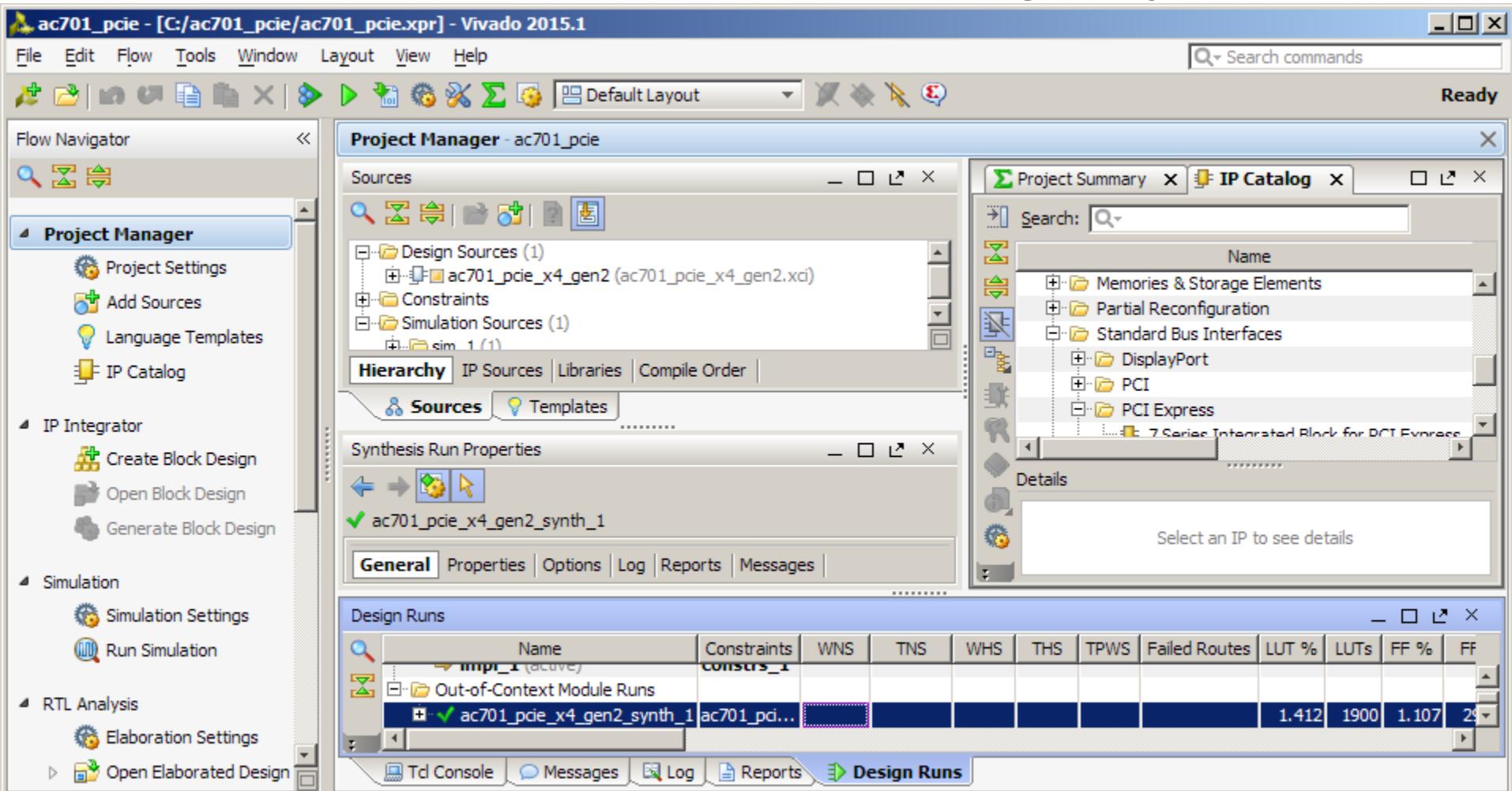
► Click Generate



# Generate x4 Gen 2 PCIe Core

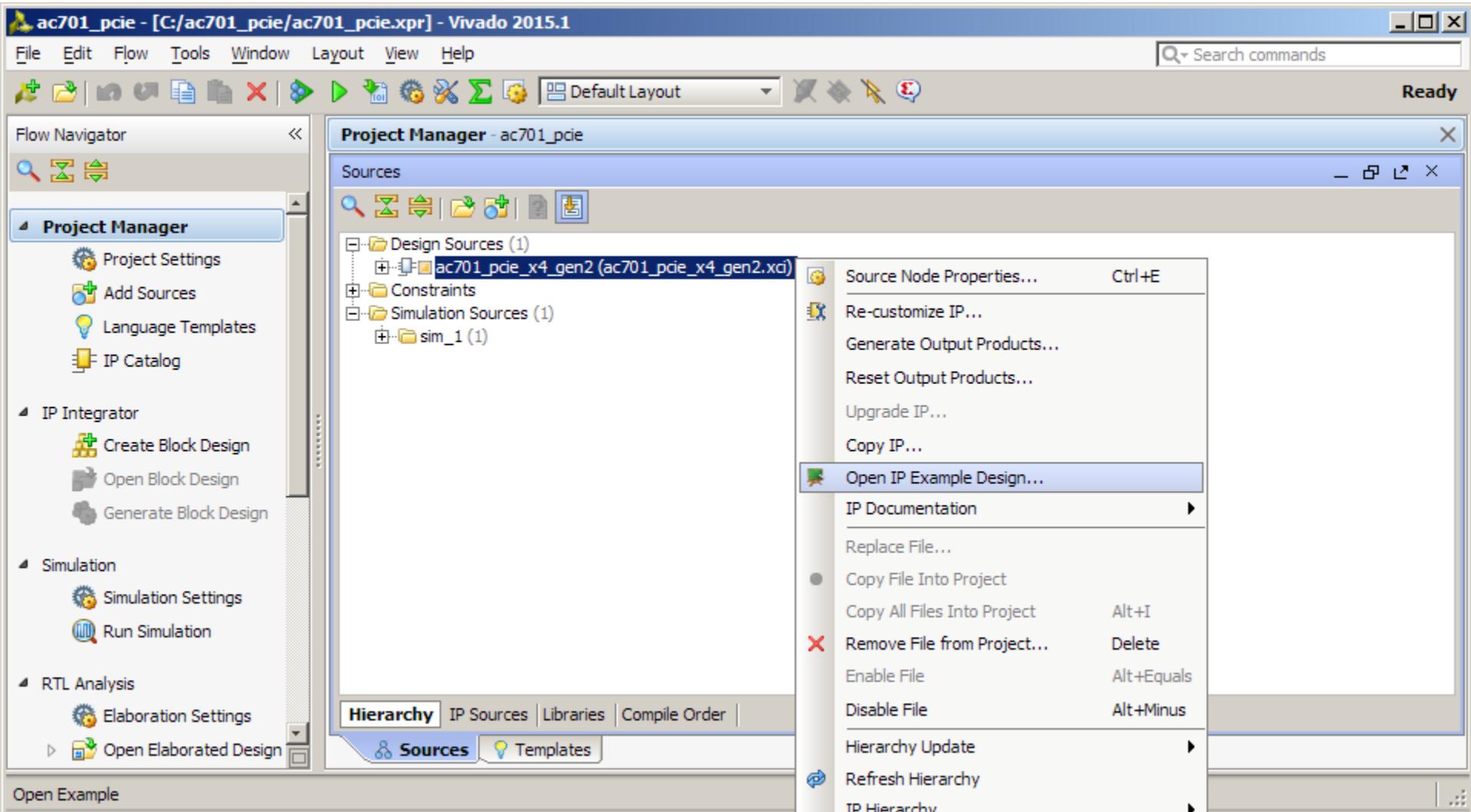
## ► PCIe design appears in Design Sources

- Wait until checkmark appears on ac701\_PCIE\_x4\_gen2\_synth\_1



# Generate x4 Gen 2 PCIe Core

- Right-click on ac701\_PCIE\_x4\_gen2 and select Open IP Example Design...

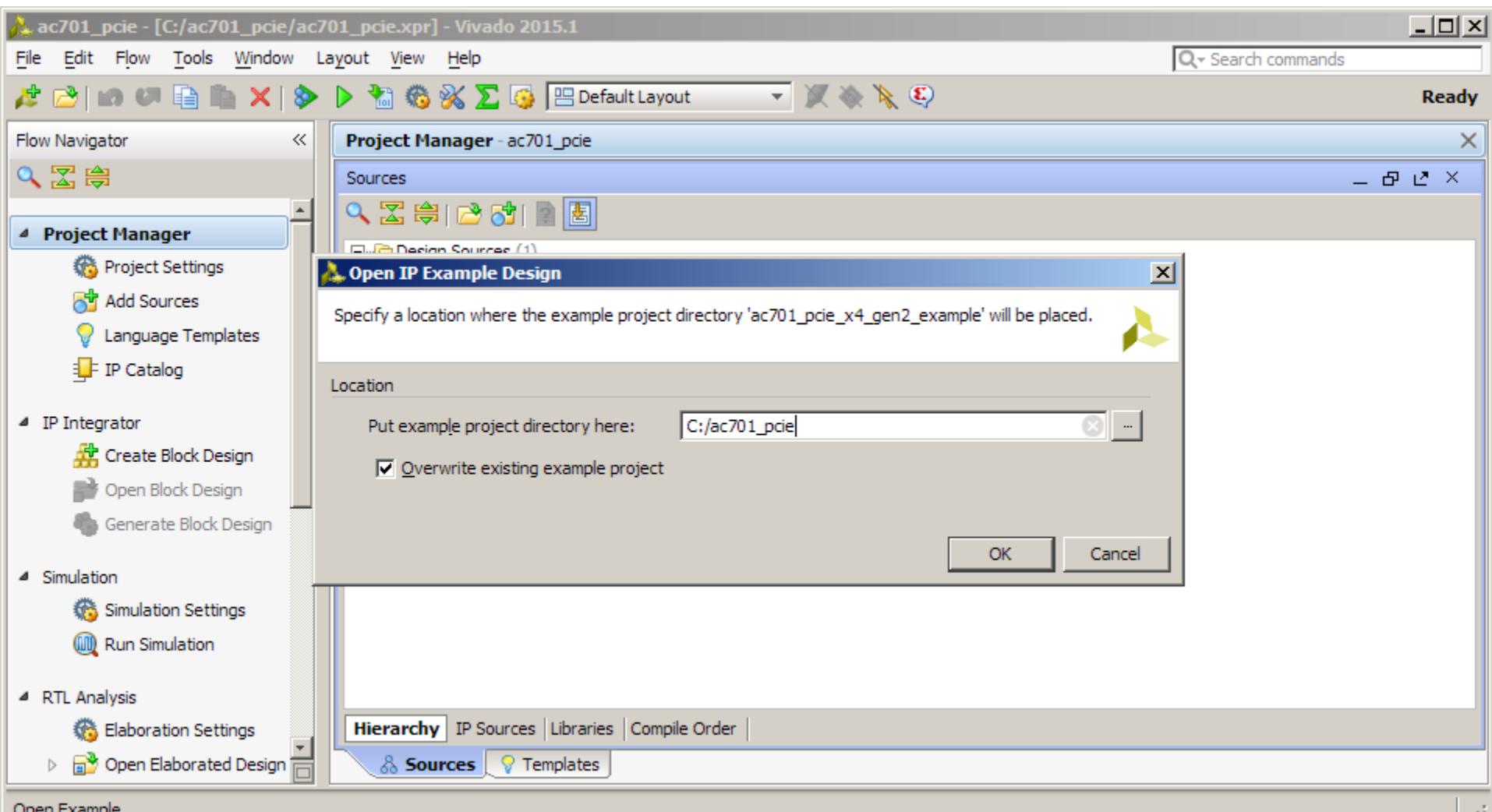


Note: Presentation applies to the AC701

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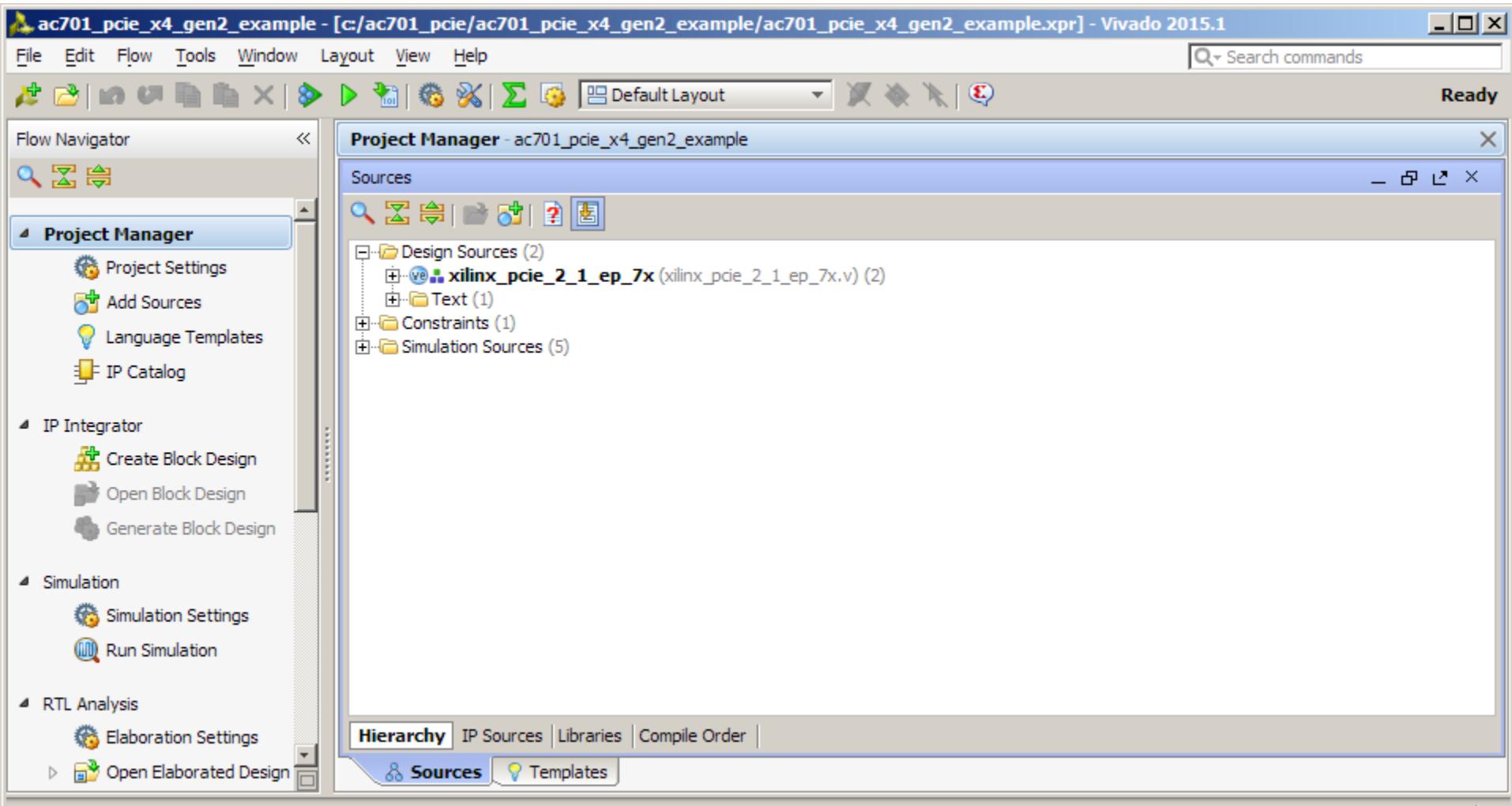
# Generate x4 Gen 2 PCIe Core

► Set the location to C:/ac701\_pcnie and click OK



# Generate x4 Gen 2 PCIe Core

- A new project is created



Note: The original project window can be closed

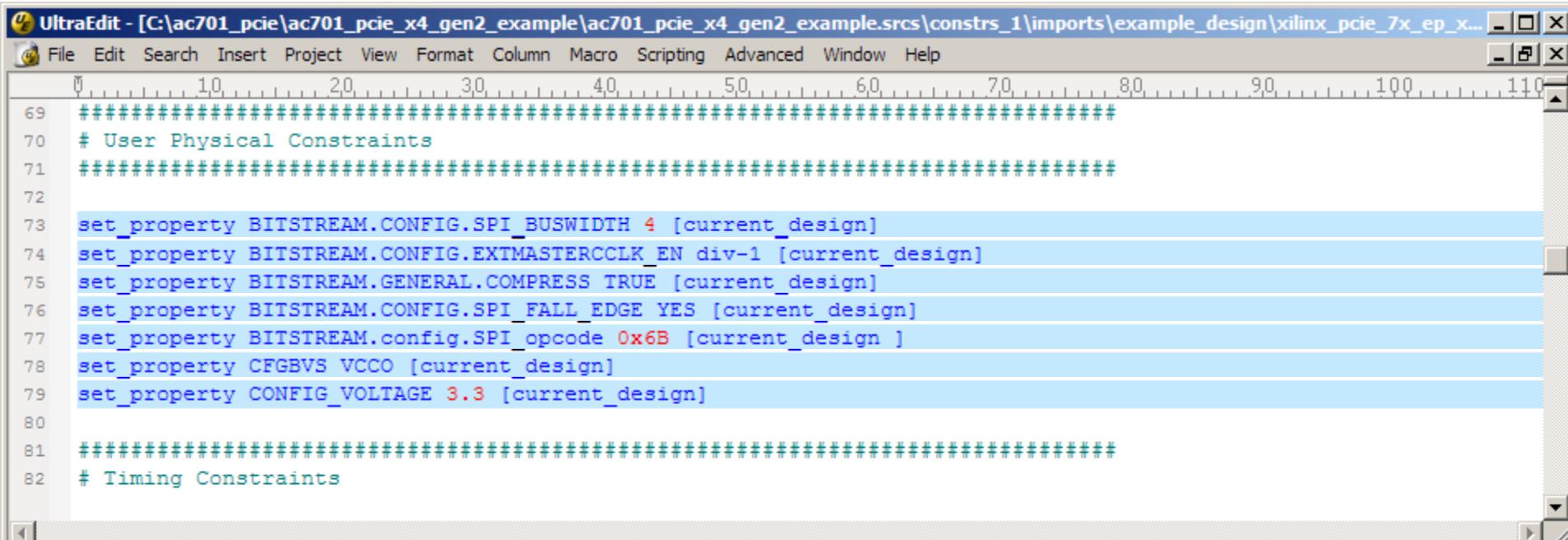
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# Modify PCIe Core

► As per [UG470](#), [UG899](#), [UG908](#), and [N25Q256 Flash](#) specifications

- In the XDC file, `xilinx_pcie_7x_ep_x4g2_AC701.xdc`, add these lines:

```
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
```



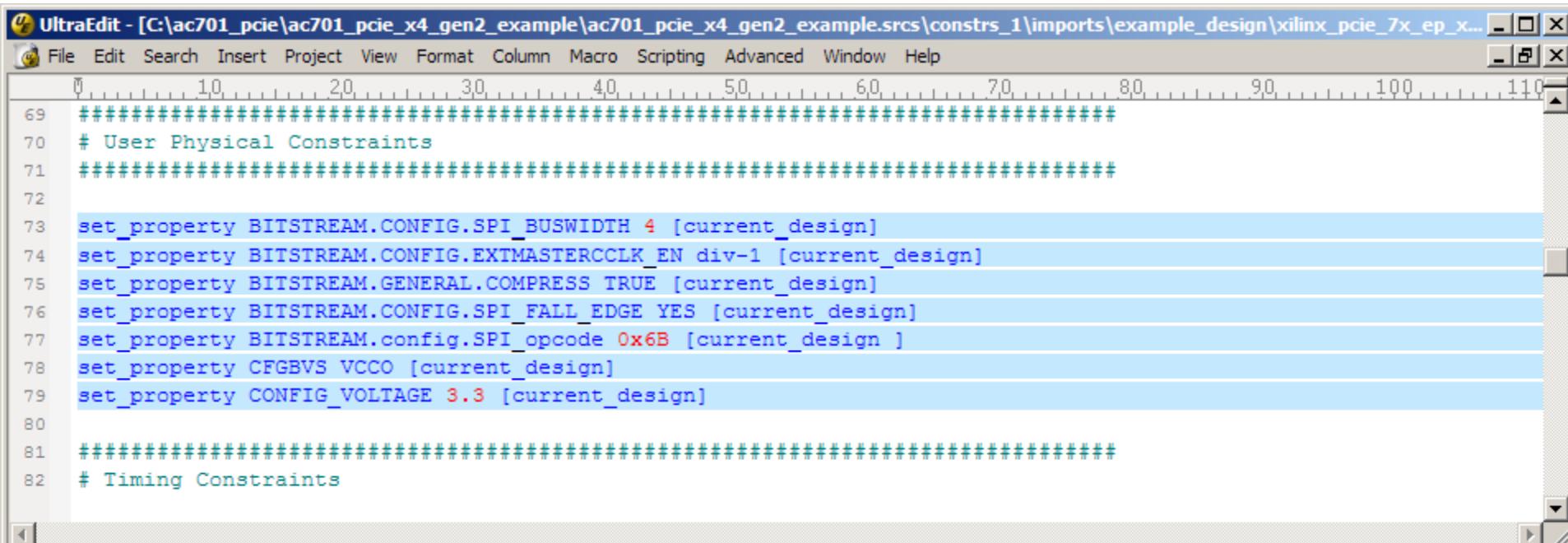
The screenshot shows the UltraEdit text editor displaying an XDC file. The file contains comments and several set\_property commands. The code is as follows:

```
UltraEdit - [C:\ac701_PCIE\ac701_PCIE_X4_GEN2_EXAMPLE\ac701_PCIE_X4_GEN2_EXAMPLE.srcs\constrs_1\imports\example_design\xilinx_PCIE_7X_EP_X4G2_AC701.xdc]
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
69 #####
70 # User Physical Constraints
71 #####
72
73 set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
74 set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
75 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
76 set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
77 set_property BITSTREAM.config.SPI_opcode 0x6B [current_design ]
78 set_property CFGBVS VCCO [current_design]
79 set_property CONFIG_VOLTAGE 3.3 [current_design]
80
81 #####
82 # Timing Constraints
```

# Modify PCIe Core

## ► Details on the XDC constraints :

- N25Q256 Maximum Frequency: 108 MHz; AC701 EMCCLK Freq: 90 MHz
- **BITSTREAM.CONFIG.SPI\_BUSWIDTH 4**: For Quad SPI
- **BITSTREAM.CONFIG.EXTMMASTERCCLK\_EN div-1**: Sets the EMCCLK in the FPGA to divide by 1
- **BITSTREAM.GENERAL.COMPRESS TRUE**: Shrinks the bitstream
- **BITSTREAM.CONFIG.SPI\_FALL\_EDGE YES**: Improves SPI loading speed



The screenshot shows a Windows application window titled "UltraEdit - [C:\ac701\_PCIE\ac701\_PCIE\_x4\_gen2\_example\ac701\_PCIE\_x4\_gen2\_example.srcts\constrs\_1\imports\example\_design\xilinx\_PCIE\_7x\_EP.xdc]". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The status bar at the bottom shows line numbers from 69 to 82. The code area contains the following XDC constraints:

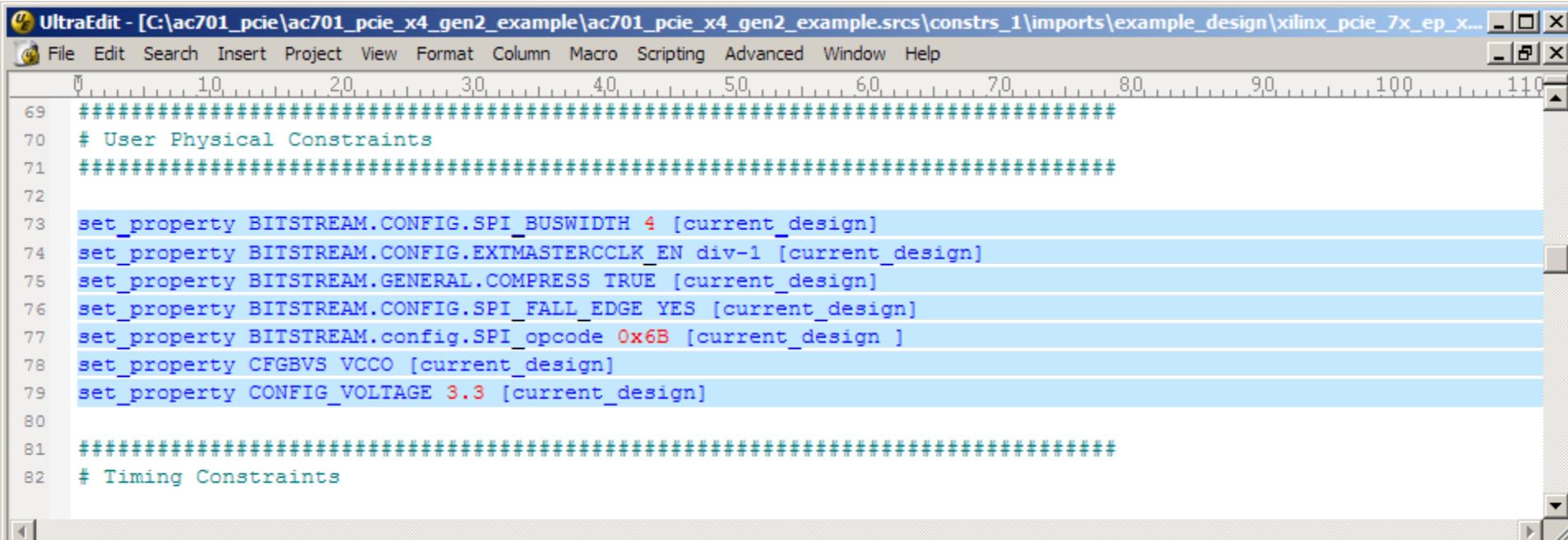
```
# User Physical Constraints
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
set_property BITSTREAM.config.SPI_opcode 0x6B [current_design ]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]

# Timing Constraints
```

# Modify PCIe Core

## ► Details on the XDC constraints :

- **CFGVBUS VCCO**: Set to VCCO when CONFIG\_VOLTAGE is either 2.5 or 3.3 V
- **CONFIG\_VOLTAGE 3.3**: The AC701 Configuration Bank (Bank 0) voltage is connected to 3.3 V

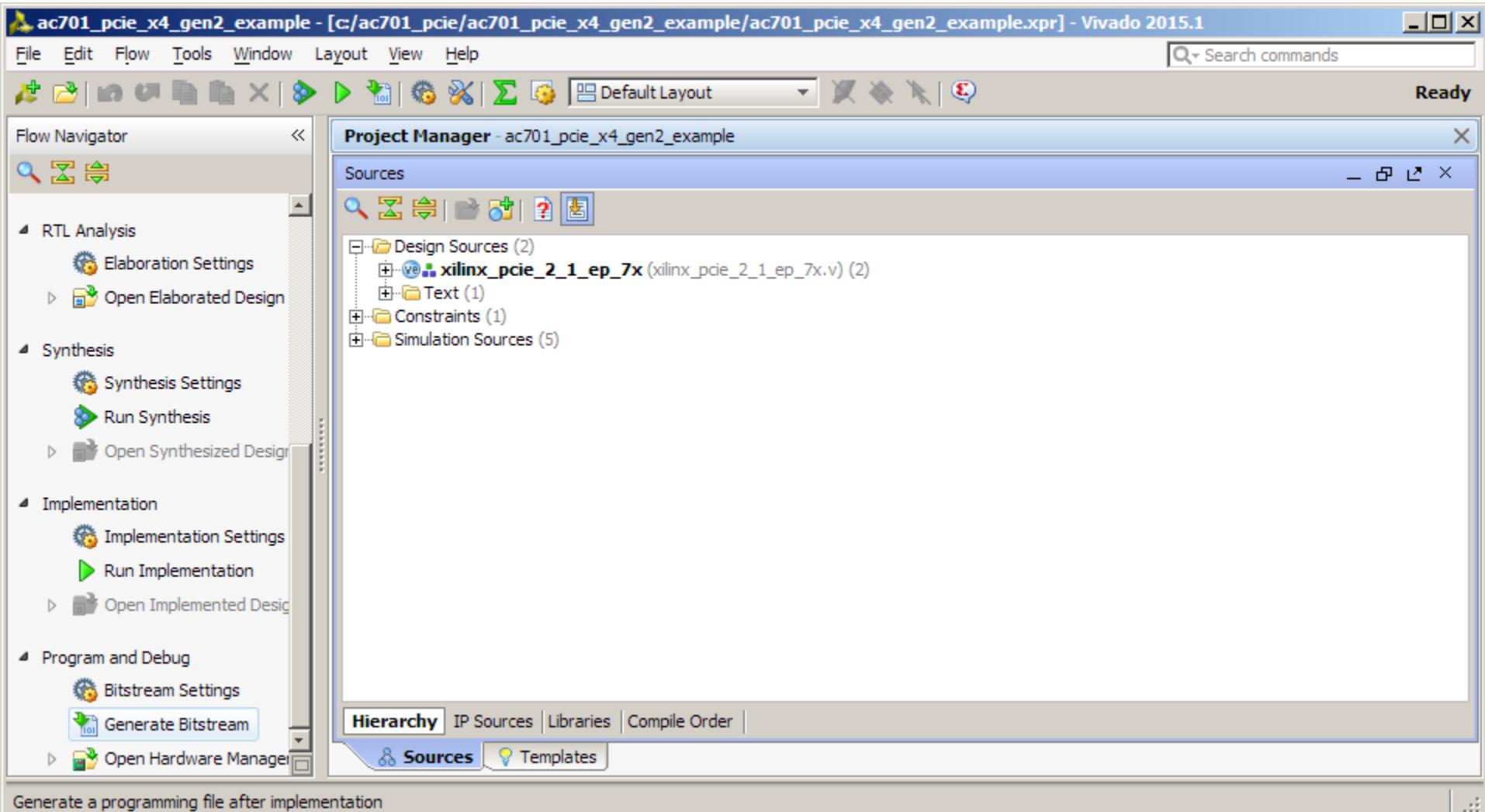


The screenshot shows a window titled "UltraEdit - [C:\ac701\_pcnie\ac701\_pcnie\_x4\_gen2\_example\ac701\_pcnie\_x4\_gen2\_example.srccs\constrs\_1\imports\example\_design\xilinx\_pcnie\_7x\_ep\_x...]" containing XDC constraint code. The code defines physical and timing constraints for a bitstream configuration. It includes properties for SPI bus width, external master clock enable, compression, fall edge, SPI opcode, CFGVBUS VCCO, and CONFIG\_VOLTAGE set to 3.3V. The code is annotated with comments and section markers.

```
UltraEdit - [C:\ac701_pcnie\ac701_pcnie_x4_gen2_example\ac701_pcnie_x4_gen2_example.srccs\constrs_1\imports\example_design\xilinx_pcnie_7x_ep_x...
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
0 10 20 30 40 50 60 70 80 90 100 110
69 ######
70 # User Physical Constraints
71 #####
72
73 set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
74 set_property BITSTREAM.CONFIG.EXTMASTERCLK_EN div-1 [current_design]
75 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
76 set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
77 set_property BITSTREAM.config.SPI_opcode 0x6B [current_design ]
78 set_property CFGVBUS VCCO [current_design]
79 set_property CONFIG_VOLTAGE 3.3 [current_design]
80
81 #####
82 # Timing Constraints
```

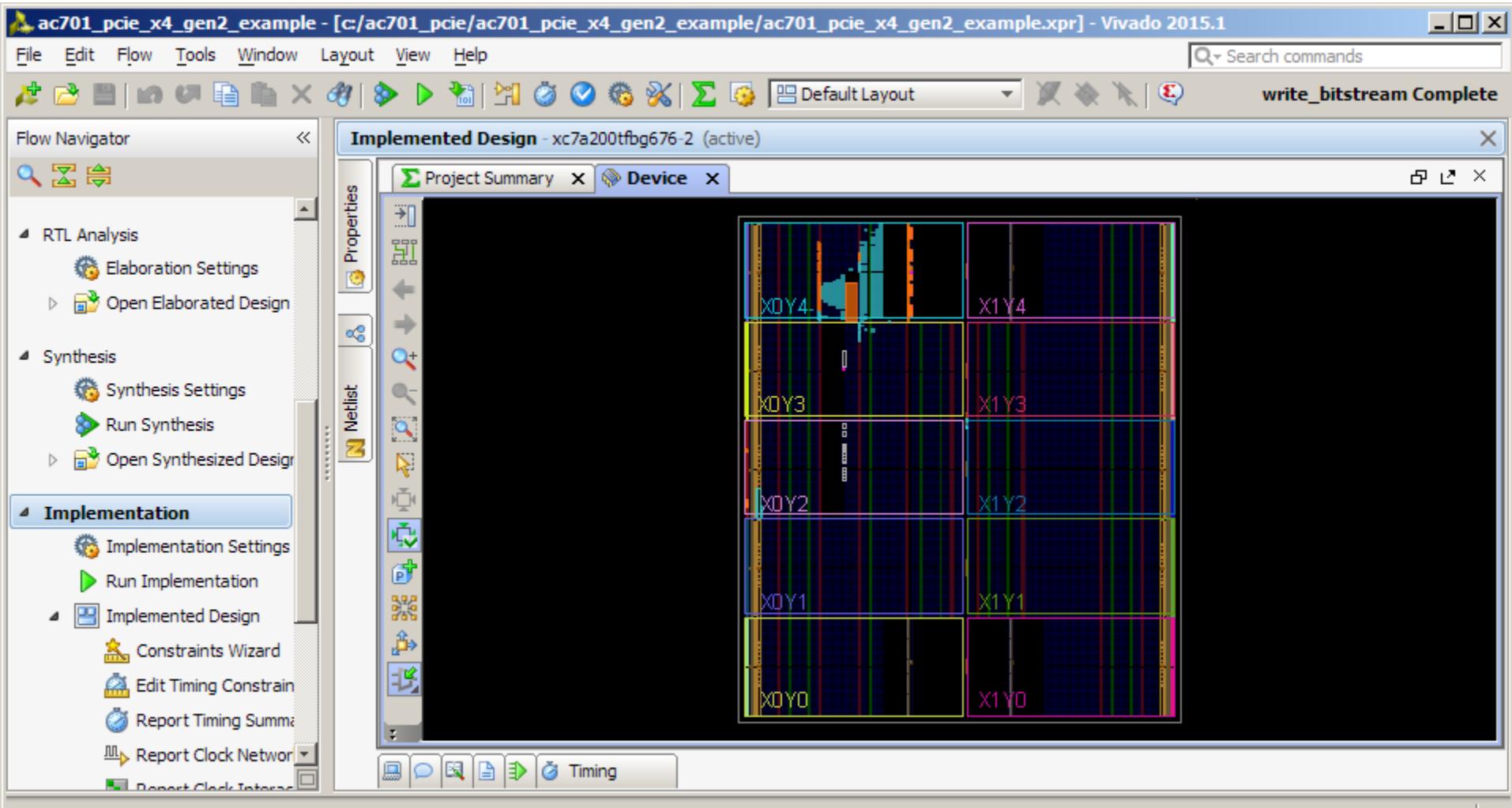
# Compile Example Design

► Click on Generate Bitstream



# Compile Example Design

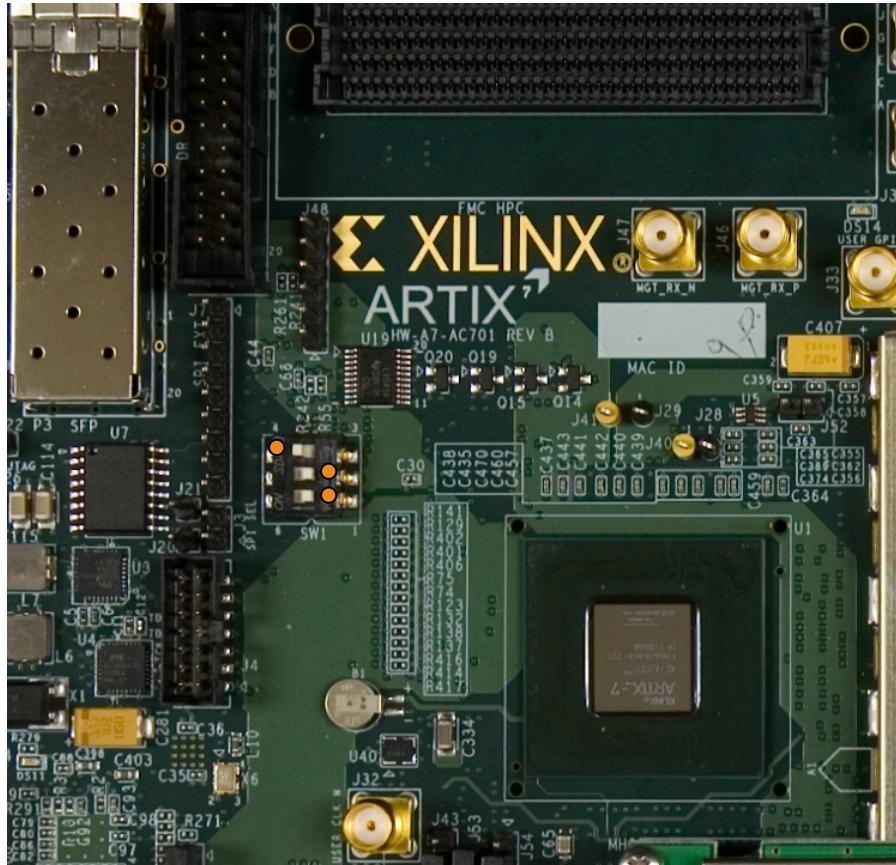
► Open and view the Implemented Design



# Hardware Setup

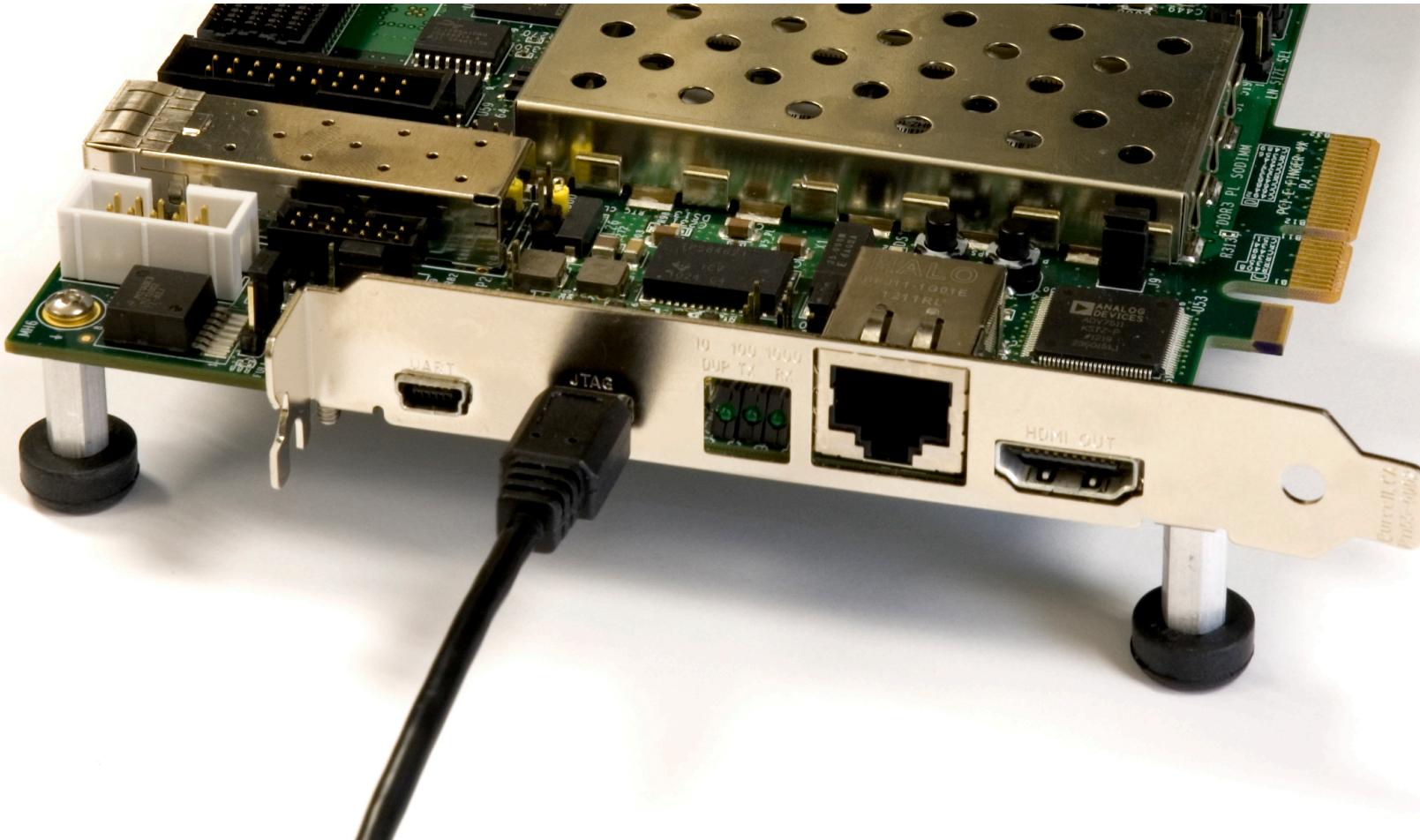
## ► Set SW1 to 001 (1 = on, Position 1 → Position 3)

- This enables Master SPI configuration from the N25Q SPI Flash
- FPGA mode pins M[2:0] = 001



# Hardware Setup

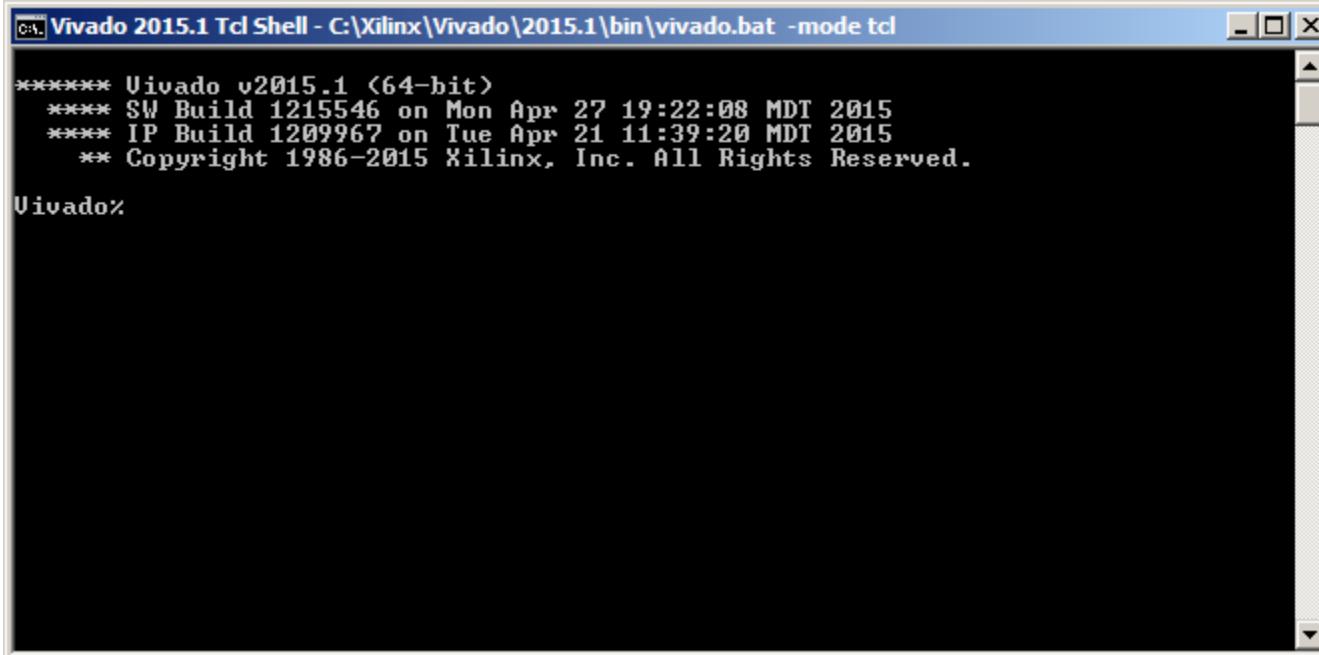
- ▶ Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the AC701 board
  - Connect this cable to your PC
  - Power on the AC701 board



# Generate PCIe MCS File

## ► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2015.1 →  
Vivado 2015.1 Tcl Shell**

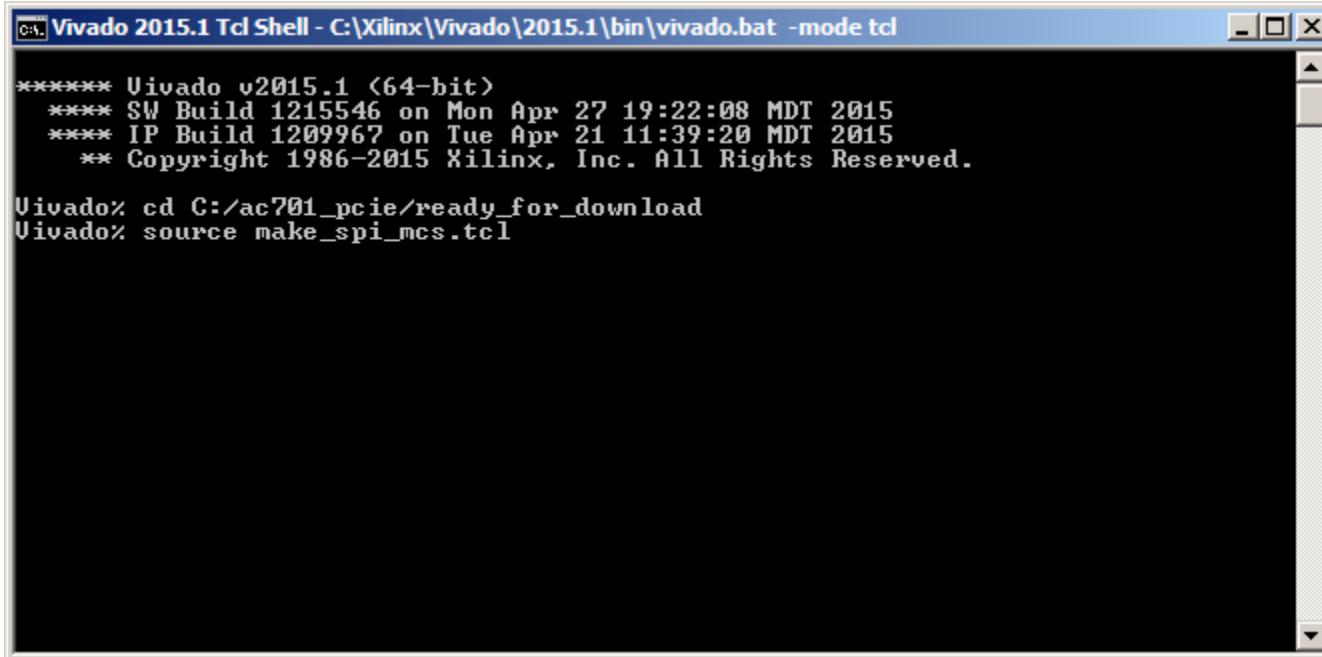


The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:  
\*\*\*\*\* Vivado v2015.1 (64-bit)  
\*\*\*\* SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
\*\*\*\* IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
\*\* Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
Vivado%

# Generate PCIe MCS File

- In the Vivado Tcl Shell type:

```
cd C:/ac701_pcie/ready_for_download  
source make_spi_mcs.tcl
```



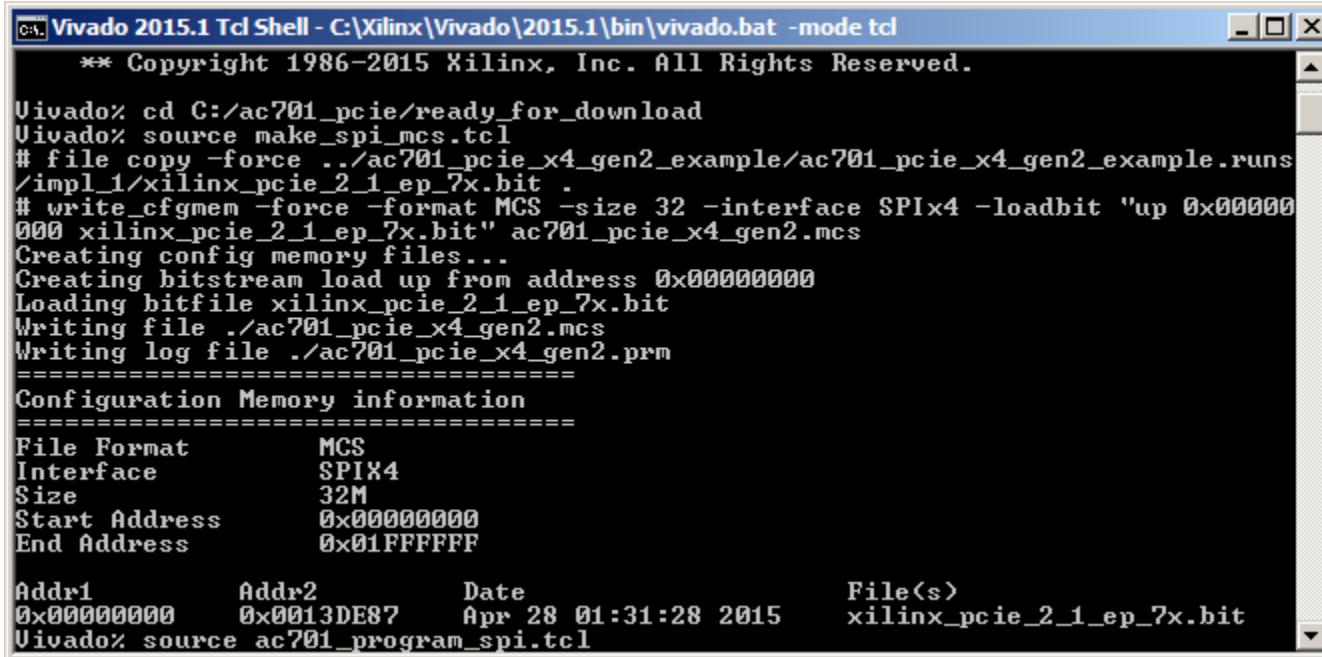
The screenshot shows a Windows command-line interface window titled "C:\ Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2015.1 (64-bit)  
**** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
**** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
  
Vivado% cd C:/ac701_pcie/ready_for_download  
Vivado% source make_spi_mcs.tcl
```

# Program SPI Flash with PCIe Design

- In the Vivado Tcl Shell type:

```
source ac701_program_spi.tcl
```



```
c:\Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

Vivado> cd C:/ac701_pcie/ready_for_download
Vivado> source make_spi_mcs.tcl
# file copy -force ../ac701_pcie_x4_gen2_example/ac701_pcie_x4_gen2_example.runs
/impl_1/xilinx_pcie_2_1_ep_7x.bit .
# write_cfm -force -format MCS -size 32 -interface SPIx4 -loadbit "up 0x000000
000 xilinx_pcie_2_1_ep_7x.bit" ac701_pcie_x4_gen2.mcs
Creating config memory files...
Creating bitstream load up from address 0x00000000
Loading bitfile xilinx_pcie_2_1_ep_7x.bit
Writing file ./ac701_pcie_x4_gen2.mcs
Writing log file ./ac701_pcie_x4_gen2.prm
=====
Configuration Memory information
=====
File Format      MCS
Interface        SPIx4
Size            32M
Start Address   0x00000000
End Address     0x01FFFFFF

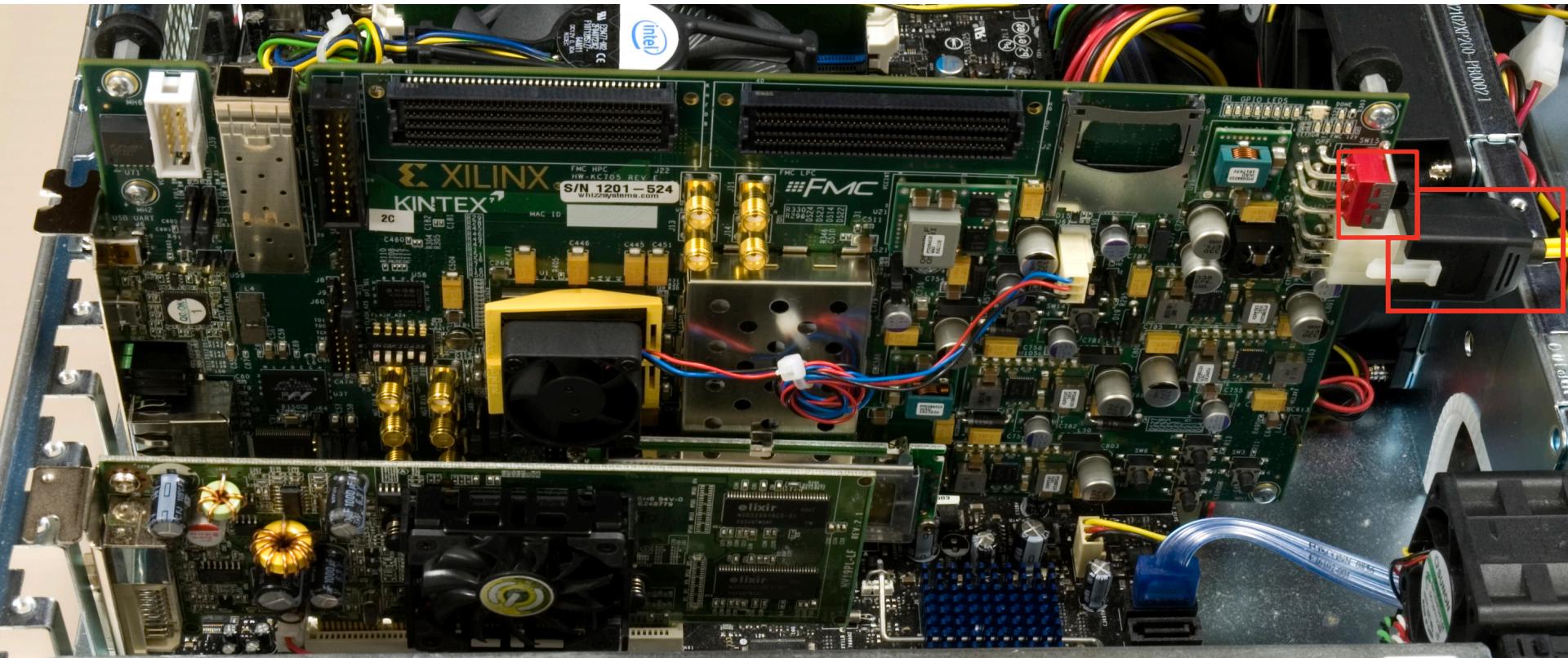
Addr1          Addr2          Date           File(s)
0x0000000000  0x0013DE87  Apr 28 01:31:28 2015  xilinx_pcie_2_1_ep_7x.bit
Vivado> source ac701_program_spi.tcl
```

Note: Takes about a minute

# Hardware Setup

## ► Insert the AC701 Board into a PCIe slot

- Use the included PC Power adapter; turn on Power Switch

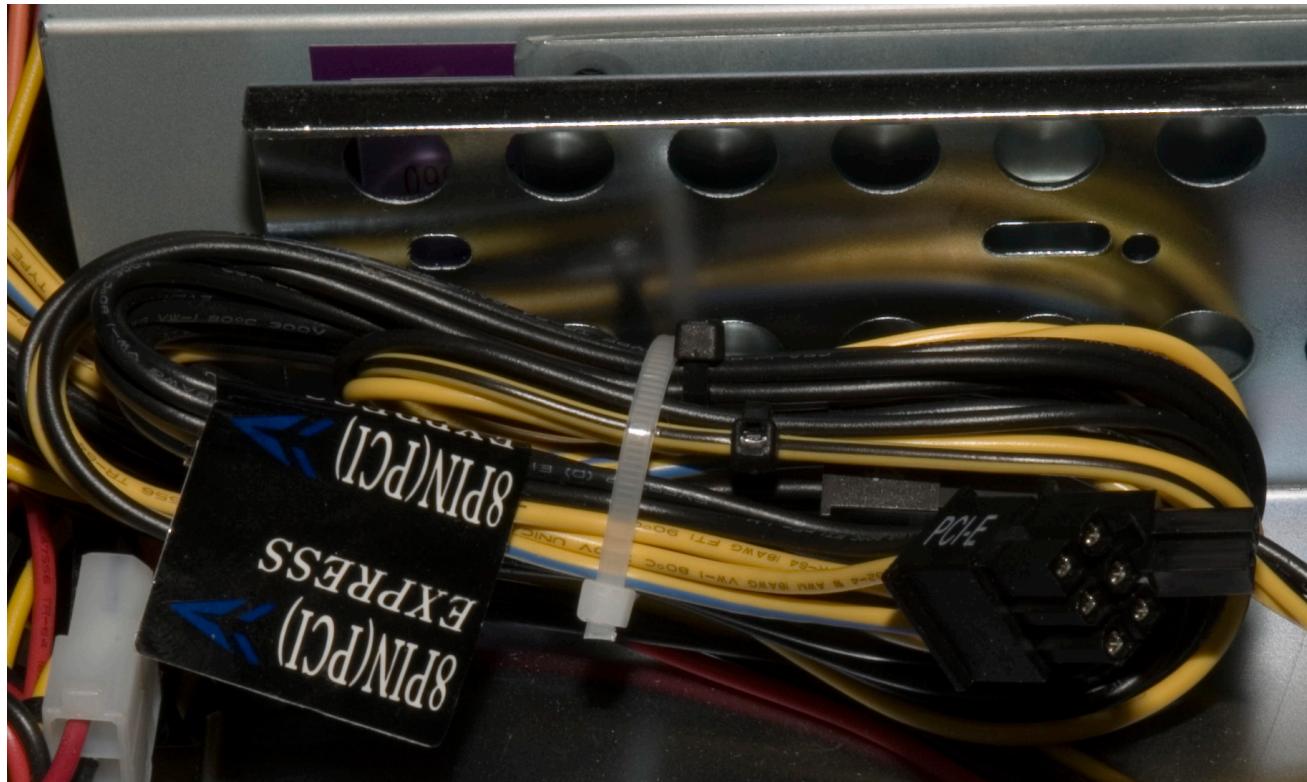


Note: KC705 shown in this photo

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# Hardware Setup

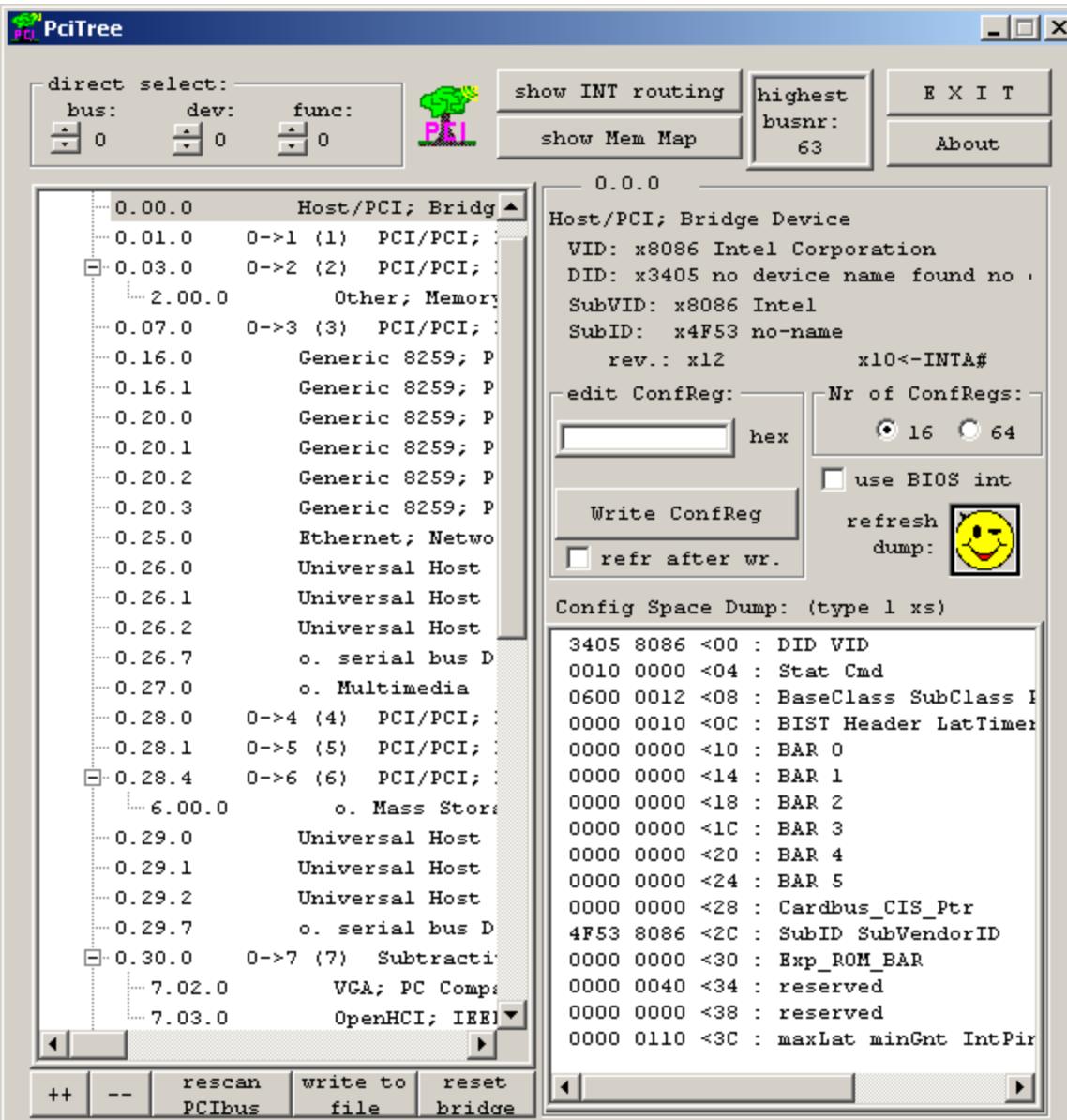
- Do not use the PCIe connector from the PC power supply



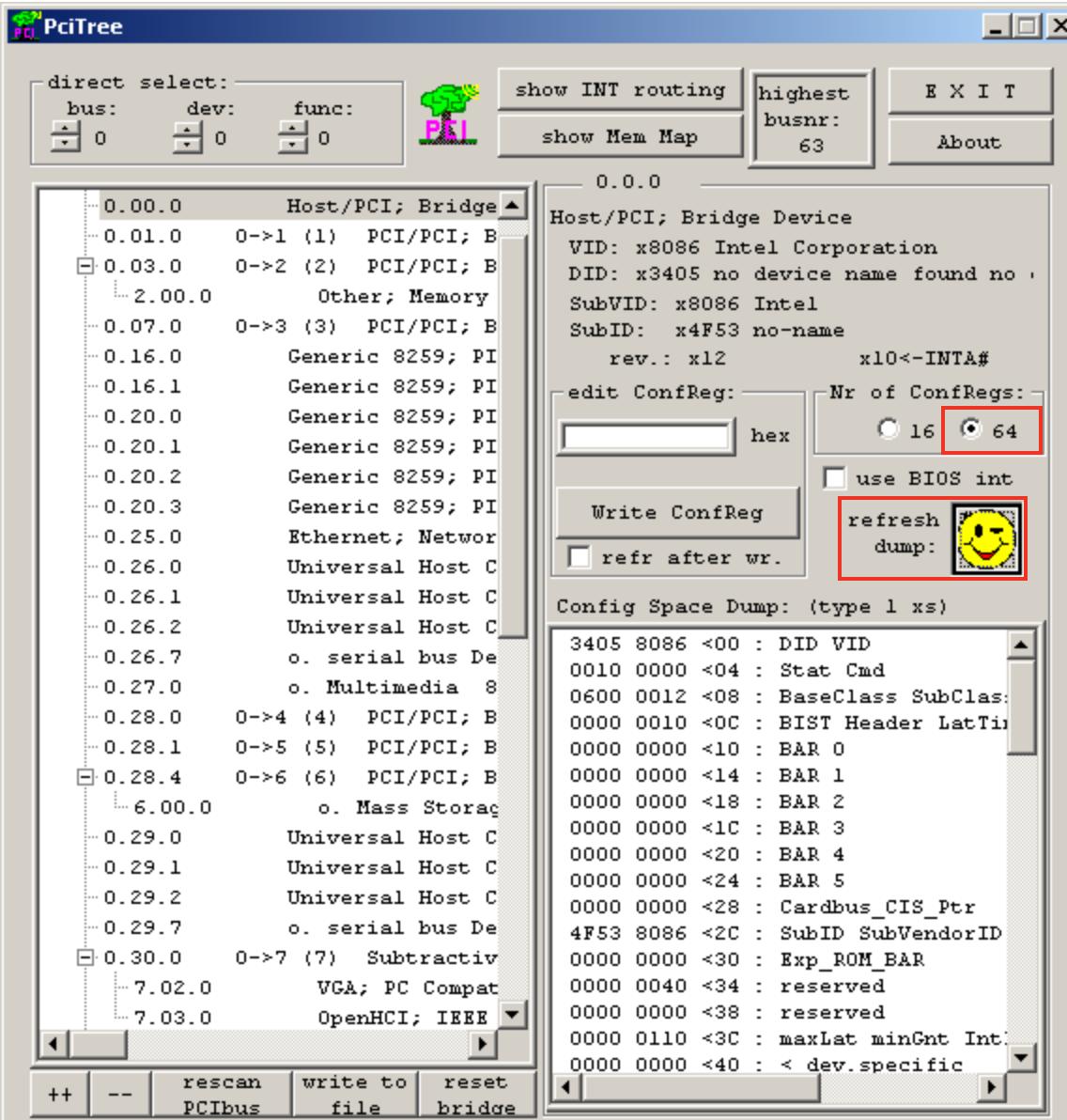
# Running the PCIe x4 Gen 2 Design

► Power on the PC

► Start PciTree



# Running the PCIe x4 Gen 2 Design

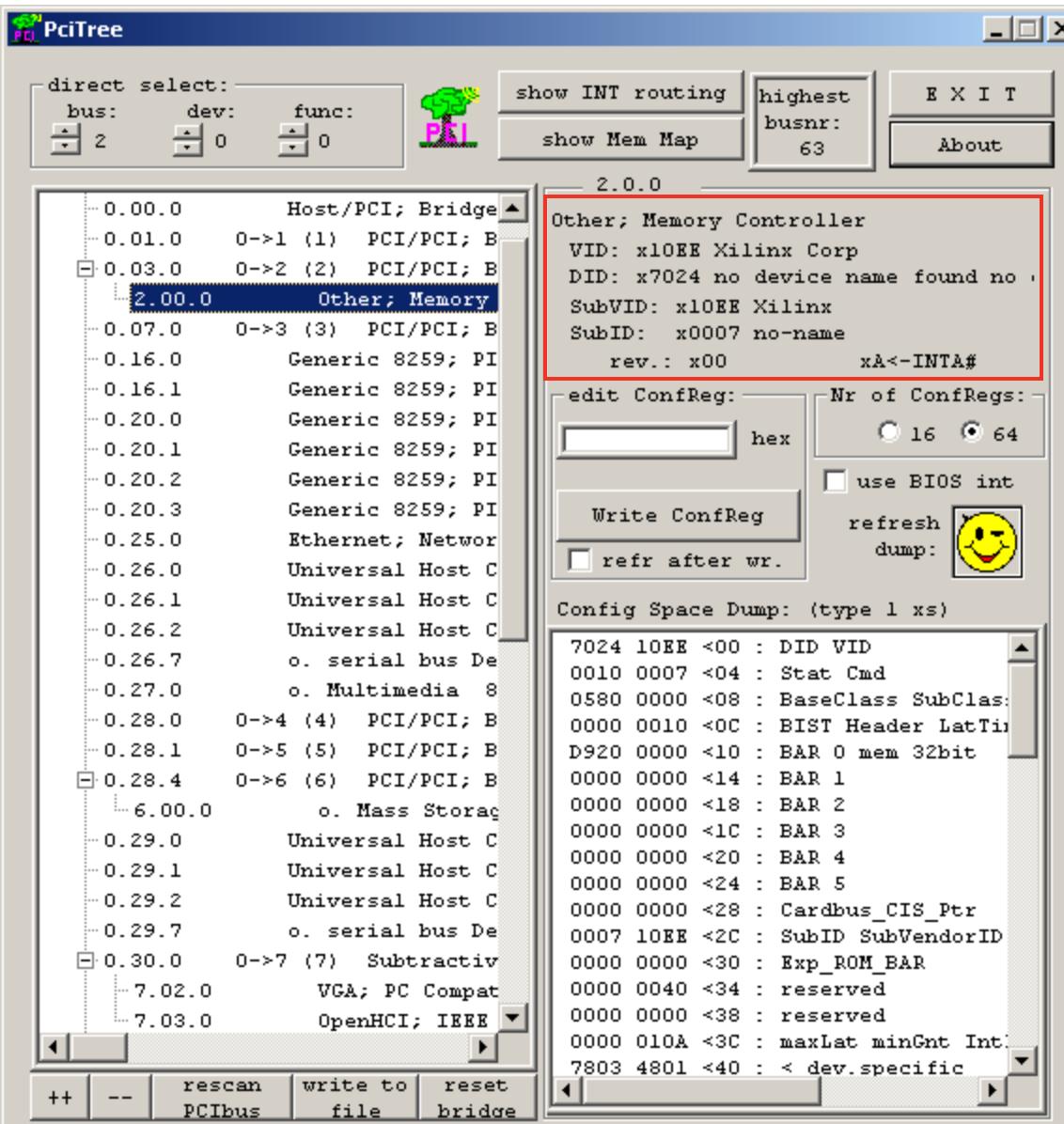


- Set Number of Configuration Registers to 64
- Click on Refresh dump

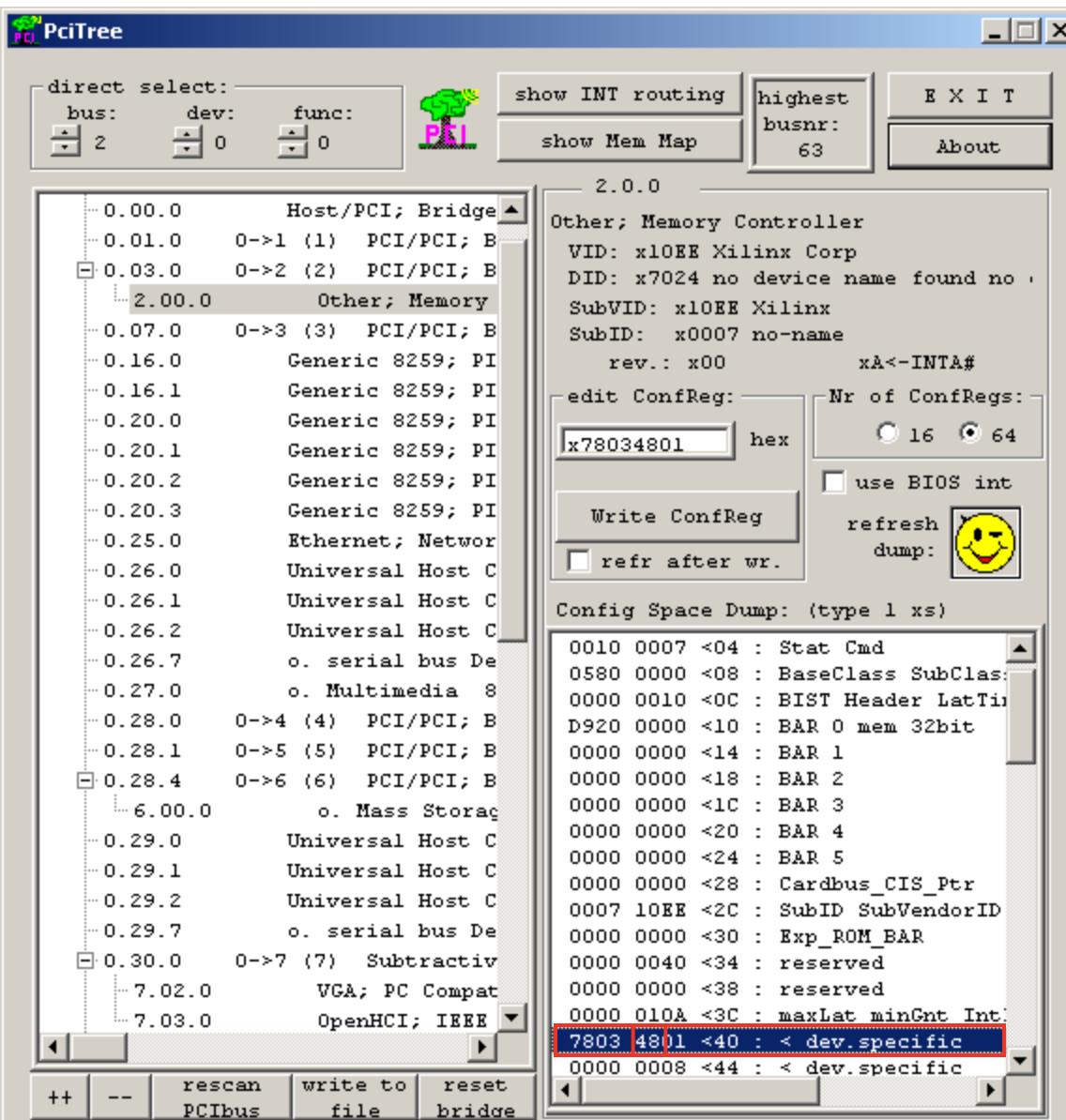
# Running the PCIe x4 Gen 2 Design

## ► Locate the Xilinx Device

- Vendor ID is 0x10EE
- The x4 Gen 2 configuration will have a Device ID of 0x7024



# Running the PCIe x4 Gen 2 Design



➤ Navigate the linked list in configuration space to locate the PCIe Capabilities Structure

- See [PG054](#) for details

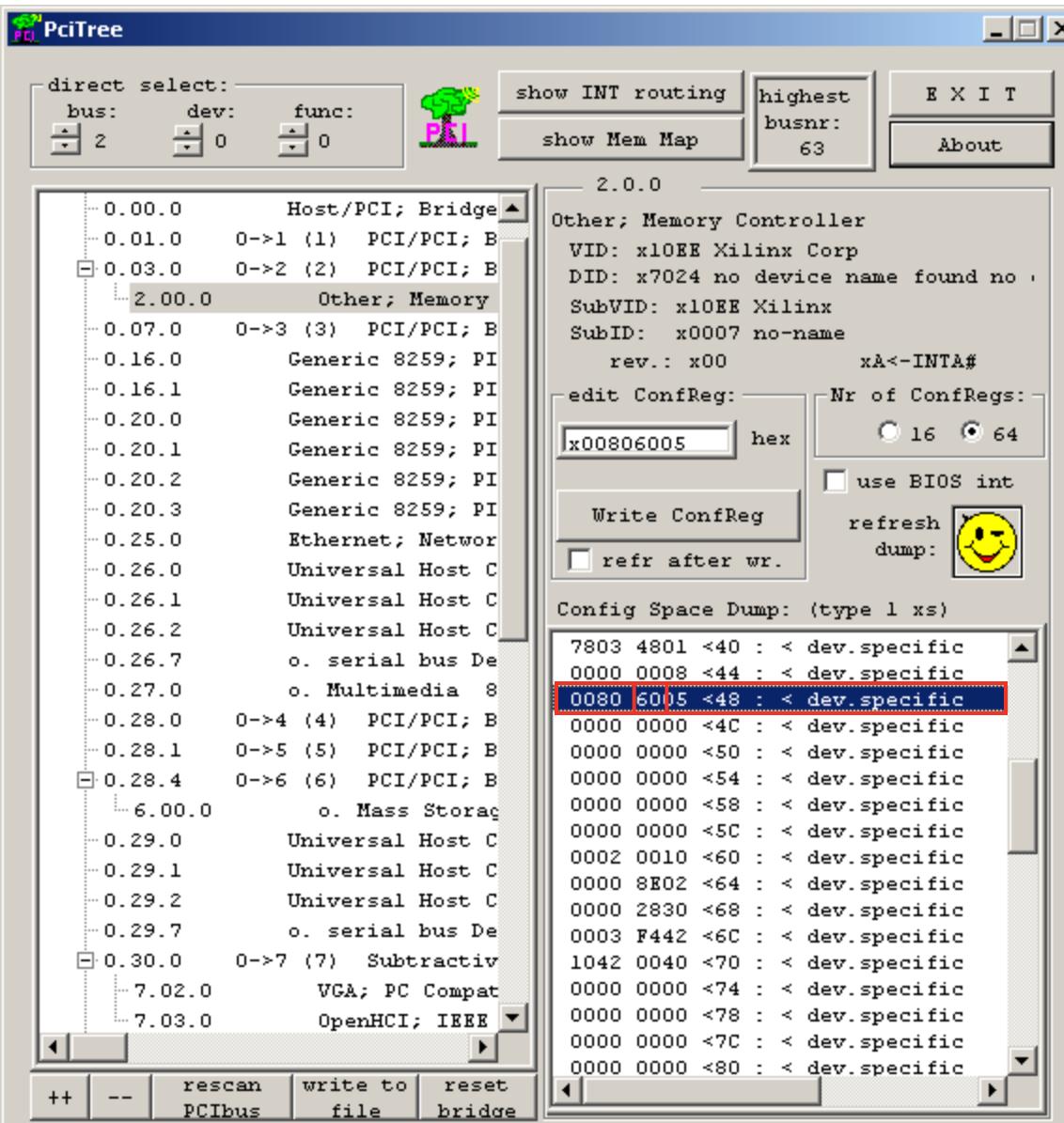
➤ With the Xilinx device selected, select Register 0x40

- Register 0x40 points to the next structure
- 0x48 is the address of the next structure

# Running the PCIe x4 Gen 2 Design

## ► Select Register 0x48

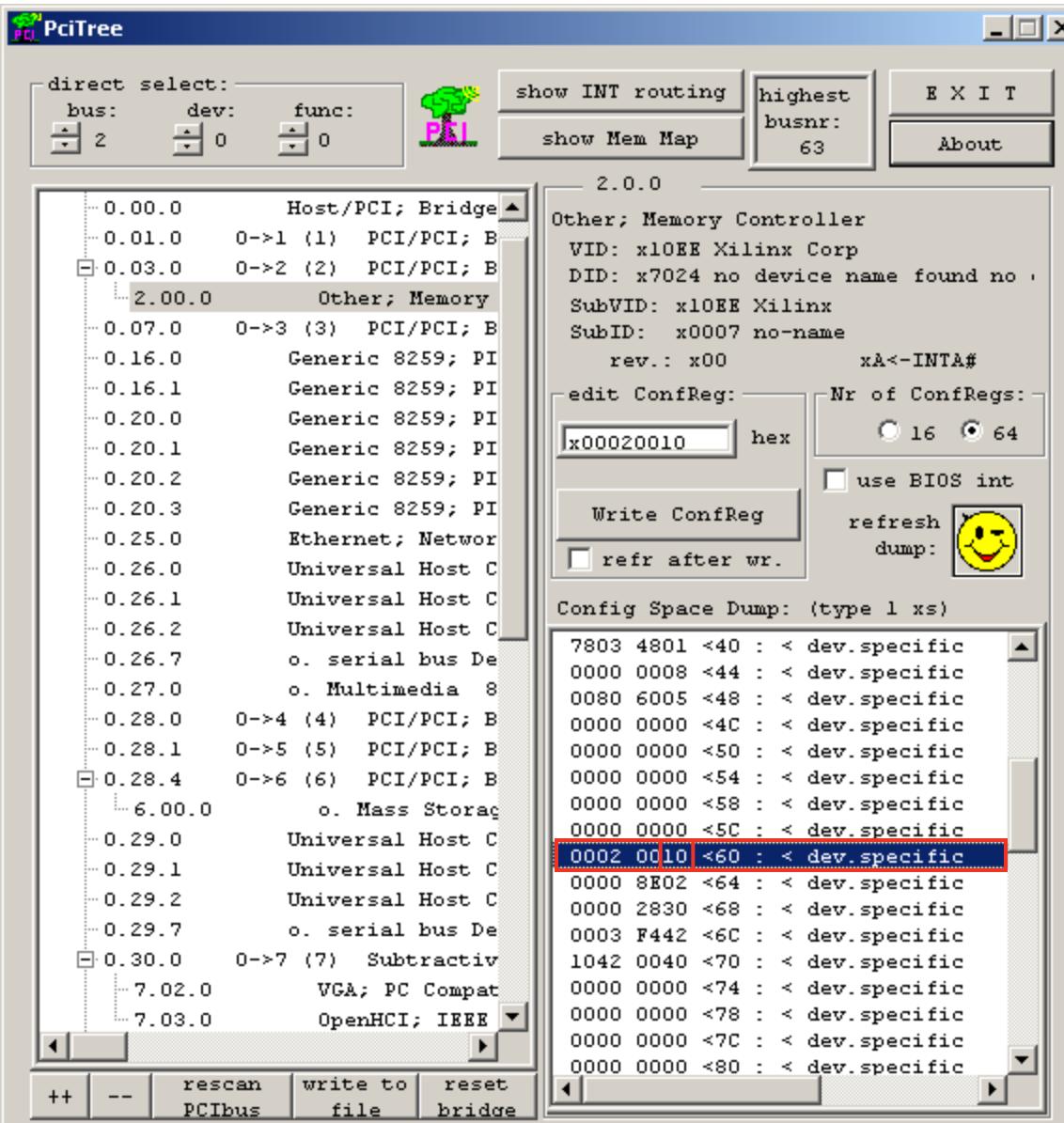
- Register 0x48 points to the next structure
- 0x60 is the address of the next structure



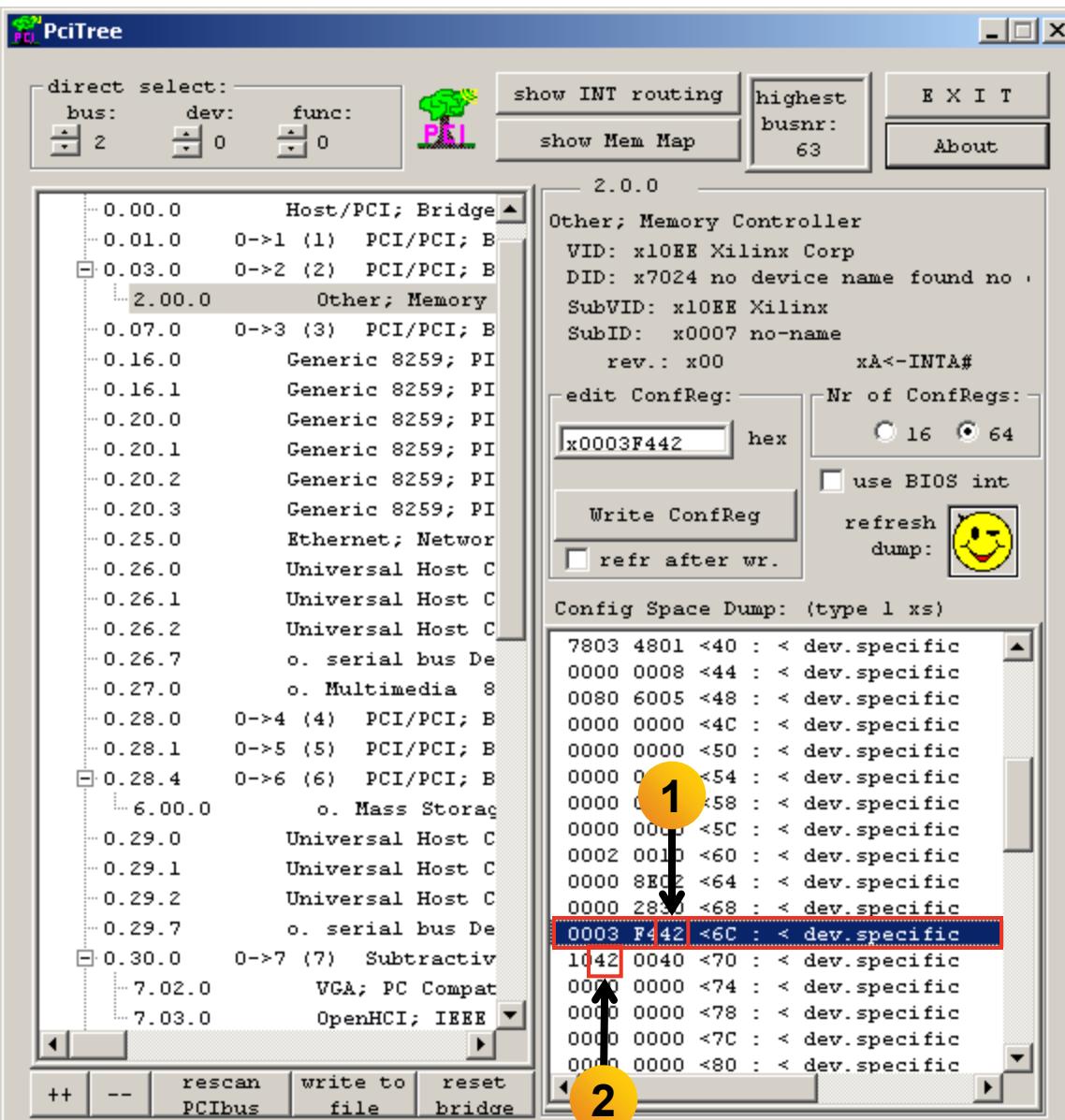
# Running the PCIe x4 Gen 2 Design

## ► Register 0x60

- 0x60 is a type 0x10, indicating PCIe Capabilities Structure
- Last Structure



# Running the PCIe x4 Gen 2 Design



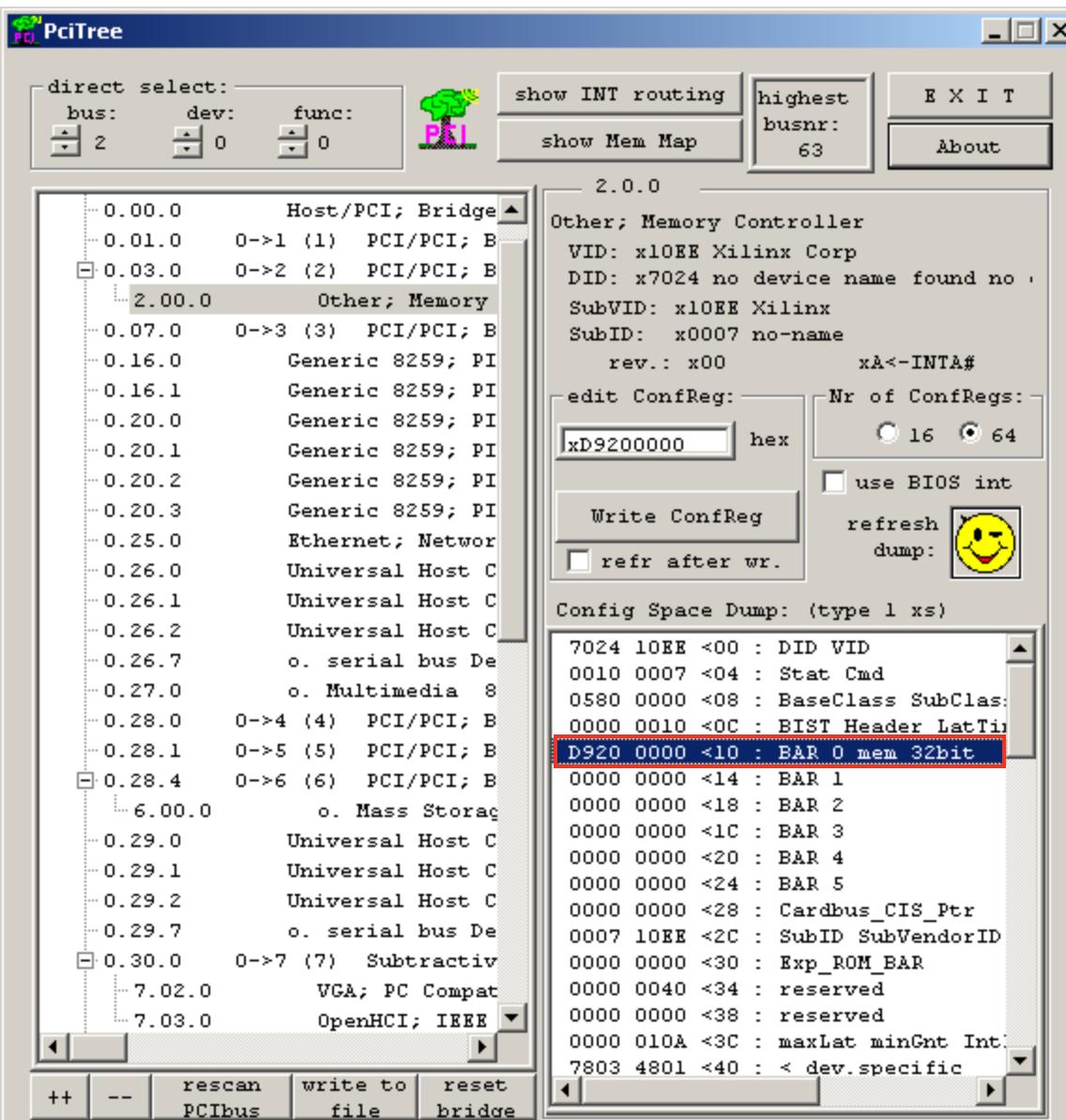
## ➤ Register 0x6C

- Link Capabilities Register
- Indicates the maximum number of lanes and speed (Gen 1, Gen 2) for device
- The value 0x42 shows this is an x4 Gen 2 device (1)

## ➤ Link Status Register

- 0x70
- Shows the current link status
- This design, in a Gen 2 chassis, trained to x4 Gen 2 (2)

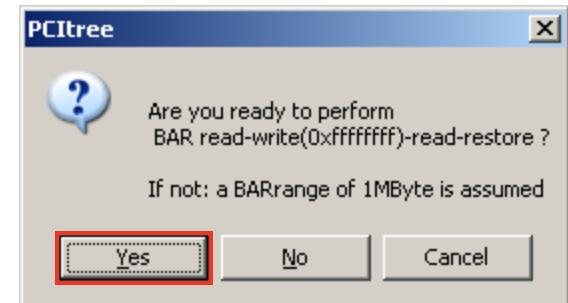
# Running the PCIe x4 Gen 2 Design



## ► Double-click on BAR 0

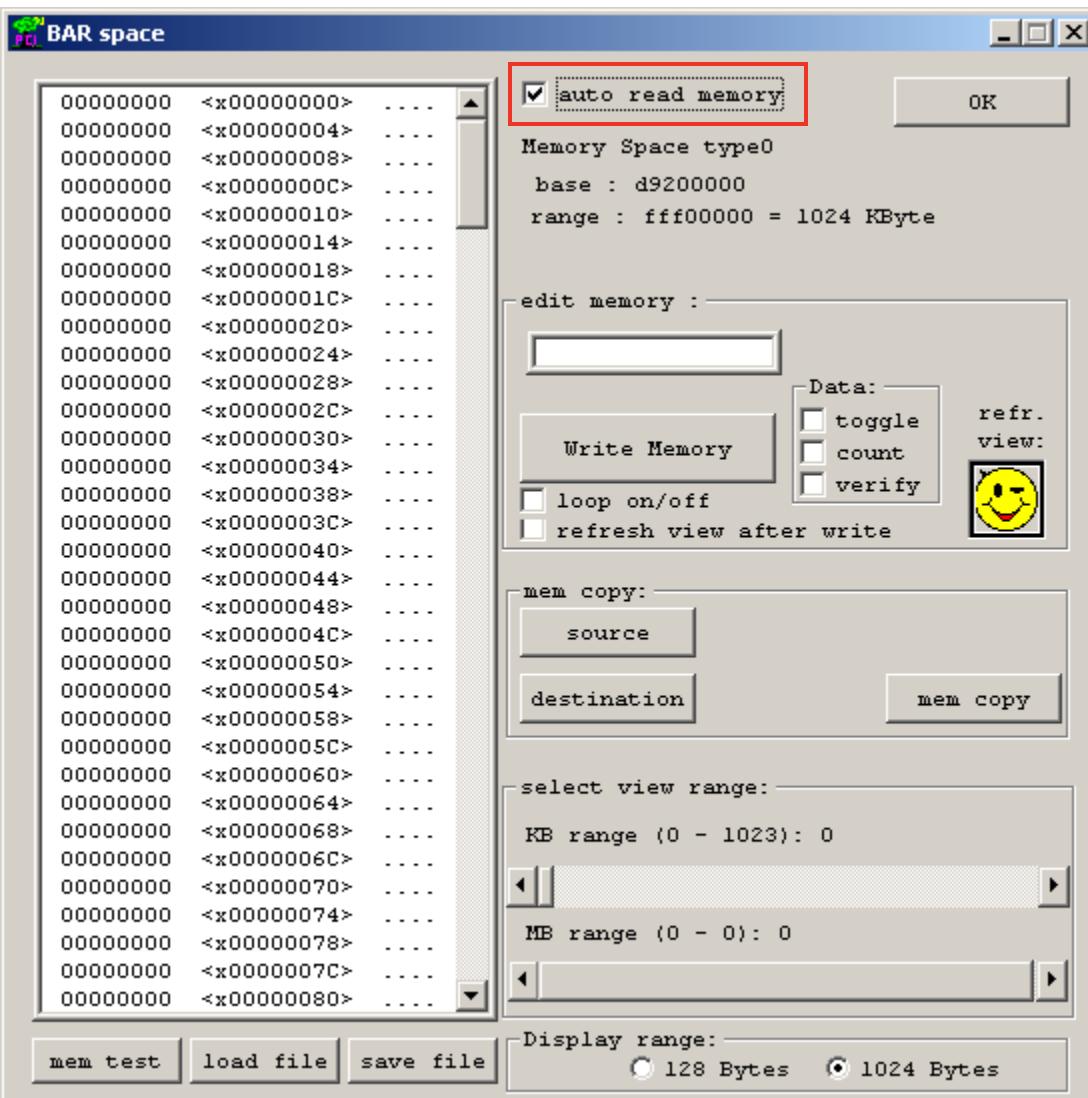
- BAR 0 Address is machine dependent

## ► Click Yes on the Dialog box seen below



# Running the PCIe x4 Gen 2 Design

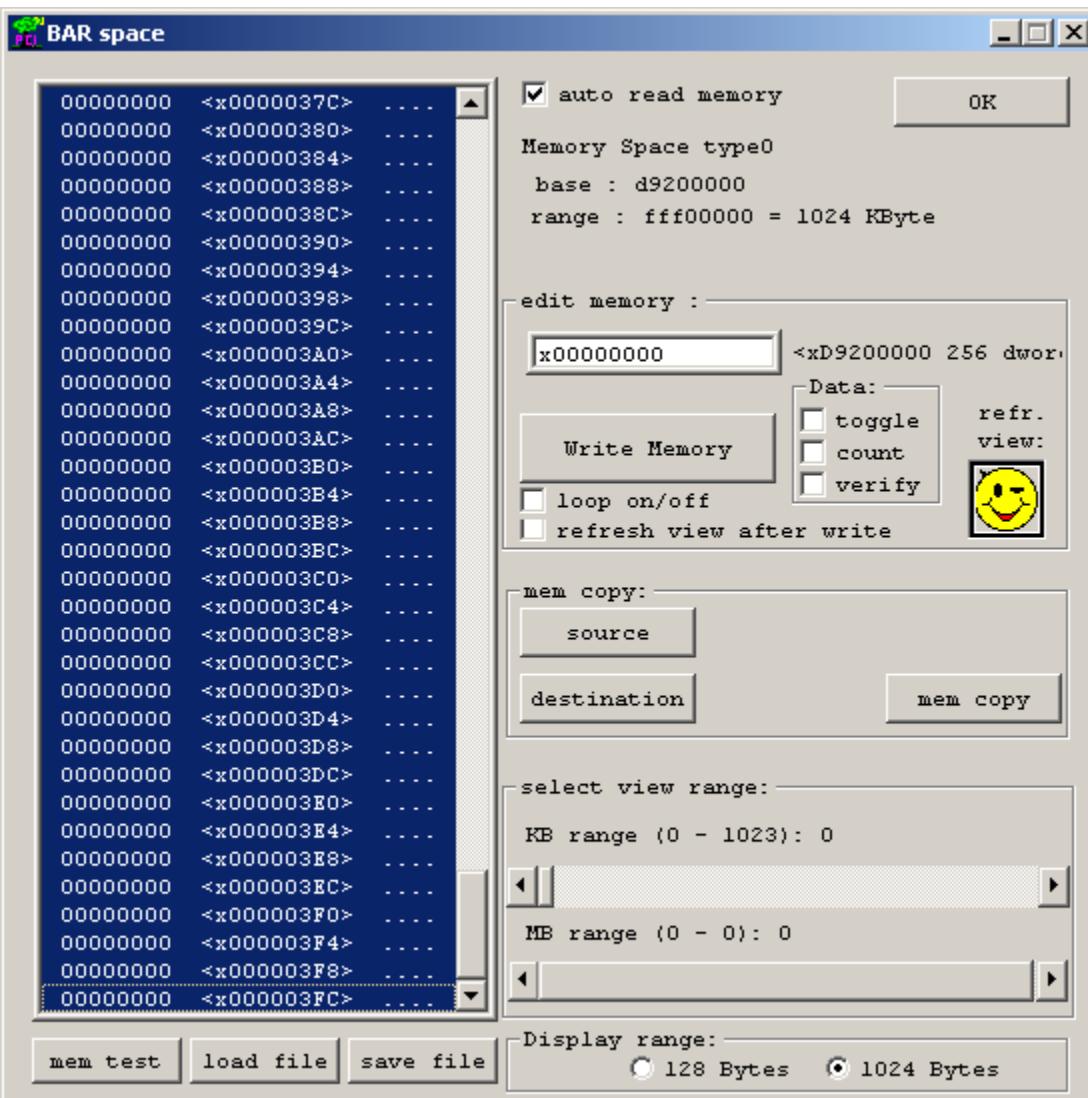
► Select auto read memory



# Running the PCIe x4 Gen 2 Design

► Click on the first memory location

- Type <Shift-End> to select 1024 Bytes

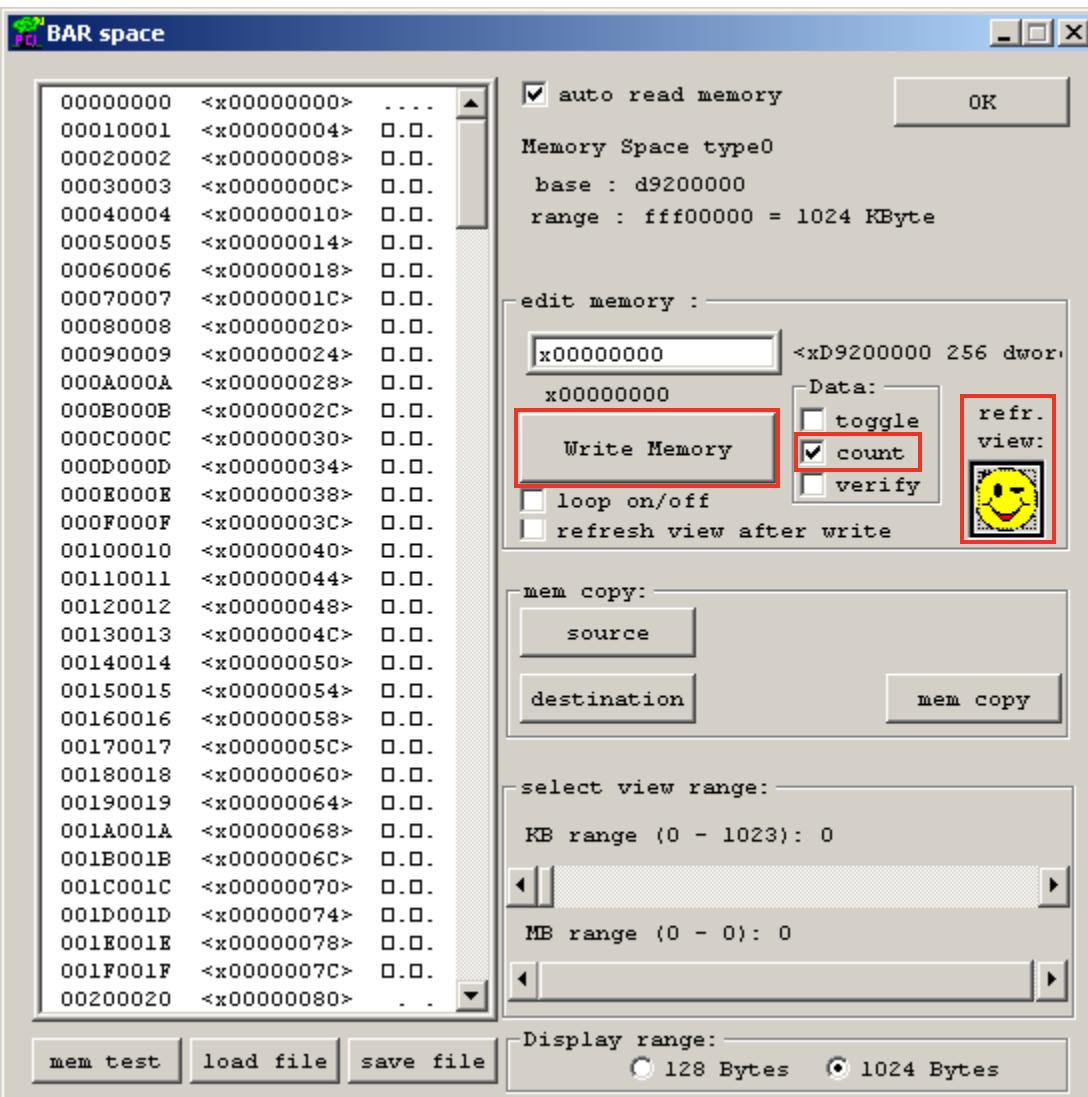


# Running the PCIe x4 Gen 2 Design

## ➤ Write Memory

- Select count
- Click Write Memory
- Click refr view

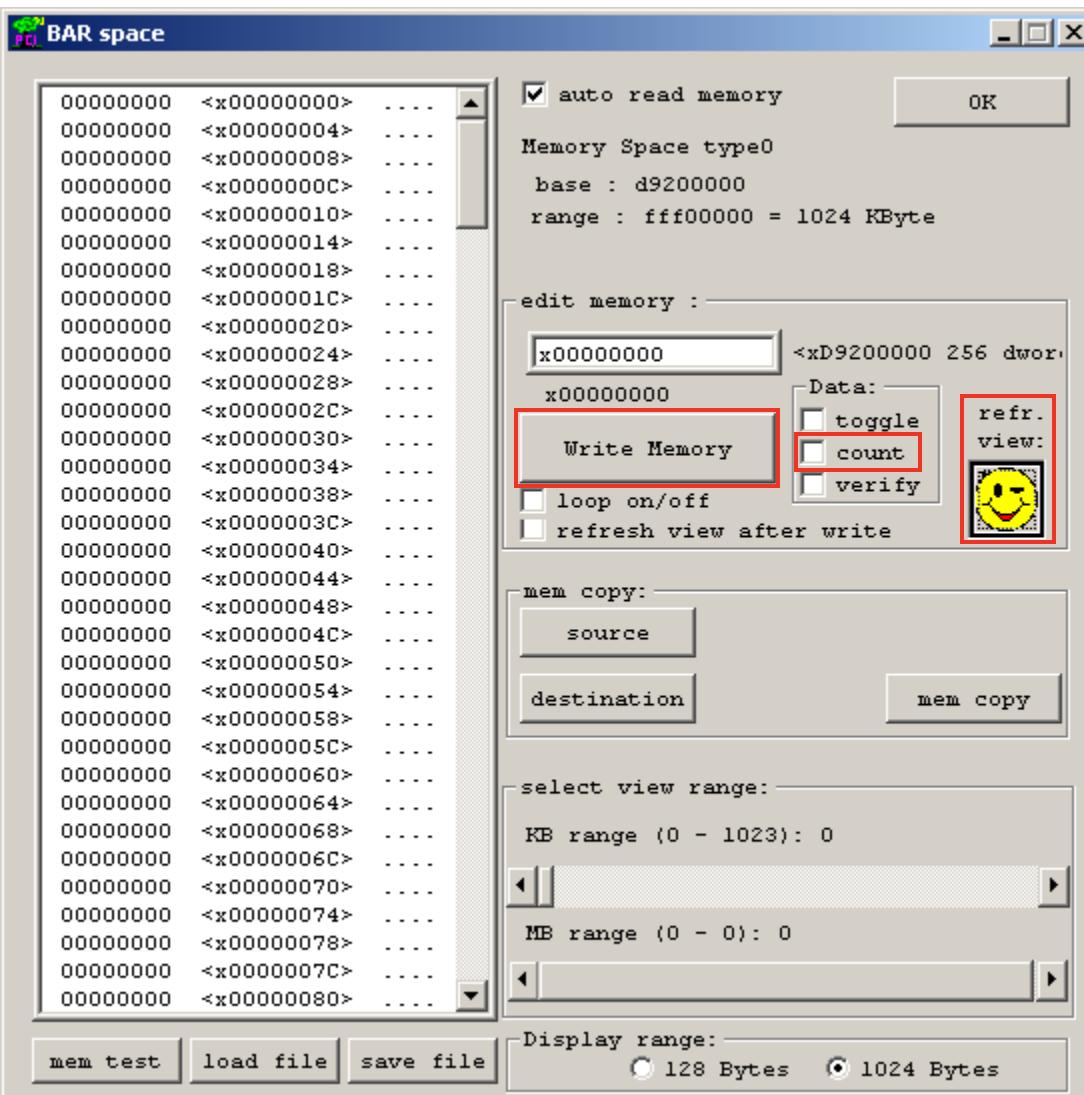
## ➤ View results – counting up to FF



Note: Presentation applies to the AC701

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# Running the PCIe x4 Gen 2 Design



## ➤ Restore Memory

- Deselect count
- Click Write Memory
- Click refr view

## ➤ Memory is reset to zeros

## ➤ Turn off PCIe chassis and remove AC701 board

## References

# References

## ► PCIe Base Specification

- PCI SIG Web Site
  - <http://www.pcisig.com/home>

## ► Xilinx PCI Express

- Xilinx PCI Express Overview
  - <http://www.xilinx.com/products/technology/pci-express.html>
- 7 Series Integrated Block for PCI Express Product Page
  - [http://www.xilinx.com/products/intellectual-property/7\\_series\\_pci\\_express\\_block.html](http://www.xilinx.com/products/intellectual-property/7_series_pci_express_block.html)
- 7 Series Integrated Block for PCI Express Product Guide – PG054
  - [http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_7x/v3\\_1/pg054-7series-pcie.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_7x/v3_1/pg054-7series-pcie.pdf)
- 7 Series Integrated Block for PCI Express – Release Notes
  - <http://www.xilinx.com/support/answers/54643.htm>

# References

## ► Micron NOR Flash

- Micron N25Q256 Flash
  - <http://www.micron.com/partsnor-flash/serial-nor-flash/n25q256a13esf40g>
- Datasheet
  - [http://www.micron.com/~media/Documents/Products/Data%20Sheet/NOR%20Flash/Serial%20NOR/N25Q/n25q\\_256mb\\_3v\\_65nm.pdf](http://www.micron.com/~media/Documents/Products/Data%20Sheet/NOR%20Flash/Serial%20NOR/N25Q/n25q_256mb_3v_65nm.pdf)

## ► Xilinx Generation 7 Configuration with SPI Flash

- 7 Series FPGAs Configuration User Guide – UG470
  - [http://www.xilinx.com/support/documentation/user\\_guides/ug470\\_7Series\\_Config.pdf](http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf)
- Vivado Design Suite Programming and Debugging User Guide – UG908
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2015\\_1/ug908-vivado-programming-debugging.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug908-vivado-programming-debugging.pdf)
- Using SPI Flash with 7 Series FPGAs – XAPP586
  - [http://www.xilinx.com/support/documentation/application\\_notes/xapp586-spi-flash.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp586-spi-flash.pdf)

# Documentation

# Documentation

## ➤ Artix-7

- Artix-7 FPGA Family
  - <http://www.xilinx.com/products/silicon-devices/fpga/artix-7/index.htm>
- Design Advisory Master Answer Record for Artix-7 FPGAs
  - <http://www.xilinx.com/support/answers/51456.htm>

## ➤ AC701 Documentation

- Artix-7 FPGA AC701 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html>
- AC701 Getting Started Guide – UG967
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ac701/2014\\_3/ug967-ac701-eval-kit-getting-started.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ac701/2014_3/ug967-ac701-eval-kit-getting-started.pdf)
- AC701 User Guide – UG952
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ac701/ug952-ac701-a7-eval-bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ac701/ug952-ac701-a7-eval-bd.pdf)