DESIGN OF CURRENT MIRROR BASED TWO STAGE CMOS CASCODE OP-AMP FOR HIGH FREQUENCY APPLICATION

A Mini project

Submitted in partial fulfilment of the requirements for the award of the degree

Of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

By

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the project entitled "design of current mirror based two stage cmos cascode op-amp for high frequency application" being submitted by

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in the partial fulfilment for the award of the degree of bachelor of technology in Electronics and Communication Engineering to the Jawaharlal Nehru Technological University, Hyderabad. This is a record of bonafide work carried out under my guidance and supervision. The results embodied in this project report have not been submitted to any other university or institute for the award of any degree or diploma.

Mrs. NEETU SRIVATSAVA	**Dr. S.SATHEES KUMARAN**
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ACKNOWLEDGEMENT

This project is an acknowledgement to the inspiration, drive and technical assistance contributed by many individuals. This project would have never seen light of this day without the help and guidance we have received. We would like to express our gratitude to all the people behind the screen who helped us to transform an idea into a real application.

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DECLARATION

We hereby declare that the result embodied in this project report entitled "**Design of current mirror based two stage CMOS cascode op-amp for high frequency application using Cadence**" is carried out by us during the year 2018-2019 for the partial fulfilment of the award of **Bachelor of Technology in Electronics and Communication Engineering**, from **ANURAG GROUP OF INSTITUTION** (formerly CVSR college of Engineering). We have not submitted this project report to any other Universities / Institute for the award of any degree.

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ABSTRACT:

This project mainly focuses on high slew rate, Moderate gain, Ultra wide band two stage CMOS cascode operational amplifier for “Radio Frequency” application. Current mirror based cascoding technique is mainly used to increase the gain characteristics of the circuit. We are going to implement on 180nm technology. This radio frequency integrated circuit (RFIC) is in high demand for VLSI High frequency application requires High speed Op-Amp. Unity gain bandwidth should be very high because our circuitry is going to be applied for Wireless Application.

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CHAPTER 1

INTRODUCTION

1.1 OVERVIEW OF THE THESIS

This project mainly focuses on high slew rate, Moderate gain, Ultra wide band two stage CMOS cascode operational amplifier for “Radio Frequency” application. Current mirror based cascoding technique is mainly used to increase the gain characteristics of the circuit. We are going to implement on 180nm technology. This radio frequency integrated circuit (RFIC) is in high demand for VLSI High frequency application requires High speed Op-Amp. Unity gain bandwidth should be very high because our circuitry is going to be applied for Wireless Application.

1.2 OBJECTIVES

- This radio frequency integrated circuit (RFIC) is in high demand for VLSI High frequency application requires High speed Op-Amp.
- Unity gain bandwidth should be very high because our circuitry is going to be applied for Wireless Application.

1.3 INTRODUCTION TO ELECTRONIC DEVICES AND CIRCUITS

1.3.1 Types of Transistors

Transistor is a semiconductor device which is used to amplify the signals as well as in switching circuits. Generally transistor is made of solid material which contains three terminals such as emitter (E), Base (B) and Collector (C) for connections with other components in the circuit. Some transistors contains fourth terminal also i.e. substrate (S). Transistor is one of the active components.

From the time of first transistor invention to present days the transistors are classified into different types depending on either construction or operation, they are explained using tree diagram as below.

1.3.2 Transistor Tree Diagram

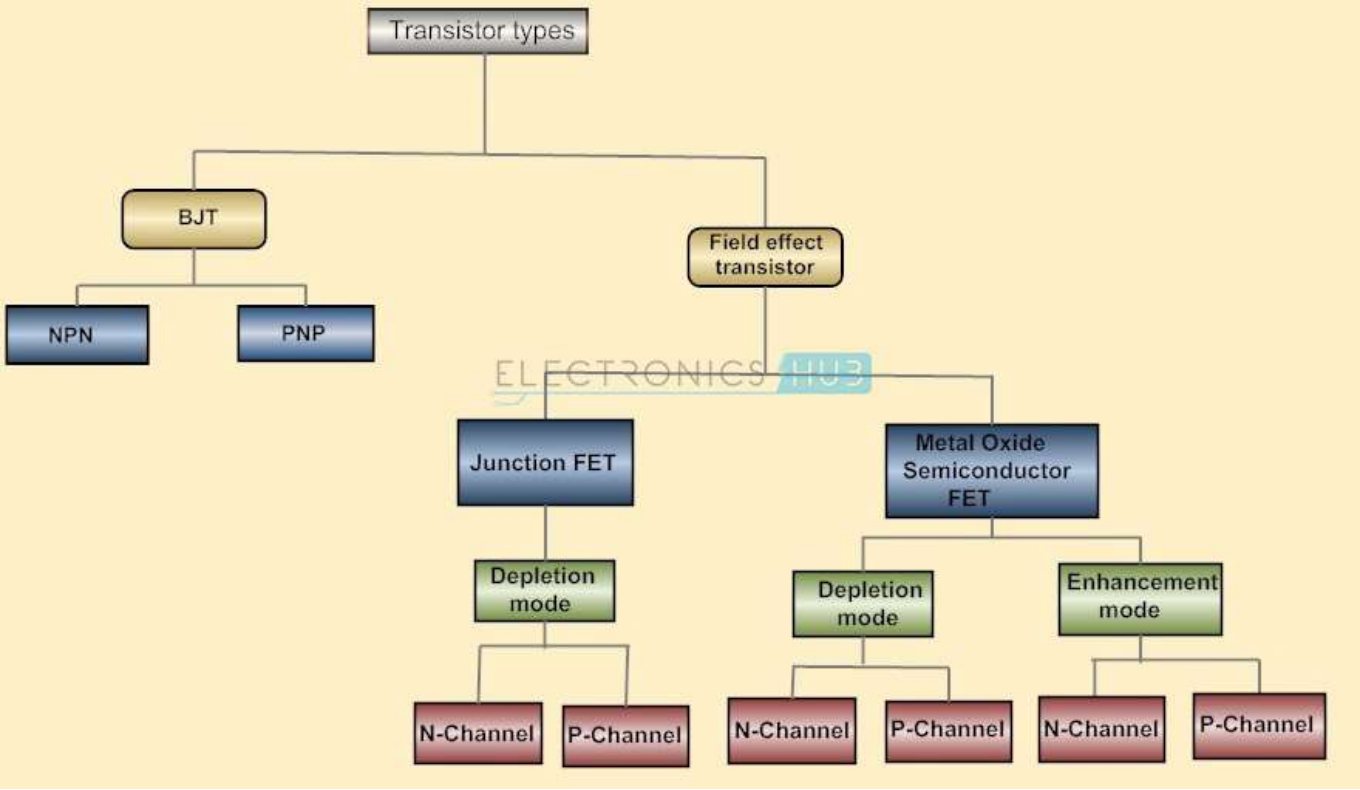


Fig 1

The transistors classification can be understood by observing the above tree diagram. Transistors are basically classified into two types; they are Bipolar Junction Transistors (BJT) and Field

Effect Transistors (FET). The BJTs are again classified into NPN and PNP transistors. The FET transistors are classified into JFET and MOSFET.

Junction FET transistors are classified into N-channel JFET and P-channel JFET depending on their function. MOSFET transistors are classified into Depletion mode and Enhancement mode. Again depletion and enhancement mode transistors are classified into N-channel JFET and P-channel.

Nowadays, the vacuum tubes are replaced with transistors because the transistors have more benefits over vacuum tubes. Transistors are small in size and it requires low voltage for operation and also it has low power dissipation. Due to these reasons the transistor is used in many applications such as amplifiers, switching circuits, oscillators and also in almost all electronic circuits.

MOSFET has several advantages over BJT

- The BJT is a bipolar junction transistor whereas MOSFET is a metal oxide semiconductor field effect transistor.
- A BJT has three terminals namely base, emitter and collector, while a MOSFET has three terminals namely source, drain and gate.
- BJT's are used for low current applications, whereas MOSFET is used for high power applications.
- Nowadays, in analog and digital circuits, MOSFETs are treated to be more commonly used than BJTS.
- The working of BJT depends on the current at the base terminal and the working of the MOSFET depends on the voltage at the oxide insulated gate electrode.
- The BJT is a current controlled device and MOSFET is a voltage controlled device. MOSFETs are used more than BJTs in most of the applications
- The structure of the MOSFET is more complex than BJT.

1.3.3 History of MOSFET

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices. The MOSFET is a core of integrated circuit and it can be designed and fabricated in a single chip because of these very small sizes. The MOSFET is a four terminal device with source(S), gate (G), drain (D) and body (B) terminals. The body of the MOSFET is frequently connected to the source terminal so making it a three terminal device like field effect

transistor. The MOSFET is very far the most common transistor and can be used in both analog and digital circuits.

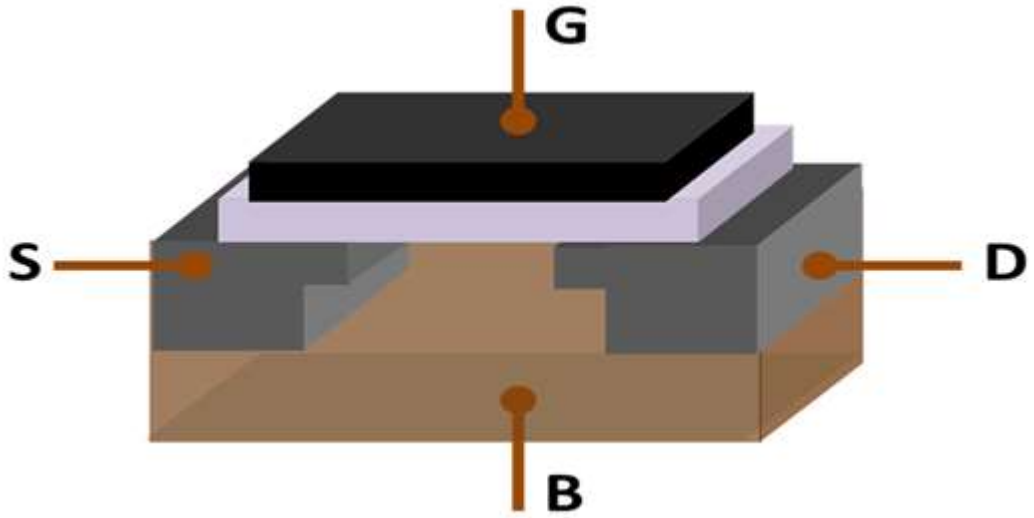


Fig 1.1

The MOSFET works by electronically varying the width of a channel along which charge carriers flow (electrons or holes). The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide. The MOS capacity present in the device is the main part.

From this we can observe that the cascade topology improves the gain of the amplifier. This is mainly because the small input signal is first amplified by CS stage and the amplified output signal of CS stage is further amplified by the CG stage. Further the cascade stage also has the high output impedance.

These transistors are available in 4 different types such as P-channel or N-channel with either in enhancement mode or depletion mode. The source and Drain terminals are made of N-type semiconductor for N-channel MOSFETs and equally for P-channel devices. The gate terminal is made of metal and detached from source & drain terminals using a metal oxide. This insulation roots low power consumption & it is a benefit in this transistor. Therefore, this transistor is used where p and n channel MOSFETs are used as building blocks to reduce the power consumption like digital CMOS logic.

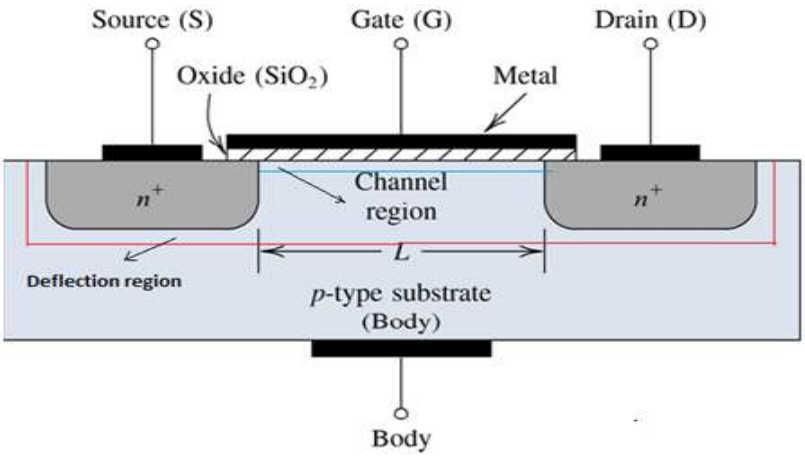
MOSFETs are classified into two types such as enhancement mode and depletion mode

Depletion Mode: When the voltage on the 'G'-terminal is low, then the channel shows its max conductance. As the voltage on the 'G'-terminal is positive or negative, then channel conductivity will be decreased.

Enhancement Mode: When the voltage on the 'G'-terminal is low, then the device does not conduct. When the more voltage is applied to the gate terminal, then the conductivity of this device is good.

1.3.4 Working Principle of MOSFET:

The working of MOSFET depends upon the MOS (metal oxide capacitor) which is the essential part of the MOSFET. The oxide layer presents, among the two terminals such as source and drain. By applying positive or negative gate voltages, we can set from p-type to n-type. When positive voltage is applied to the gate terminal, then the holes existing under the oxide layer with a repulsive force and holes are pushed down through the substrate. The deflection region occupied by the bound negative charges which are associated with the acceptor atoms.



Working Principle of MOSFET

Fig 1.2

CHAPTER 2

IMPORTANT CIRCUIT ELEMENTS

2.1 Current Mirror

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being "copied" can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. Or it can consist of a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits. It can also be used to model a more realistic current source (since ideal current sources don't exist).

Current mirrors are basically used for,

1. **Biasing:** Transistors functioning as linear amplifiers need to be biased such that they are operating in a desirable portion of their transfer characteristic. The best way to do this in the context of IC design is to cause a predetermined current to flow through the transistor's drain (for MOSFETs) or collector (for BJTs). This predetermined current needs to be stable and independent of the voltage across the current-source component. Of course, no real circuit will ever be perfectly stable or perfectly immune to changes in voltage, but as is usually the case in engineering, perfection is not quite necessary.

2. **Active loads:** In amplifier circuits, current sources can be used instead of collector/drain resistors. These "active loads" provide higher voltage gain and allow the circuit to function properly with lower supply voltage. Also, IC manufacturing technology favours transistors over resistors.

2.1.1 Working Of Current Mirror

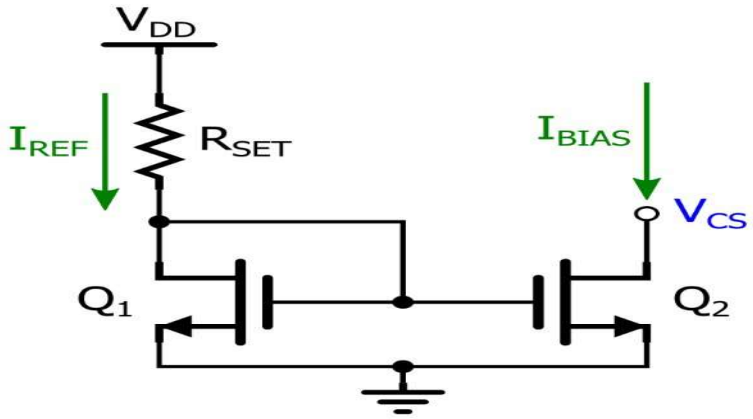


Fig 2

As you can see, the drain of Q_1 is shorted to its gate. This means that $V_G = V_D$, and thus $V_{GD} = 0V$. So, is Q_1 in cutoff, the triode region, or the saturation region? It can't be in cutoff, because if no current were flowing through the channel, the gate voltage would be at V_{DD}, and thus V_{GS} would be greater than the threshold voltage V_{TH} (we can safely assume that V_{DD} is higher than V_{TH}). This means Q_1 will always be in saturation (also referred to as "active" mode), because $V_{GD} = 0$ V, and one way of expressing the condition for MOSFET saturation is that V_{GD} must be less than V_{TH}.

If we recall that no steady-state current flows into the gate of a MOSFET, we can see that the reference current I_{REF} will be the same as Q_1's drain current. We can customize this reference current by choosing an appropriate value for R_{SET}. So what does all this have to do with Q_2? Well, the drain current of a MOSFET in saturation is influenced by the width-to-length ratio of the channel and the gate-to-source voltage.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

At this point we are ignoring channel-length modulation; consequently, as indicated by the equation, the drain current is not affected by the drain-to-source voltage. Now notice that both FETs have their sources tied to ground and that their gates are shorted together—in other words, both have the same gate-to-source voltage. Thus, if we assume that both devices have the same channel dimensions, their drain currents will be equal, regardless of the voltage at the drain of Q_2. This voltage is labeled V_{CS}, meaning the voltage across the current-source component; this helps to remind us that Q_2, like any well-behaved current source, generates a bias current that is not affected by the voltage across its terminals. Another way to say this is that Q_2 has infinite output resistance.

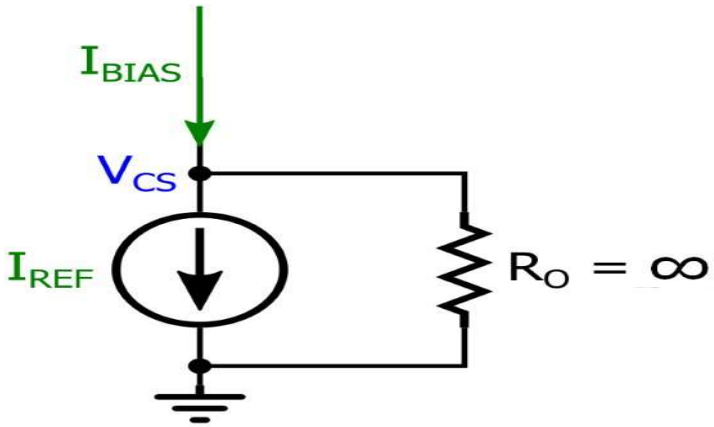


Fig 2.1

Under these conditions, no current ever flows through the output resistance R_O, even when V_{CS} is very high. This means that the bias current is always exactly equal to the reference current.

A common name for this circuit is a "current mirror." You can probably see why the current generated by the right-hand transistor mirrors (i.e., is similar to) the reference current flowing through the left-hand transistor.

2.1.2 The Importance of the Transistor Staying in Saturation

The first major affront to the idealized analysis of this circuit is the fact that everything falls apart when the transistor is not in saturation. If Q_2 is in the triode (AKA linear) region, the drain current will be highly dependent on V_{DS}. In other words, we no longer have a current source because the bias current is affected by V_{CS}. We know that Q_2's gate-to-drain voltage must be less than the threshold voltage to maintain saturation.

Another way to say this is that Q_2 will leave the saturation region when the drain voltage becomes V_{TH} volts lower than the gate voltage. We can't put a precise number on this because both the gate voltage and the threshold voltage will vary from one implementation to another.

A reasonable example is the following: The gate voltage required to generate the desired bias current is around 0.9 V, and the threshold voltage is 0.6 V; this means we can maintain saturation as long as V_{CS} stays above ~0.3 V.

2.1.3 Channel-Length Modulation

Unfortunately, even when our overall circuit design ensures that Q_2 will always be in saturation, our MOSFET current source is not exactly ideal. The culprit is channel-length modulation.

The essence of the saturation region is the "pinched-off" channel that exists when the gate-to-drain voltage does not exceed the threshold voltage.

Fig 2.2

The idea is that drain current becomes independent of V_{DS} after the channel is pinched off because further increases in drain voltage do not affect the shape of the channel. In reality, though, increases in V_{DS} cause the "pinch-off point" to move toward the source, and this allows the drain voltage to have a small effect on the drain current even when the FET is in saturation. The result can be represented as follows:

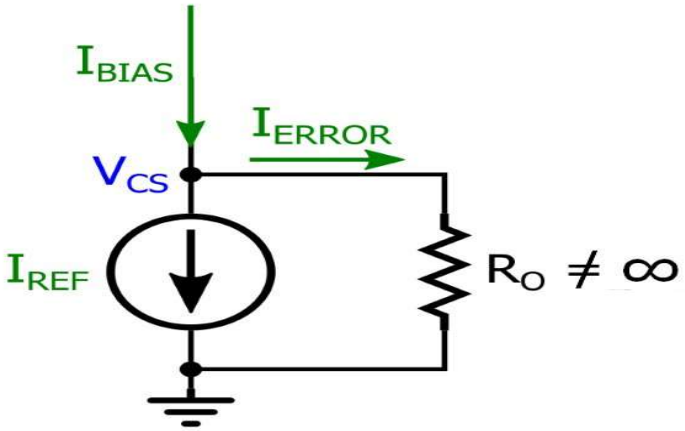


Fig 2.3

I_{BIAS} is now the sum of I_{REF} (determined by R_{SET}) and I_{ERROR} (the current flowing through the output resistance). I_{ERROR} obeys the simple Ohm's law relationship: higher V_{CS} means more I_{ERROR} and consequently more I_{BIAS}, and thus the current source is no longer independent of the voltage across its terminals.

2.1.4 Adjusting and Steering

This handy current-source circuit becomes even better when you realize how flexible it is. First let's look at adjusting the current generated by Q_2. So far we've assumed that the generated current is the same as the reference current, but this is true only when the transistors have the same channel-width-to-channel-length ratio. Remember the equation for saturation-mode drain current:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Drain current is directly proportional to the width-to-length ratio, and thus we can increase or decrease I_{BIAS} simply by making Q_2's W/L ratio higher than or lower than that of Q_1. For example, if we want the bias current to be two times larger than the reference current, all we need to do is keep the channel lengths the same and increase Q_2's channel width by a factor of two. (This may not seem so easy if you're used to working with discrete FETs, but specifying channel dimensions is standard practice in IC design.)

It is also quite straightforward to use this circuit for "current steering." The following diagram illustrates the current-steering concept:

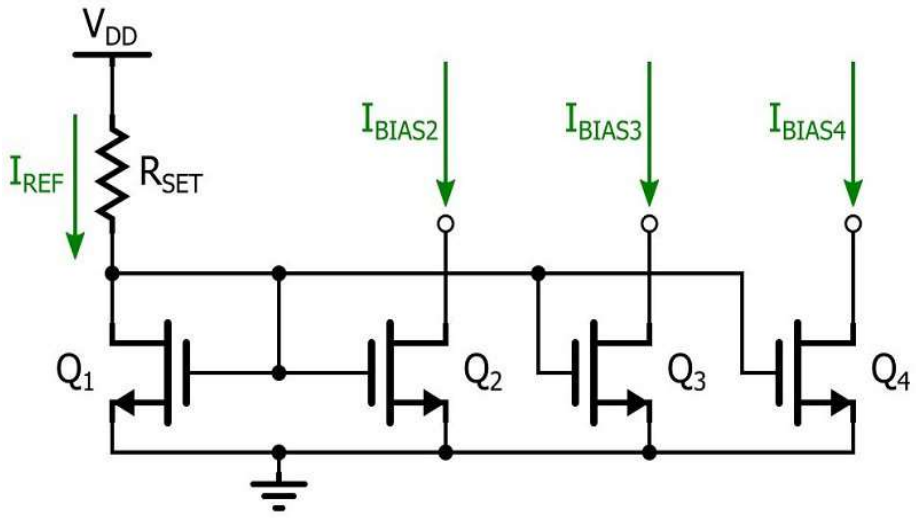


Fig 2.4

This clever arrangement allows us to generate multiple bias currents from one reference current. Even better, each of these currents can be different. They can be individually modified simply by adjusting the width-to-length ratios.

2.1.5 Breif summary of Current Mirror

We've covered the operation and capabilities of the basic MOSFET constant-current source, and we also discussed limitations. As implied by the adjective "basic," there are better circuits out there. But the basic circuit is a good place to start, because the two-transistor current mirror remains the conceptual core of the higher-performance topologies.

2.2 Cascode Technique

Cascode amplifier is a two stage circuit consisting of a transconductance amplifier followed by a buffer amplifier. The word "cascode" was originated from the phrase "cascade to cathode". This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher slew rate etc. The reason behind the increase in bandwidth is the reduction of Miller effect. Cascode amplifier is generally constructed using FET (field effect transistor) or BJT (bipolar junction transistor). One stage will be usually wired in common source/common emitter mode and the other stage will be wired in common base/common emitter mode.

2.2.1 Miller effect

Miller effect is actually the multiplication of the drain to source stray capacitance by the voltage gain. The drain to source stray capacitance always reduces the bandwidth and when it gets multiplied by the voltage gain the situation is made further worse. Multiplication of stray capacitance increases the effective input capacitance and as we know, for an amplifier, the increase in input capacitance increases the lower cut of frequency and that means reduced bandwidth. Miller effect can be reduced by adding a current buffer stage at the output of the amplifier or by adding a voltage buffer stage before the input.

2.2.2 MOSFET Cascode amplifier

The cascade of CS stage and CG stage is called as the cascode amplifier. Figure below shows the cascode amplifier circuit in which CS stage and CG stage cascaded.

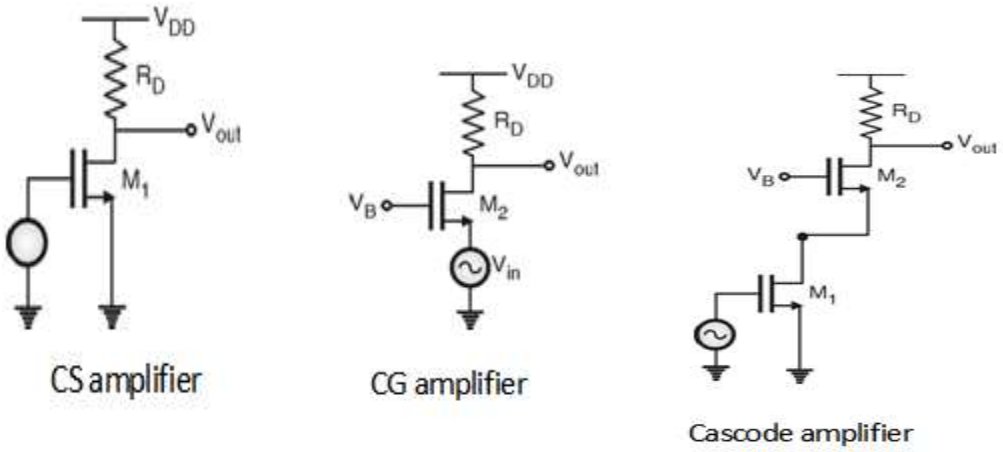


Fig 2.5

In cascode amplifier the output of CS amplifier is connected to the input of CG amplifier. Figure below shows the small signal equivalent circuit of the cascade amplifier.

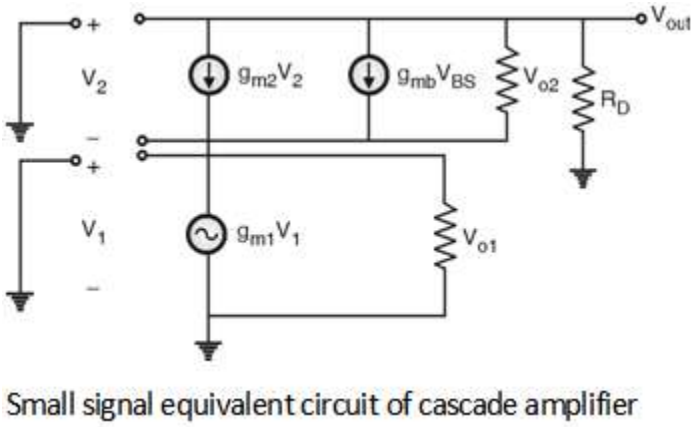


Fig 2.6

The voltage gain of the cascade amplifier is given by,

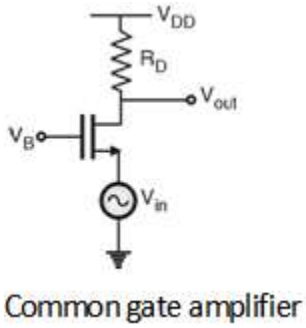
$A_v = = g_{m1} V_{o1} [(g_{m2} + g_{mb2}) V_{o2} + 1]$

From this we can observe that the cascade topology improves the gain of the amplifier. This is mainly because the small input signal is first amplified by CS stage and the amplified output signal of CS stage is further amplified by the CG stage. Further the cascade stage also has the high output impedance.

Common Gate Amplifier :

In common source amplifier and source follower circuits, the input signal is applied to the gate of a MOSFET. It is also possible to apply the input signal to the source terminal by keeping common gate terminal. This type of amplifier is called as common gate amplifier.

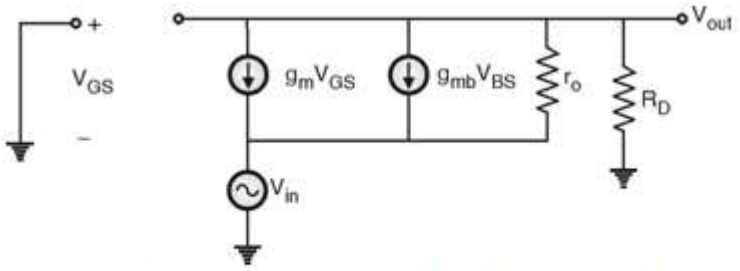
Figure below shows the CG amplifier in which the input signal is sensed at the source terminal and the output is produced at the drain terminal. The gate terminal is connected to V_B i.e. dc potential which will maintain the proper operating conditions.



Common gate amplifier

Fig 2.7

Figure below shows the small signal equivalent circuit of the CG amplifier.



small signal equivalent circuit of the CG amplifier

Fig 2.8

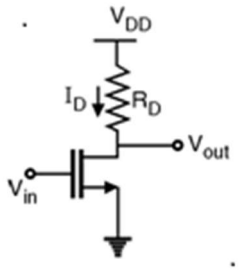
By analizing the small signal equivalent circuit, the voltage gain of CG amplifier is given by,

$A_v = = g_m R_D$

The important point is the gain is positive, further the input impedance is given by which shows that the input impedance of common gate amplifier is relatively low. Furthermore, the input impedance of of common gate stage is relatively low only if the load resistance connected to the drain is small.

Common Source Amplifier :

Figure below shows the common source amplifier circuit. In this circuit the MOSFET converts variations in the gate-source voltage into a small signal drain current which passes through a resistive load and generates the amplified voltage across the load resistor.



CS stage with resistive load

Fig 2.8.1

Now from above Figure,

$$I_D = \frac{1}{2} u_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

i.e.

$$. I_D = \frac{1}{2} u_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

V_{DD} - $I_D R_D = V_{out}$

Therefore $V_{out} = V_{DD} - \frac{1}{2} u_n C_{OX} \frac{W}{L} (V_{in} - V_{TH})^2 R_D$

Differentiating this equation with respect to V_{in}

$$. \frac{dV_{out}}{dV_{in}} = -u_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) R_D$$

Hence, the voltage gain $A_V = -g_m R_D$ $[\, g_m = u_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})]$

Also, from small signal model of shown in above Figure.

By applying KVL,

$V_{in} - V_{GS} = 0$

$$V_{in} = V_{GS}$$

Also

$$V_{out} + g_m V_{GS} R_D = 0$$
$$V_{out} = -g_m V_{GS} R_D$$

$$or\ V_{out} = -g_m V_{GS} R_D$$

Hence, The voltage gain $A_V = \frac{V_{out}}{V_{in}} - g_m R_D$

As the gate terminal of MOSFET draws a zero current we can say that the common source amplifier provides a current gain of infinity.

$$A_i = \infty$$

Also, because of zero gate current the input impedance of CS amplifier is also infinite.

$$R_{in} = \infty$$

In order to calculate the output impedance R_{out} consider the circuit shown in Figure below.

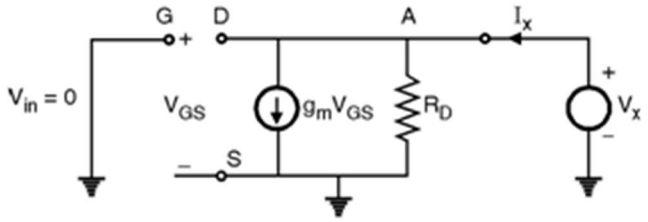


Fig 2.8.2

By applying KCL at point 'A'

We get,

$$g_m V_{GS} + \frac{V_x - 0}{R_D} = I_x$$

But $V_{GS} = 0$,

$$\frac{V_x}{R_D} = I_x$$

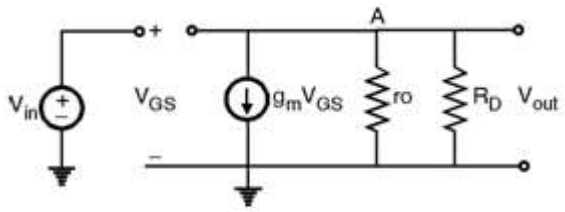
$$R_{out} = \frac{V_x}{I_x} = R_D$$

$$R_{out} = R_D$$

The output impedance of common source amplifier is,

$$R_{out} = R_D$$

If we consider the non Ideal effect such as channel length modulation in the CS amplifier then the small signal model includes one more resistor i.e. r o as shown in
Figure below.



CS amplifier with CLM

Fig 2.8.3

By applying KVL

We get

$$V_{in} - V_{GS} = 0$$

i.e. $V_{in} = V_{GS}$

By applying KCL at node A

We get,

$$g_m V_{GS} + \frac{V_{out} - 0}{r_o} + \frac{V_{out} - 0}{R_D} = 0$$

$$g_m V_{in} = -[\frac{V_{out}}{r_o} + \frac{V_{out}}{R_D}]$$

$$g_m V_{in} = -V_{out}(\frac{1}{r_o} + \frac{1}{R_D})$$

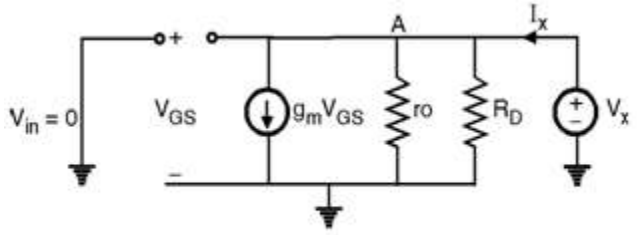
$$\frac{V_{out}}{V_{in}} = A_V = \frac{-g_m}{(\frac{1}{r_o} + \frac{1}{R_D})}$$

$$A_V = -g_m(r_o \,||R_D)$$

The voltage gain of CS amplifier with CLM is $-g_m(r_o||R_D)$

The current gain and input impedance will not be affected by CLM and theses are A_i = Av and R_{in} = Av. But the output impedance is affected because of CLM.

In order to calculate the output impedance of CS amplifier with CLM consider the circuit as shown in Figure below.



Output impedance of CS stage with CLM

Fig 2.8.4

By applying KCL at node 'A'

We get, $g_m V_{GS} + + = I_x$

$V_x = I_x$ [$V_{GS} = V_{in} = 0$]

$R_{out} = (ro \,||\, R_D)$

Thus, the output impedance of the CS amplifier with CLM is r o || R D.

In order to derive the voltage gain of CS amplifier with CLM using I-V characteristics consider the drain current equation with CLM as :

$I_{DS} = m_n C_{ox} (V_{GS} - V_{TH})^2 (1 + l V_{DS})$

where l is channel length modulation coefficient.

From Fig. 8.9.1(a)

$V_{DD} - I_D R_D = V_{out}$

$V_{out} = V_{DD} - m_n C_{ox} (V_{in} - V_{TH})^2 (1 + l V_{out})$

Differentiating this equation with respect to V_{in}.

By product rule of differentiation :

$= - m_n C_{ox} (V_{in} - V_{TH})^2$

$- m_n C_{ox} (1 + l V_{out}) Â´ 2 (V_{in} - V_{TH})$

$A_n = - m_n C_{ox} (V_{in} - V_{TH})^2 A_n - g_m R_D$

By approximating I_D as :

$I_D = m_n C_{ox} (V_{in} - V_{TH})^2$

We get, $A_n = - g_m R_D - R_D Ã— l Ã— I_D Ã— A_n$

$A_n(1 + R_D Ã— l I_D) = - g_m R_D$

i.e. $A_n = - g_m (ro || R_D)$

which is same as the voltage gain derived using small signal model.

Thus, the voltage gain of CS amplifier is depends upon the transconductance g_m, the linear resistor ro and load. In order to increase the gain we have to increase the g_m. In return we have to increase the ratio.

Hence the gain of amplifier is increases with increasing 'W' and decreasing 'L'. The ro resistance is appears in shunt with R_D because of this the effect of r o (i.e. channel length modulation) decreases the voltage gain of amplifier on the other hand the effect of parallel combination of ro and R_D decreases the output impedance (R_{out}) which is the beneficial effect.

In order to increase the gain of the amplifier along with g_m another important factor is the load impedance connected at the output. To have larger gain load impedance should be larger. The two choices of load impedance of CS stages are;

1) Current source load.

2) Diode connected load.

2.2.3 Bandwidth Capacitance and the Miller Effect

The key to understanding the wide bandwidth of the cascode configuration is the Miller effect. The Miller effect is the multiplication of the bandwidth robbing collector-base capacitance by voltage gain Av. This C-B capacitance is smaller than the E-B capacitance. Thus, one would think that the C-B capacitance would have little effect. However, in the C-E

configuration, the collector output signal is out of phase with the input at the base. The collector signal capacitively coupled back opposes the base signal. Moreover, the collector feedback is (1-Av) times larger than the base signal. Keep in mind that Av is a negative number for the inverting C-E amplifier. Thus, the small C-B capacitance appears (1+|Av|) times larger than its actual value. This capacitive gain reducing feedback increases with frequency, reducing the high frequency response of a C-E amplifier.

2.3 Differential Amplifier

Active loading is essential in the design of high-performance amplifiers. Though the circuitry involved is straightforward, the overall concept can be, in my opinion, somewhat abstruse. So we are going to take our time with this subject, with the primary goal (as usual) being a thorough, intuitive understanding.

Let's start by looking at a passively loaded, non-differential MOSFET amplifier:

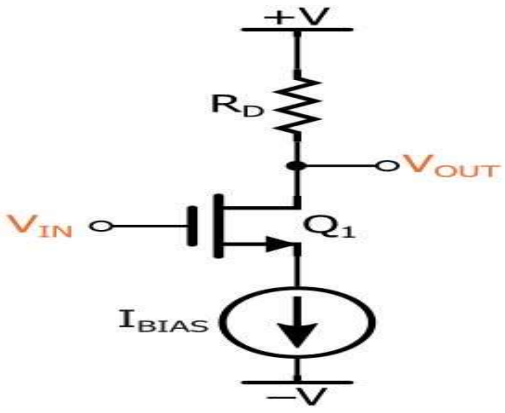


Fig 2.9

The current source biases the FET so that it can operate in the saturation region. The overdrive voltage (V_{OV})—i.e., the gate-to-source voltage (V_{GS}) minus the threshold voltage (V_{TH})—will be whatever value corresponds to a drain current of I_{BIAS}. We are assuming that the input signal will be a small-amplitude sinusoid with no DC offset, and thus the source voltage will be equal to (0 – V_{OV}).

What is the fundamental amplification mechanism in this circuit? Well, when biased in the saturation region, the FET acts like a voltage-controlled current source, with the drain current (if we ignore channel-length modulation) governed by the following equation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Thus, our small-amplitude input signal will create small-amplitude variations in drain current. The ratio between small changes in input voltage and the resulting small changes in drain current is the transconductance, denoted by g_m:

$$\Delta I_D = \Delta V_{GS} \times g_m$$

But the transconductance is not the same as the gain of the amplifier because we still need to convert this drain current into a voltage. This is the purpose of R_D: It converts drain-current variations into drain-voltage variations. From Ohm's law, we know that the ratio between the current variations and the voltage variations is the resistance R_D, and thus the amplitude of the variations in drain voltage will be equal to the amplitude of the variations in gate voltage multiplied by g_m multiplied by R_D. If we recall that the gate is the input node and the drain is the output node, we can say that the magnitude of the voltage gain (A_V) is the following:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = A_V = g_m \times R_D$$

So right away we see that one very easy way to increase the gain is to increase the value of the drain resistor. So why bother with the active load? If we want more gain, we just use more drain resistance!

2.3.1 The Drain-Resistor Problem

There is one major problem with the more-drain-resistance approach: that resistance applies not only to small-signal variations in drain current but also to the larger steady-state drain current required for biasing. Consider the following diagram:

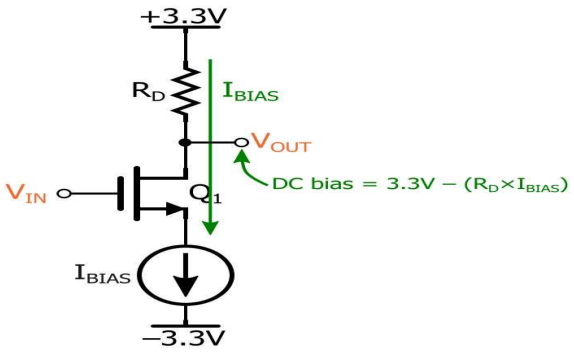


Fig 2.9.1

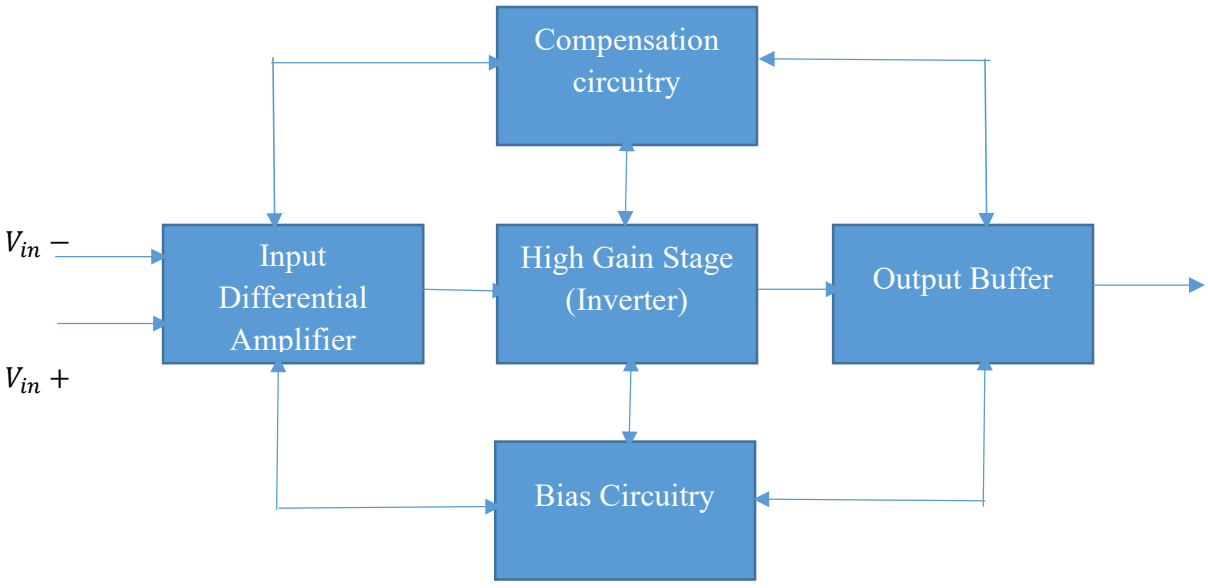
So the drain resistor creates a biasing problem: More resistance means more voltage drop, and this means a lower bias-point voltage for the drain node. This may not seem like a serious concern if you're thinking in terms of ±15 V supplies, but with ±3.3 V supplies, we need to be careful. If the drain voltage goes too low, the transistor will leave saturation and enter the triode region, and that's not something we can tolerate—MOSFET amplifiers need to stay in saturation. Even if the bias voltage itself is not low enough to cause problems, too much negative signal swing could push the FET into the triode region. In either case, our amplifier is compromised.

So using large amounts of drain resistance is impractical, especially in modern low-voltage systems. How can we provide more small-signal resistance without introducing bias-point problems?

2.4 Two–Stage Op-Amp

2.4.1 Introduction

A transistor circuit containing two stages of amplification is known as TWO STAGE AMPLIFIER. Successful application of feedback around an amplifier having large amounts of open-loop gain is done most readily if the amplifier has a simple frequency response (preferably one with a single dominant pole), and input and output impedance levels which minimize the interactions with the source and load. For many applications, a high input impedance and a low output impedance work well. The "two-stage" does a good job of meeting these requirements in applications ranging from general purpose op-amps to wide-band video amplifiers to audio power amplifiers.



2.4.2 Advantages:

It has excellent frequency response. The gain is constant over the audio frequency range which is the reason of most importance for speech, music etc. It has lower cost since it employee's registers and capacitors which are cheap. The circuit is very compact as the modern resisters and capacitors are small and extremely light.

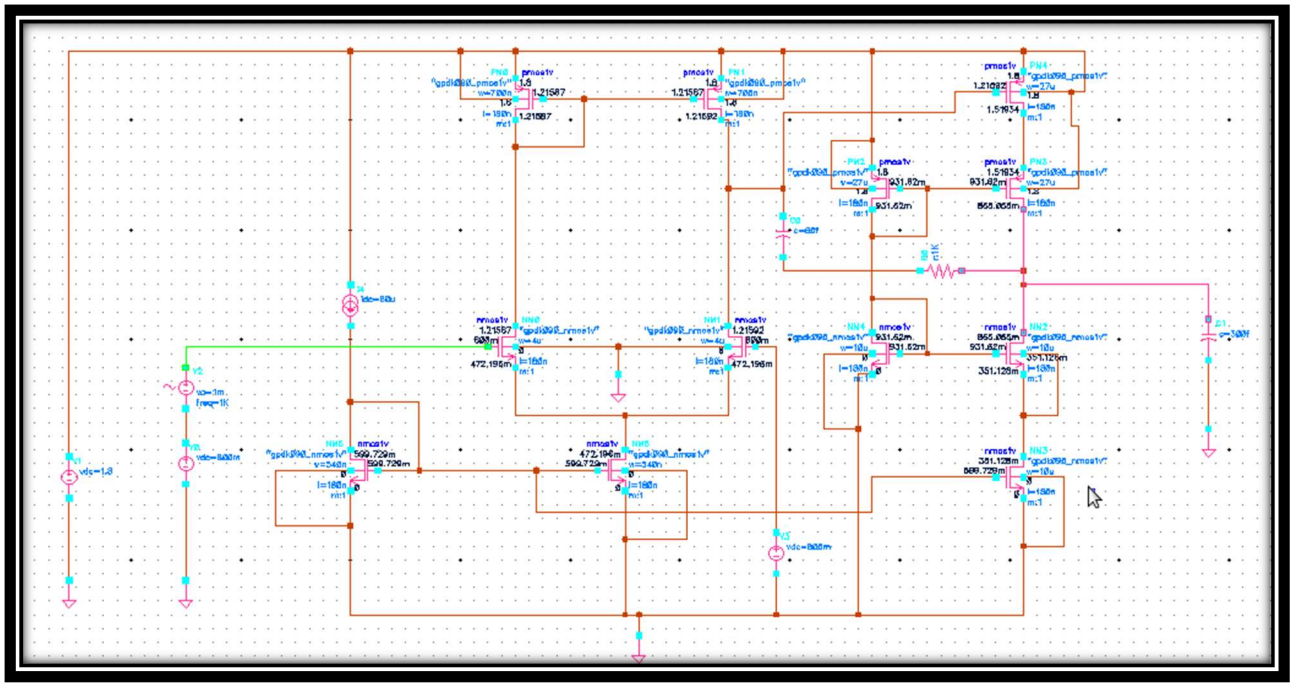
2.4.3 Disadvantages:

They tend to become noisy with age, particularly in moist climate. Impedance matching is poor.

CHAPTER 3

PROPOSED CIRCUITORY

3.1 Main Circuit



3.2 Design Specifications

S.No	Specifications	Value
1	Technology	Gpdk 90
2	Power Supply(V_{DD})	1.8 V
3	Load Capacitance(C_L)	0.5 pF
4	Gain	>=50 dB
5	Phase Margin	>=45 degree
6	Gain Bandwidth	>600 MHz
7	Slew rate (SR)	>=500 V/usec
8	ICMR(+)	1.6 V
9	ICMR(-)	0.8 V

3.3 Design Procedure

STEP 1: L= 180nm

Cc >= 0.22 $C_{/}$
= 0.22 * 0.5 *p F
=110 f F

$S_R = \frac{I_5}{C_c}$ => $I_5 = S_R$ * Cc
= 500 V/us * 110 f F
= 65 uA

STEP 2: DESIGN OF M1,M2

GBW = gain * bandwith
gm1 = GBW * Cc *2*π
=1 Ghz *110 f F *2* π
=753.9u
=753 u

$.\left(\frac{W}{L}\right)_1 = \frac{gm^2}{2*\mathrm{Id}*\mathrm{K}} = \frac{753\ u^2}{2*32.5\ \mathrm{u}\ *416\ \mathrm{u}}$ =20.96 =21

STEP 3: DESIGN 0F M3,M4

$.\left(\frac{W}{L}\right)_3 = \frac{2*Id_3}{\mathrm{K}*(Vdd-ICMR-Vt3\max+Vt1\min)^2}$

$== \frac{2*32.5\ u}{204*(1.8-I.6-0.15+0.29)^2}$ = 3.62 = 4

STEP 4: DESIGN OF M5

Vd sat <= ICMR - $\sqrt{\frac{2*Id}{\beta\ 1}}$ -Vt1 max
= 0.8 -0.115.4 – 0.38
= 343 mV

$.\left(\frac{W}{L}\right)_5 = \frac{2*Id}{\mathrm{K}*Vd\ sat^2} = \frac{2*65}{416*(343\ mV)^2}$ = 2.65 = 3

STEP 5: DESIGN OF M6
In order to have good phase margin
gm6 >=10* gm4

gm6 >= 10*753

= 7530

gm4 = $\sqrt{K * \left(\frac{W}{L}\right)_4 * 2 * Id} = \sqrt{204u * 4 * 2 * 32.5}$ =197 u

$.\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 * \frac{gm6}{gm4} = 4 * \frac{7530}{197} =$ 152.8 =153

STEP 6: Now the current I_6 is given by

$I_6 = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} * I_4$

$= \frac{153}{4} *$ 32.5 u =1.24 mA

Since the M6 and M7 form the cascode configuration we consider

$.\left(\frac{W}{L}\right)_6 = .\left(\frac{W}{L}\right)_7 =$ 153

Since the M7 and M8 form the current mirror we consider $.\left(\frac{W}{L}\right)_7 = .\left(\frac{W}{L}\right)_8 =$ 153

STEP 7: DESIGN OF M9, M10, M11, M12

We know that $\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_5 * \frac{I_9}{I_5} =$ 57

Since the M9 and M10 form the cascode configuration we consider $.\left(\frac{W}{L}\right)_9 = .\left(\frac{W}{L}\right)_{10} =$ 57

Since the M7 and M8 form the current mirror we consider $.\left(\frac{W}{L}\right)_{10} = .\left(\frac{W}{L}\right)_{11} =$ 57

Now since the M5 forms current mirror with M12 we have

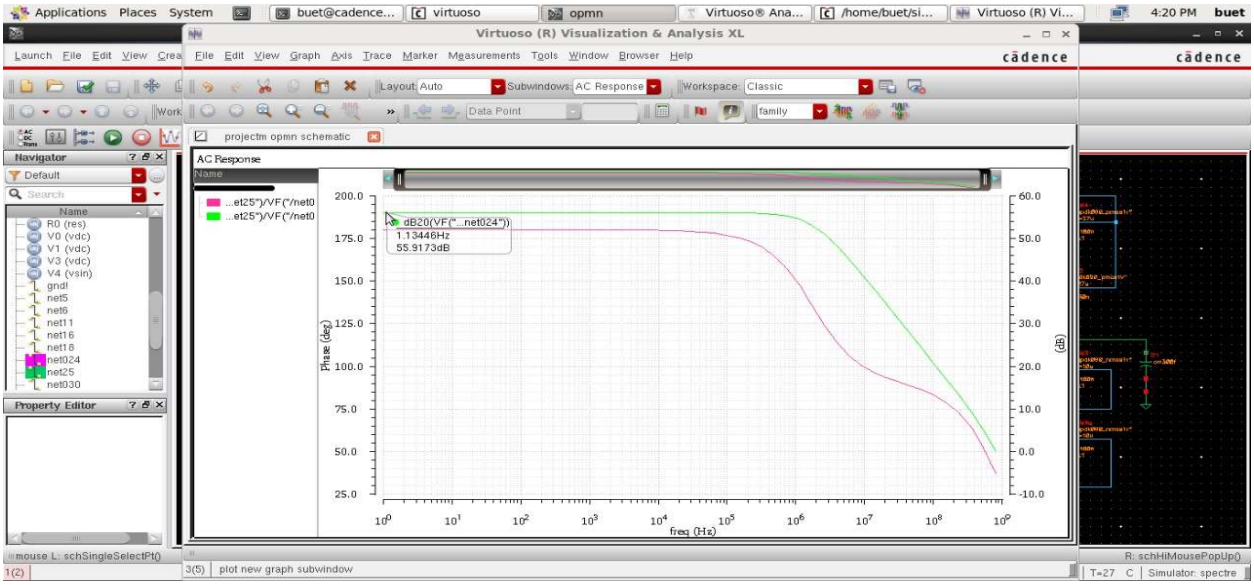
$\left(\frac{W}{L}\right)_5 = .\left(\frac{W}{L}\right)_{12} =$ 3

CHAPTER 4

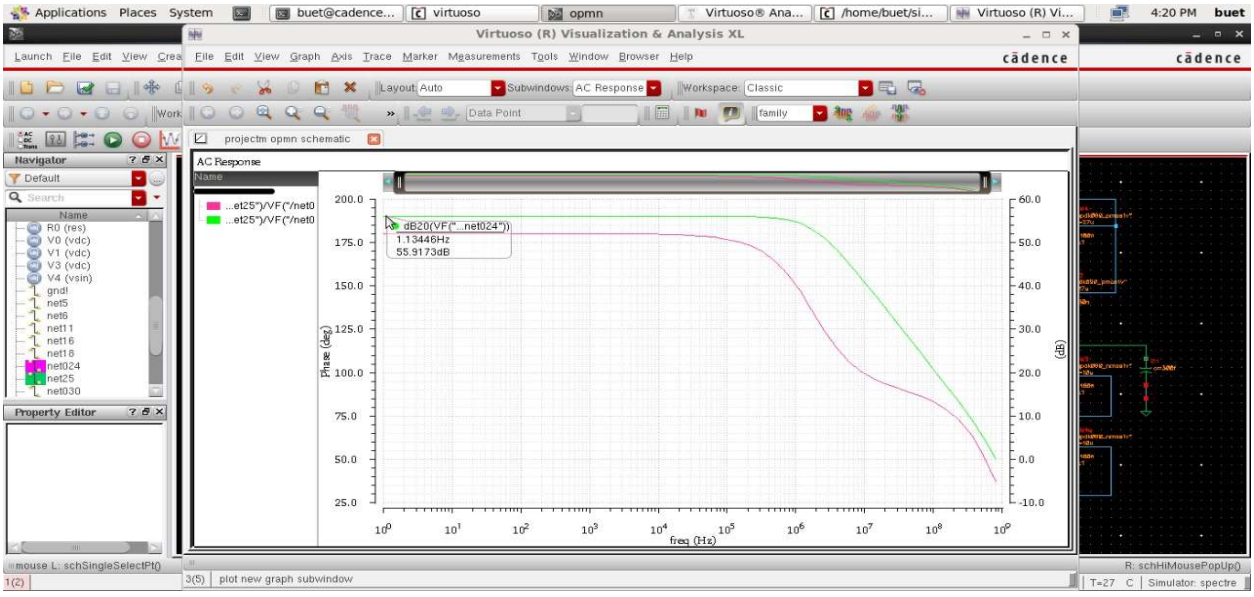
SIMULATION RESULTS & DISCUSSIONS

4.1 Outputs

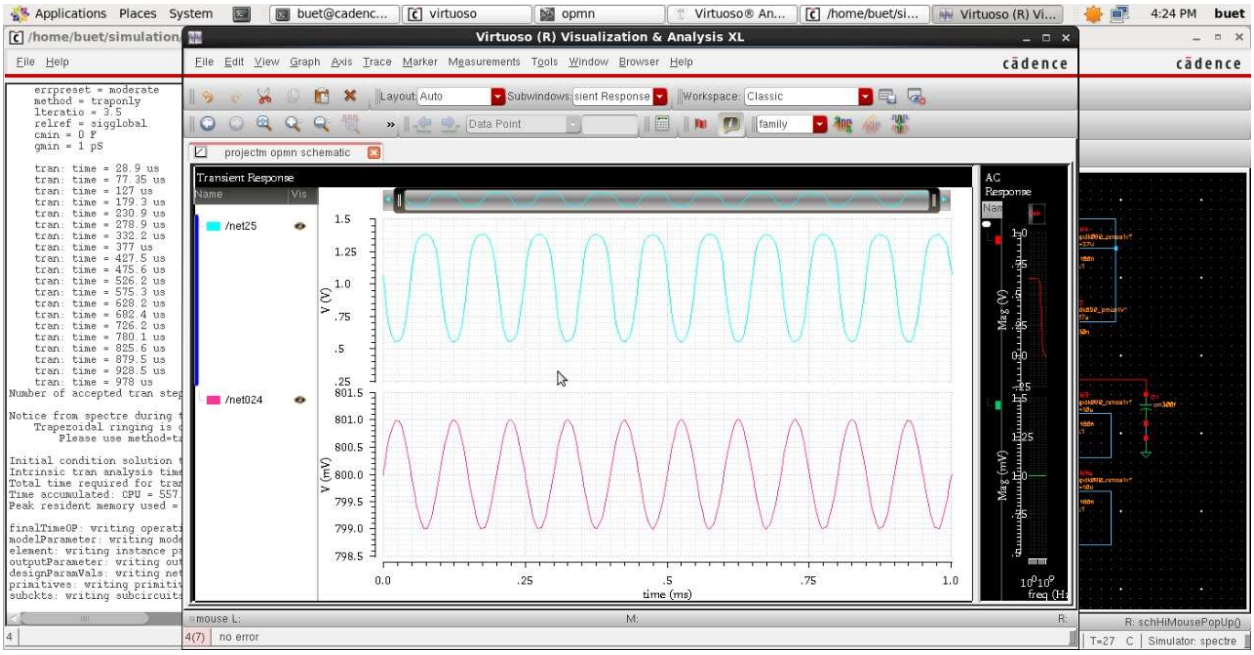
4.1.1 Gain:



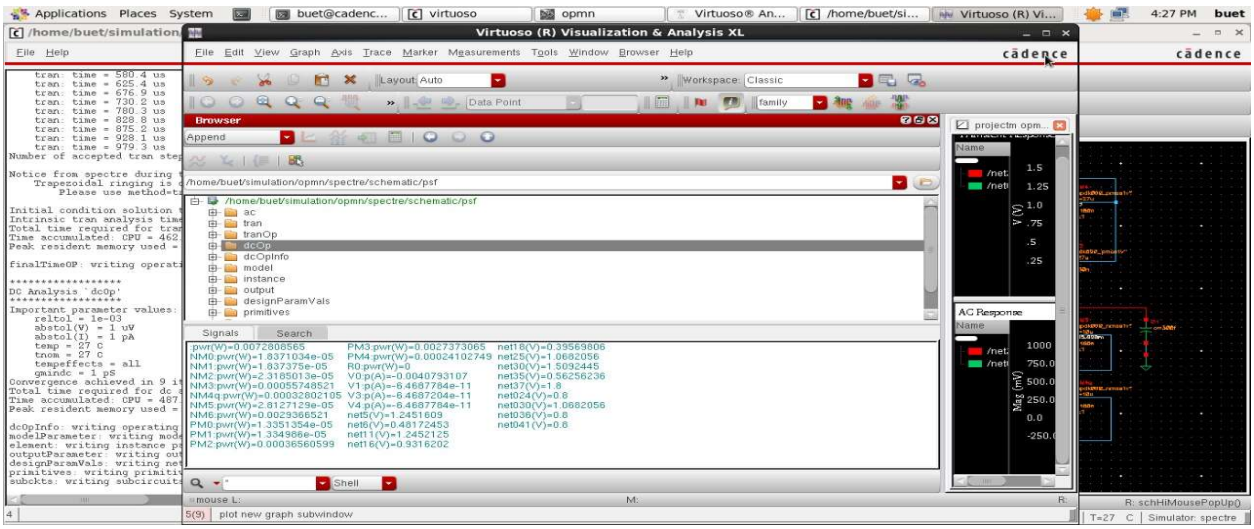
4.1.2 Phase:



4.1.3 Transient Analysis:



4.1.4 Power Report:



4.2 Project Results

S.No	Specifications	Acquired Values
1	Technology	Gpdk90
2	Power Supply (V_{DD})	1.8 V
3	Load Capacitance (C_L)	0.5 pF
4	Gain	53.02 dB
5	Phase Margin	47 degree
6	Gain Bandwidth	800 MHz
7	Slew rate (SR)	400 V/usec
8	ICMR (+)	1.6 V
9	ICMR (-)	0.8 V
10	Power Dissipation	<= 0.7mW
11	CMRR	43dB

4.3 Advantages

- Since Differential Amplifier is used in the first stage, good amount of noise rejection is produced by the circuit.
- Since unity gain bandwidth is considerably high, it can be used in signal recovering circuits in the communication circuits.
- This circuit is able to amplify DC signals as well as AC signals and hence it can be used in mixed signal design.

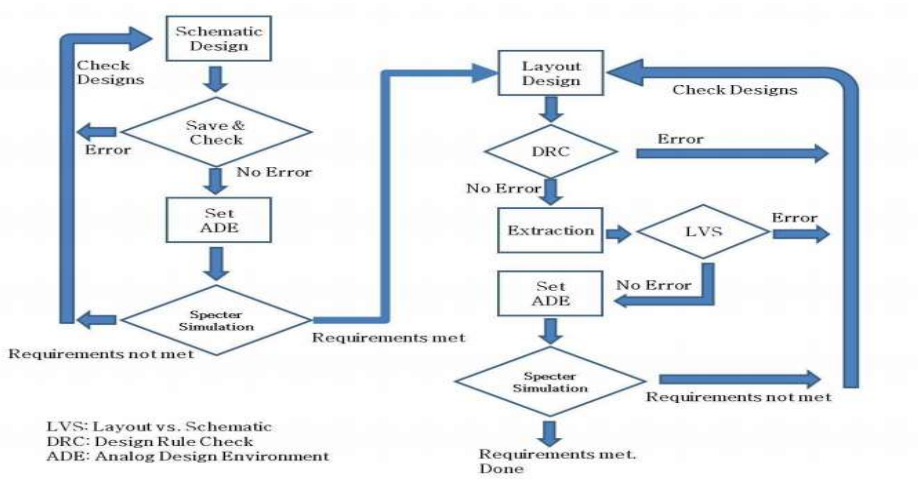
4.4 Applications

- It is used in summer, subtractor circuits
- It is used in integrator, differentiator circuits.
- It is used for various filter design like low pass, high pass, butter-worth etc.
- It is used in Instrumentation amplifiers.
- It is used in voltage-to-current converter circuit.
- Our circuit is mainly useful in high frequency wireless application

4.5 what is cadence virtuoso?

Designed to help users create manufacturing-robust designs, the Cadence Virtuoso Analog Design Environment is the advanced design and simulation environment for the Virtuoso platform. It gives designers access to a new parasitic estimation and comparison flow and optimization algorithms that help to centre designs better for yield improvement and advanced matching and sensitivity analyses. By supporting extensive exploration of multiple designs against their objective specifications, the Virtuoso Analog Design Environment sets the standard in fast and accurate design verification.

4.5.1 Overall Design Flow For cadence virtuoso

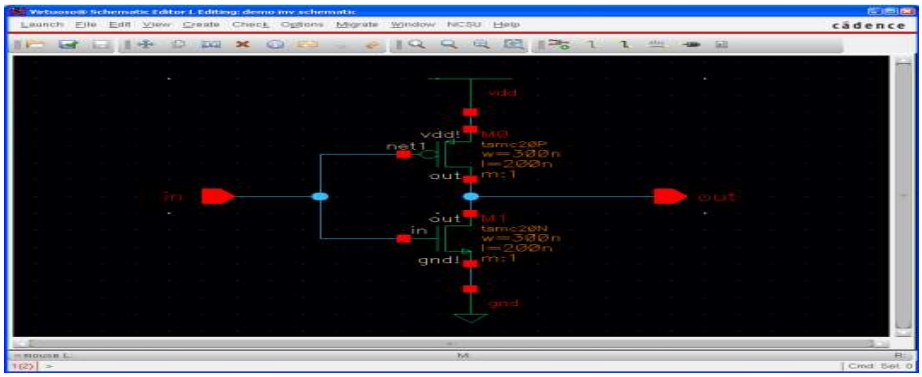


STEP 1: Create Library

- Tools -> Library Manager
- File -> New -> Library
- Give a name and attach it to a technology library

STEP 2: Schematic

- Create a cell view and select the library just created : File -> new
- Draw a schematic : Add instances – PMOS, NMOS, VDD, GND etc.
- Add wires : Create - > Wire
- Add pins : Create - > Pin

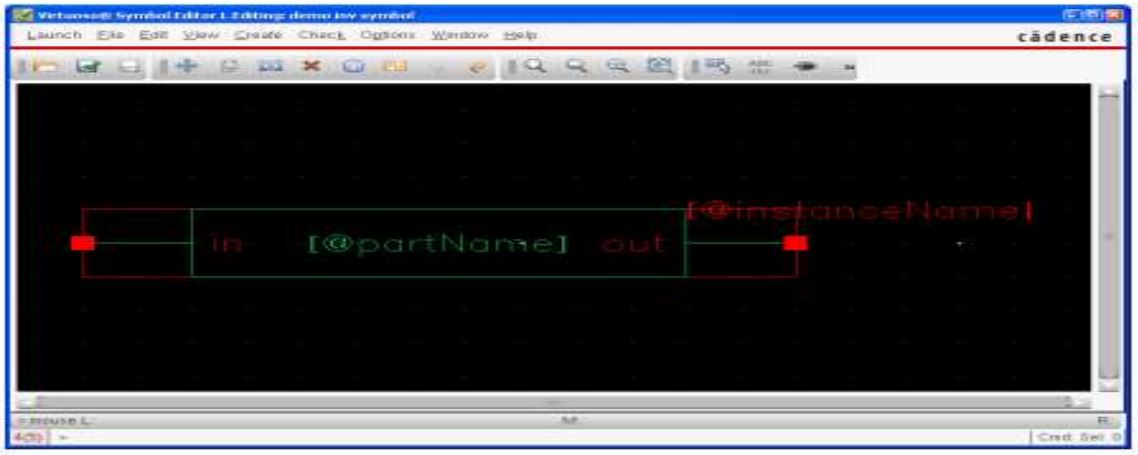


Check and save - > to make sure there are no errors. Now, we completed a schematic design.

STEP 3: Create a symbol (Optional)

For hierarchical design, we may need to make symbols of designed circuits.

Create - > CellView - > From Cellview

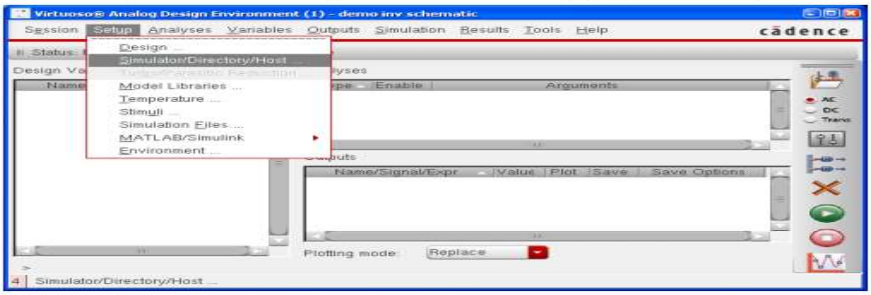


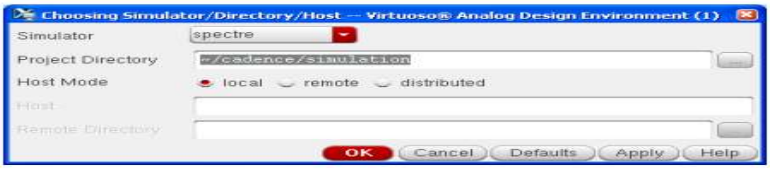
Remember that when you use more than one symbol in schematic, they all will have common Vdd and Gnd even if there are one Gnd and Vdd for each symbol (in the original design). To design with symbols in layout, you should make sure that all of the Vdd and Gnds are connected.

STEP 4: Run Spectre simulation (Transient analysis)

We will run spectre simulation. This section is for both schematics and layouts. I will show an example for a schematic. You can do the same thing for a layout.

- Launch ADE (Analog Design Environmental) L
  Launch - > ADE L
- Basic setup Check if your simulator is spectre. You can modify project directory





- Choose a type of analysis – transient

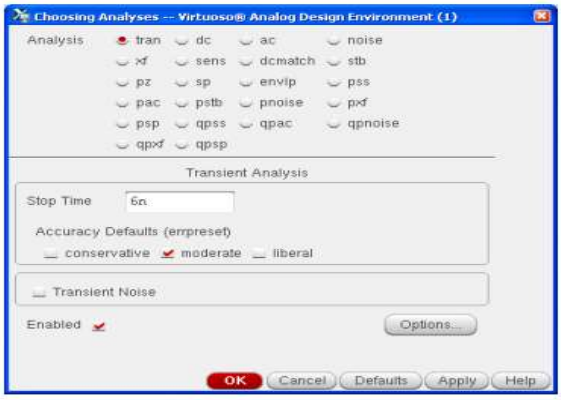
A. Choose tran

B. Give Stop time which means how long you want to simulate

C. Select moderate as accuracy defaults

D. Do not check Transient Noise

E. Check Enabled

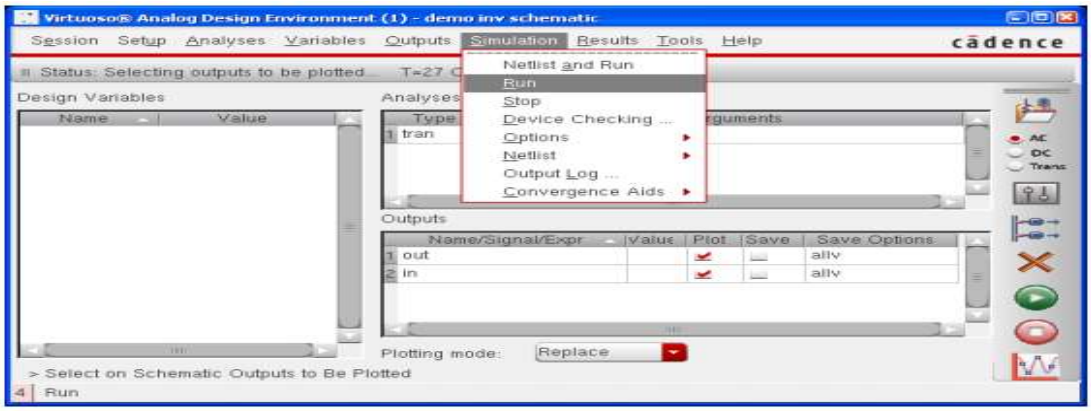


STEP 5: Select signals to plot

- Outputs - > To Be Plotted - > Select On Schematic Click a signal (Pin) on a schematic/extracted.

STEP 6: Run simulation

- Simulation - > Run



CHAPTER 5

CONCLUSION

The main task of this project is to design the single stage and two stage CMOS operational amplifier using 180nm technology in Cadence Tools. Firstly we studied the basic characteristics of nMOS and pMOS transistors, their operating region. We designed basic analog building blocks like MOSFET switch, MOSFET diode, and current mirror. Then we designed CMOS amplifier and common source amplifier. Finally, with the help of these building blocks we designed single stage and two stage CMOS operational amplifier. The notable performance areas were the gain, gain bandwidth, slew rate, CMRR.

CHAPTER 6

REFERENCES

[1] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill International Edition, 2001.

[2] Ramakrishna Kundu, Abhishek Pandey, Subhra Chakraborty, Vijay Nath, " A current mirror based two stage CMOS Cascode Op-Amp for High Frequency Application," IEEE transactions on journal of Engineering Science and Technology, Vol. 12, No. 3(2017) 686-700