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GEM5 with RISC-V: A Tinkerer's Guide to Installation



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GEM5 is a powerful computer architectural research and training tool that hosts system-level architecture and processor microarchitecture series. When combined with RISC-V Instruction Set Architecture, GEM5 becomes even more flexible, enabling users to simulate and explore the abilities of this open-source ISA. This material aims at providing a complete tutorial for those enthusiasts who want to install GEM5 with RISC-V support.

I am utilizing the following specifications on my operating system:

```
vboxuser@test:~/Downloads$ neofetch
  .-+o0ssssoo+-.
   `:+ssssssssssssssssssss+:
    -+ssssssssssssssssyyssss+-.
     .osssssssssssssssssdMMMNyssso.
    /sssssssssshdmmNNmmyNMMMHssssss/
   +ssssssssshmydMMMMMMNdddyssssssss+
  /sssssssshNMMMyhyyyyhmNMMMNhssssssss/
  sssssssssdMMMNhsssssssssshNMMMdssssssss.
  +sssshhhyNMMNyssssssssssssyNMMMyssssssss+
  ssyNMMMNyMhsssssssssssshhmmhssssssssso
  ssyNMMMNyMhsssssssssssshhmmhssssssssso
  +sssshhhyNMMNyssssssssssssyNMMMyssssssss+
  .ssssssssdMMMNhsssssssssshNMMMdssssssss.
  /sssssssshNMMMyhyyyyhdNMMMNhssssssss/
  +ssssssssdmydMMMMMMMdddyssssssss+
  /sssssssssssshdmmNNNmyNMMMHssssssss/
  .osssssssssssssssssdMMMNyssso.
   -+ssssssssssssssssssyyyssss+-.
    `:+ssssssssssssssssssss+:
     .-/+o0ssssoo+-.

vboxuser@test
-----
OS: Ubuntu 22.04.4 LTS x86_64
Host: VirtualBox 1.2
Kernel: 6.5.0-41-generic
Uptime: 1 hour, 51 mins
Packages: 1935 (dpkg), 9 (snap)
Shell: bash 5.1.16
Resolution: 1701x936
DE: GNOME 42.9
WM: Mutter
WM Theme: Adwaita
Theme: Yaru [GTK2/3]
Icons: Yaru [GTK2/3]
Terminal: gnome-terminal
CPU: Intel Xeon Silver 4216 (13) @ 2
GPU: 00:02.0 VMware SVGA II Adapter
Memory: 1696MiB / 41705MiB
```



Installing Gem5 Toolchain

To install the GEM5 toolchain, execute the following commands:

```
$ sudo apt install build-essential git m4 scons zlib1g zlib1g-dev libprotobuf-de
$ git clone https://github.com/gem5/gem5.git
$ cd gem5/
$ scons build/RISCV/gem5.opt -j8
```

To build a simulation using simple-riscv.py, run the following command:

```
$ build/RISCV/gem5.opt configs/learning_gem5/part1/simple-riscv.py
```

```
vboxuser@test:~/gem5$ build/RISCV/gem5.opt configs/learning_gem5/part1/simple-riscv.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 24.0.0.0
gem5 compiled Jul 1 2024 16:26:37
gem5 started Jul 1 2024 16:36:40
gem5 executing on test, pid 30861
command line: build/RISCV/gem5.opt configs/learning_gem5/part1/simple-riscv.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/arch/riscv/isa.cc:276: info: RVV enabled, VLEN = 256 bits, ELEN = 64 bits
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/sim/syscall_emul.hh:1075: warn: readlink() called on '/proc/self/exe' may yield unexpected results in various settings.
    Returning '/home/vboxuser/gem5/tests/test-progs/hello/bin/riscv/linux/hello'
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
Hello world!
Exiting @ tick 488719000 because exiting with last active thread context
```

To view the statistics, navigate to the /gem5/m5out folder and open the stats.txt .

Installing RISC-V Toolchain

To cross-compile C code for a RISC-V target, you will need to use the RISC-V toolchain.

```
$ sudo apt-get install autoconf automake autotools-dev curl python3 python3-pip libm
$ git clone https://github.com/riscv/riscv-gnu-toolchain
$ cd riscv-gnu-toolchain/
$ ./configure --prefix=/opt/riscv
$ sudo make linux
```



Takes huge amount of time

Here's an example of how you can compile a C program for same architecture:

```
$ gcc pi.c -lm -O pi -static -O3
$ ./pi

pi = 3.14159265358979323846264338327950288419716939937510582097494459230781640628620
```

Now, cross-compiling for the RISC-V target:

```
$ /opt/riscv/bin/riscv64-unknown-linux-gnu-gcc pi.c -lm -O pi_exec -static -O3
```

This process will generate a binary named 'pi_exec'.

Copy this binary to the directory /gem5/tests/testprogs/hello/bin/riscv/linux

It is necessary to make minor adjustments to the file
/gem5/configs/learning_gem5/part1/simple-riscv.py by updating the binary name to
'pi_exec' @line 60 or providing the path to the binary created.

```

32 import m5
33 from m5.objects import *
34
35 system = System()
36
37 system.clk_domain = SrcClockDomain()
38 system.clk_domain.clock = "1GHz"
39 system.clk_domain.voltage_domain = VoltageDomain()
40
41 system.mem_mode = "timing"
42 system.mem_ranges = [AddrRange("512MB")]
43 system.cpu = RiscvTimingSimpleCPU()
44
45 system.membus = SystemXBar()
46
47 system.cpu.icache_port = system.membus.cpu_side_ports
48 system.cpu.dcache_port = system.membus.cpu_side_ports
49
50 system.cpu.createInterruptController()
51
52 system.mem_ctrl = MemCtrl()
53 system.mem_ctrl.dram = DDR3_1600_8x8()
54 system.mem_ctrl.dram.range = system.mem_ranges[0]
55 system.mem_ctrl.port = system.membus.mem_side_ports
56
57 system.system_port = system.membus.cpu_side_ports
58
59 thispath = os.path.dirname(os.path.realpath(__file__))
60 #binary = os.path.join(
61 #    thispath,
62 #    "../..",
63 #    "tests/test-progs/hello/bin/riscv/linux/pi",
64 #)
65 binary = os.path.join(
66    thispath,
67    "../..",
68    "tests/test-progs/hello/bin/riscv/linux/pi_exec",
69 )

```

After making the necessary adjustments, rebuild the simulation:

```
$ build/RISCV/gem5.opt configs/learning_gem5/part1/simple-riscv.py
```

You can view the output on the terminal and check statistics as described earlier.

```

vboxuser@test:~/gem5$ build/RISCV/gem5.opt configs/learning_gem5/part1/simple-riscv.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 24.0.0-0
gem5 compiled Jul 1 2024 16:26:37
gem5 started Jul 6 2024 18:11:30
gem5 executing on test, pid 21217
command line: build/RISCV/gem5.opt configs/learning_gem5/part1/simple-riscv.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/nem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/arch/riscv/isa.cc:276: Info: RV64 enabled, VLEN = 256 bits, ELEN = 64 bytes
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/stm/stmulate.cc:199: Info: Entering event queue @ 0. Starting simulation...
src/stm/syscall_emul.cc:85: warn: ignoring syscall set_robust_list(...)
    (further warnings will be suppressed)
src/stm/syscall_emul.hh:1075: warn: readlink() called on '/proc/self/exe' may yield unexpected results in various settings.
    Returning '/home/vboxuser/gem5/tests/test-progs/hello/bin/riscv/linux/pi_exec'
src/stm/nem_state.cc:148: Info: Increasing stack size by one page.
src/stm/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)

pi = 3.141592653589793238462643383279502884197169399375105820974944592307816406286208998628034825342117067982148086513282306647093844609550582231725359408128481117450284102701938521105559644622948
95491511609433057270365759591953092186117381932611793105118548744623799627495673518575272489122793818301194912983367336244065643086213949463952247371907021798609437027705392171762931767523846748
18467669405132000568127145263560827785771342757789691736371787214684409012249534301465495853710507922796892589235421995611212902196086403441815981362977477130996051870721134999999 etc...
Exiting @ tick 178243677664000 because exiting with last active thread context

```

Thanks for reading!

Resources

1. [Riscv Toolchain](#)

2. [Gem5 Toolchain](#)

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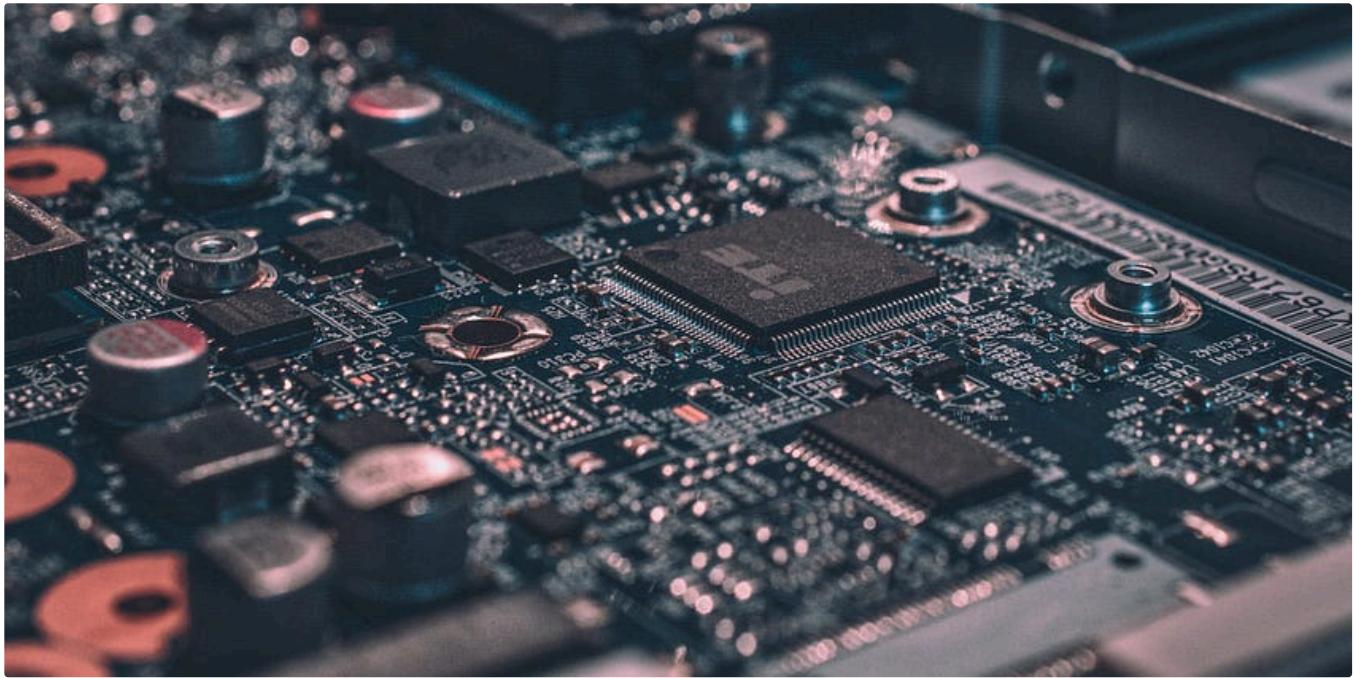
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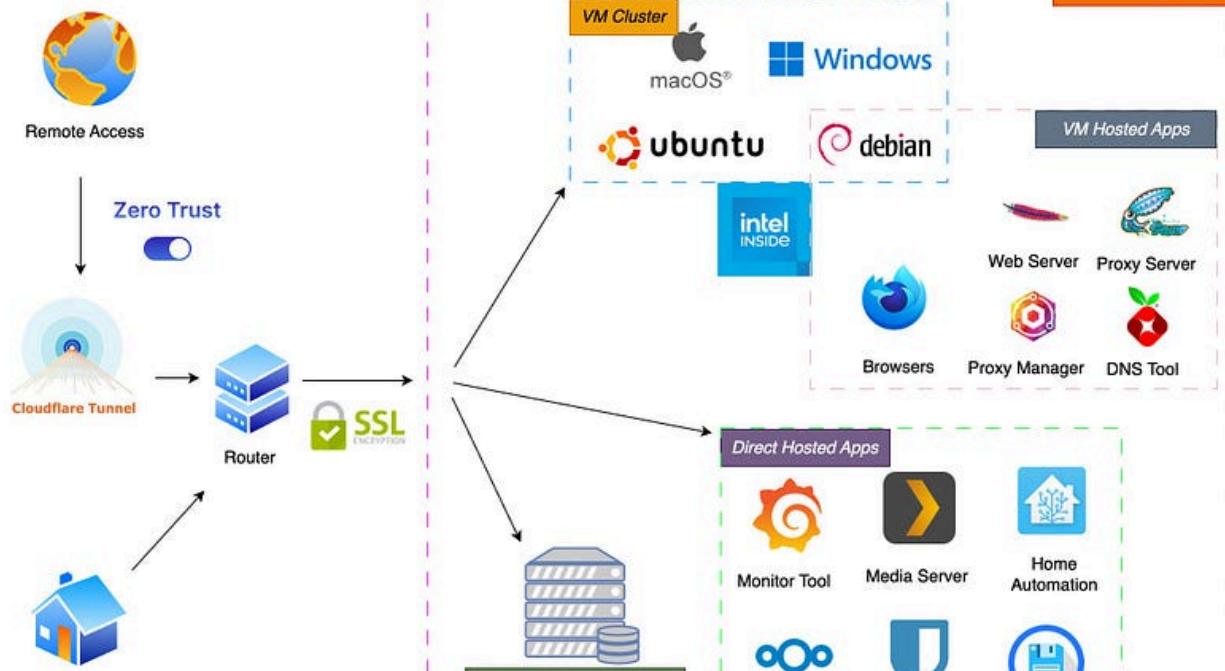
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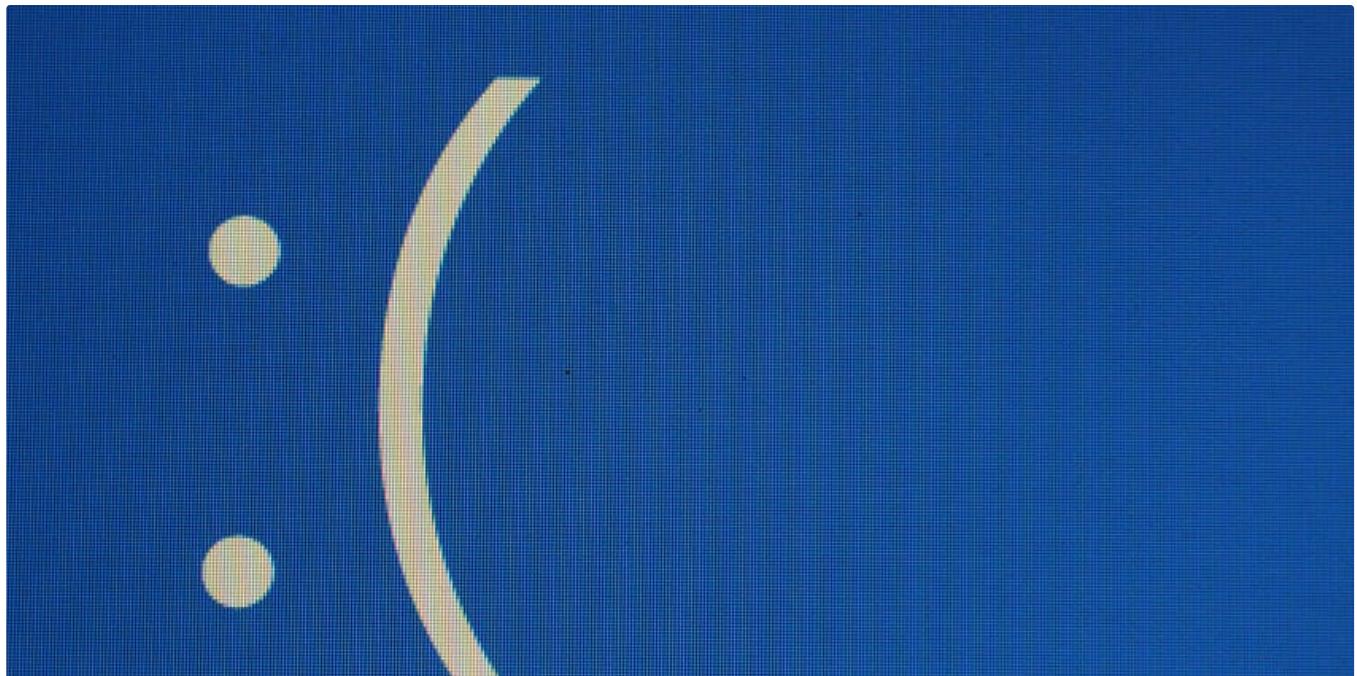
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