

UNIVERSITY OF TEXAS AT DALLAS
Department of Electrical & Computer
Engineering

CE6325:VLSI Design

Project-6
Cell Library -256 Bit Even/Odd Up-down
Counter

Submitted by,
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DESIGN AND DESCRIPTION:

The design is an even/odd up-down counter with a 256-bit output. Inputs are clock named as "clk", reset as "rst", "updown" and "even". Output has maximum and minimum value.

The maximum is $[(2^{256})-1]$, and the Minimum is 0.

The increment/decrement of this counter is circular (i.e., when out=0 and decremented by 1, then out= $[(2^{256})-1]$ and vice versa while incrementing the out= $[(2^{256})-1]$ by 1, which results in out=0).

The model will get triggered for every positive edge of the clock cycle and the reset. The count will increase when the value of updown is set 'high' and decrease when the updown is 'low'.

When even is set 'high', the output increases (i.e. updown=1) or decreases (i.e. updown=0) to the nearest even number of the previous output;. Similarly, It will increase (i.e. updown=1) or decrease (i.e. updown=0) to the nearest odd number of the previous output when even is set 'low'

DESCRIPTION AND FUNCTIONALITY:

Standard Cell Library:

The library for the 256 Bit Even/Odd Up-down Counter was created using the 65nm technology. Library consists of schematic, layout, and abstract for each functional cells.

The cells included in the design are:

Inverter

NAND2

NOR2

XOR2

AOI22

OAI21

OAI211

MUX 2:1

D Flip-Flop

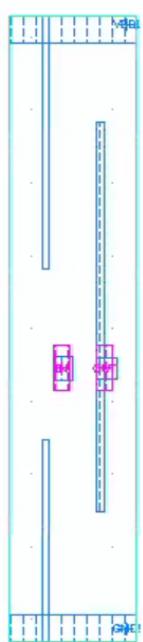
Filler Cell: The filler cell is basically used to fill the spaces between the cells.

The height of all the cells = 8.606um

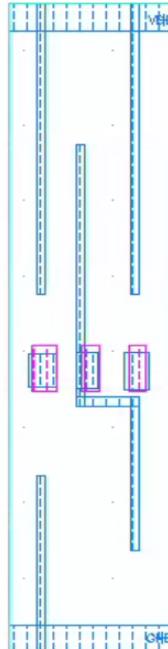
The pins are on the same grid and are placed at a distance of = $0.26 \times n$

The offset has been set to = $0.13 + 0.26 \times n$

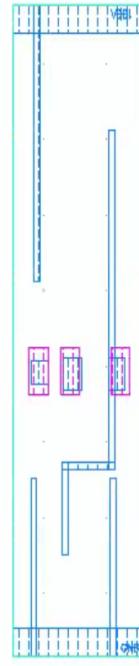
ABSTRACT VIEWS



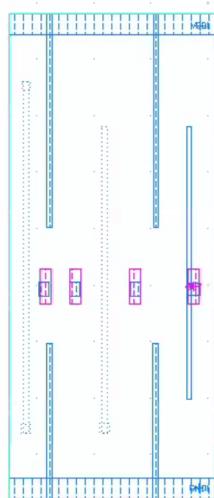
INVERTER



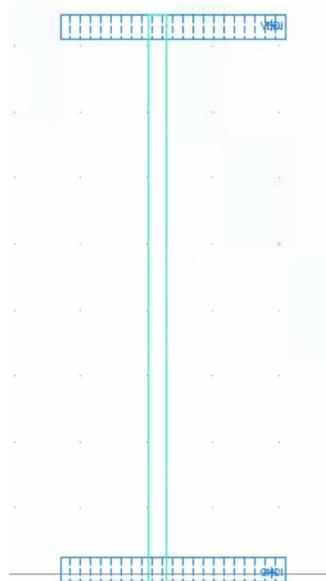
NAND



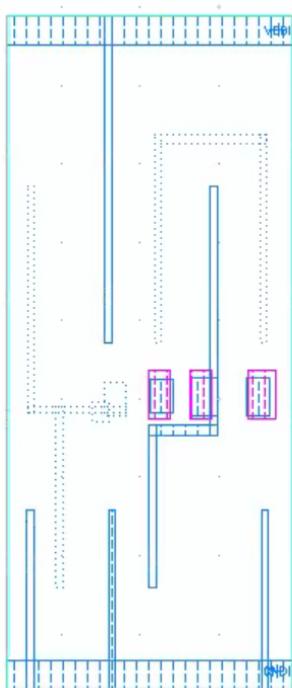
NOR



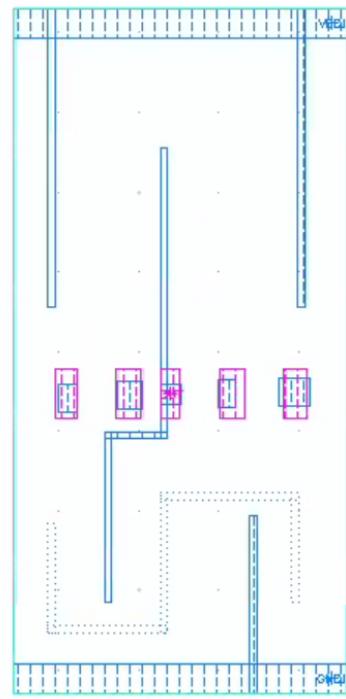
MUX



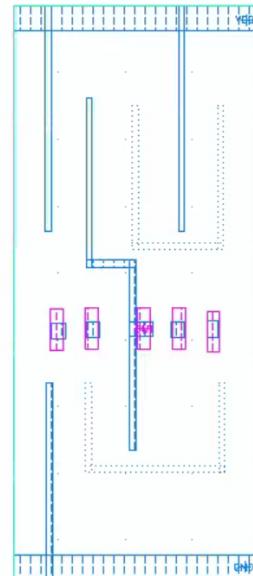
FILLER



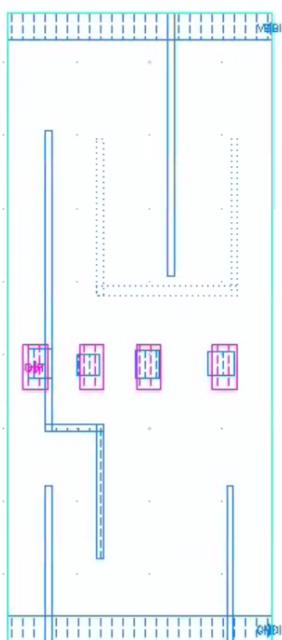
XOR



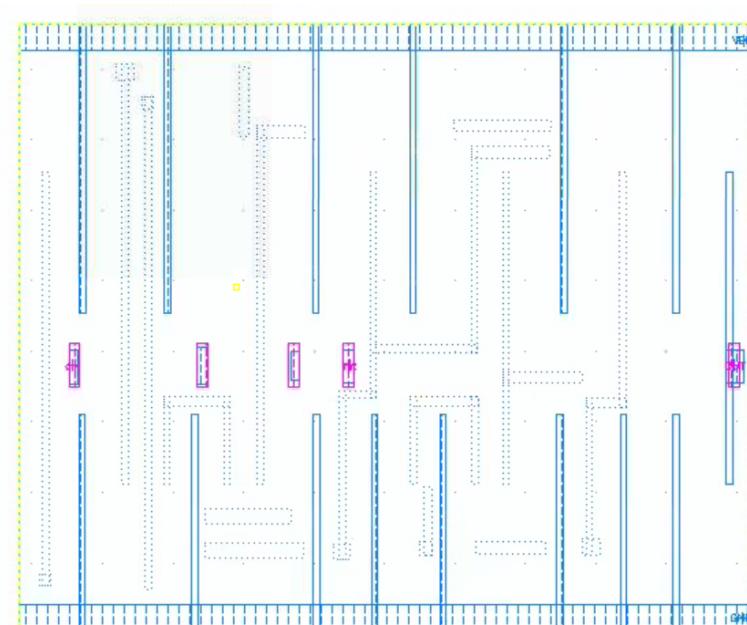
OAI22



AOA1211



AOI21



DFF

PROCEDURE:

Using PrimeLib:

The PrimeLib tool is used to characterize the cells and create a library using the .lib files generated post the PrimeLib process. To perform PrimeLib successfully, PEX files of each cell are required to be configured and characterized. Basically, the .lib files that we generate for all the cells should be combined in order to get a .db file.

Synthesized Verilog Netlist and Library Exchange Format:

We use Design Vision tool, to get a synthesized verilog code. The mapping process is done using the combined library from PrimeLib. After the conversion of Verilog code to Synthesized Verilog code, After getting all the abstracts of the cells we generate a .lef file. The .lef file and .v files are used for placing and routing.

Innovus Tool for Placement and Routing:

The Innovus tool helps in automatic placement and routing of the standard cells to a synthesized Verilog code that we generated in the design vision. We export the design by using the .lef and .v file in Innovus. The Standard cells will be placed and automatic routing is done.

COMBINED LAYOUT AND SCHEMATIC VIEW:

Cell Count: Cell Count from the Synthesized Code was= 9587 cells

Cell Count from our design = 12925 cells

out_reg[431]	dff	updated	89.500000 n
out_reg[432]	dff	updated	89.500000 n
out_reg[433]	dff	updated	89.500000 n
out_reg[434]	dff	updated	89.500000 n
out_reg[435]	dff	updated	89.500000 n
out_reg[436]	dff	updated	89.500000 n
out_reg[437]	dff	updated	89.500000 n
out_reg[438]	dff	updated	89.500000 n
out_reg[439]	dff	updated	89.500000 n
out_reg[440]	dff	updated	89.500000 n
out_reg[441]	dff	updated	89.500000 n
out_reg[442]	dff	updated	89.500000 n
out_reg[443]	dff	updated	89.500000 n
out_reg[444]	dff	updated	89.500000 n
out_reg[445]	dff	updated	89.500000 n
out_reg[446]	dff	updated	89.500000 n
out_reg[447]	dff	updated	89.500000 n
out_reg[448]	dff	updated	89.500000 n
out_reg[449]	dff	updated	89.500000 n
out_reg[450]	dff	updated	89.500000 n
out_reg[451]	dff	updated	89.500000 n
out_reg[452]	dff	updated	89.500000 n
out_reg[453]	dff	updated	89.500000 n
out_reg[454]	dff	updated	89.500000 n
out_reg[455]	dff	updated	89.500000 n
out_reg[456]	dff	updated	89.500000 n
out_reg[457]	dff	updated	89.500000 n
out_reg[458]	dff	updated	89.500000 n
out_reg[459]	dff	updated	89.500000 n

r85/U1_B_496	NAND2	updated	15.660000
r85/U1_B_497	NAND2	updated	15.660000
r85/U1_B_498	NAND2	updated	15.660000
r85/U1_B_499	NAND2	updated	15.660000
r85/U1_B_500	NAND2	updated	15.660000
r85/U1_B_501	NAND2	updated	15.660000
r85/U1_B_502	NAND2	updated	15.660000
r85/U1_B_503	NAND2	updated	15.660000
r85/U1_B_504	NAND2	updated	15.660000
r85/U1_B_505	NAND2	updated	15.660000
r85/U1_B_506	NAND2	updated	15.660000
r85/U1_B_507	NAND2	updated	15.660000
r85/U1_B_508	NAND2	updated	15.660000
r85/U1_B_509	NAND2	updated	15.660000
r85/U1_B_510	NAND2	updated	15.660000

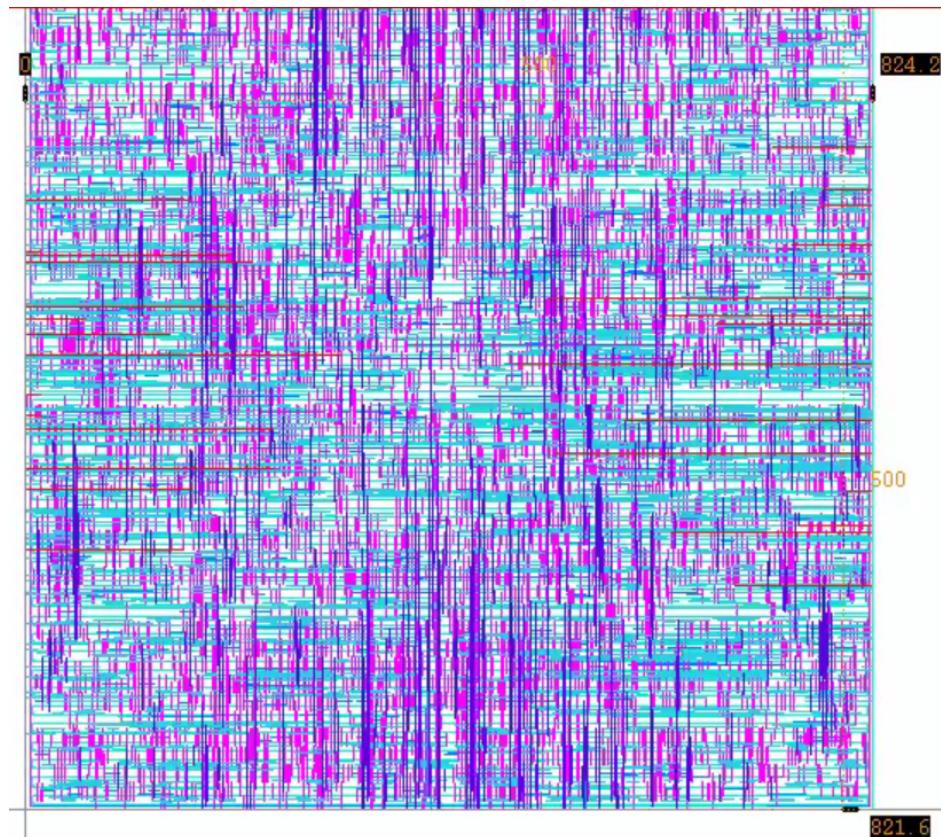
Total 12925 cells

273758.129824

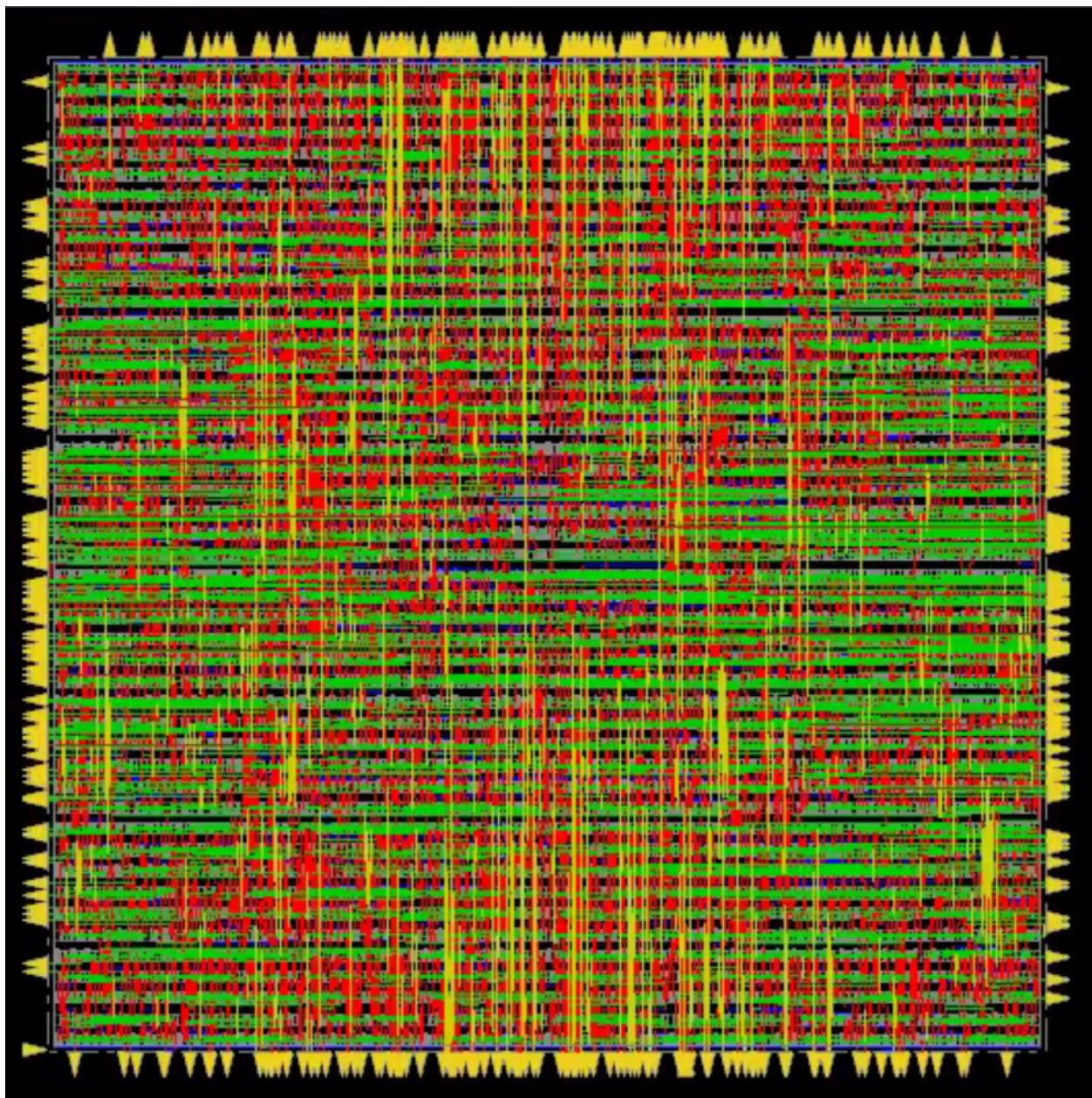
out_reg[459]	dff	library	7.000000	n
out_reg[460]	dff	library	7.000000	n
out_reg[461]	dff	library	7.000000	n
out_reg[462]	dff	library	7.000000	n
out_reg[463]	dff	library	7.000000	n
out_reg[464]	dff	library	7.000000	n
out_reg[465]	dff	library	7.000000	n
out_reg[466]	dff	library	7.000000	n
out_reg[467]	dff	library	7.000000	n
out_reg[468]	dff	library	7.000000	n
out_reg[469]	dff	library	7.000000	n
out_reg[470]	dff	library	7.000000	n
out_reg[471]	dff	library	7.000000	n
out_reg[472]	dff	library	7.000000	n
out_reg[473]	dff	library	7.000000	n
out_reg[474]	dff	library	7.000000	n
out_reg[475]	dff	library	7.000000	n
out_reg[476]	dff	library	7.000000	n
out_reg[477]	dff	library	7.000000	n
out_reg[478]	dff	library	7.000000	n
out_reg[479]	dff	library	7.000000	n
out_reg[480]	dff	library	7.000000	n
out_reg[481]	dff	library	7.000000	n
out_reg[482]	dff	library	7.000000	n
out_reg[483]	dff	library	7.000000	n
out_reg[484]	dff	library	7.000000	n
out_reg[485]	dff	library	7.000000	n
out_reg[486]	dff	library	7.000000	n
out_reg[487]	dff	library	7.000000	n

r85/U1_B_485	nand2	library	1.000000
r85/U1_B_486	nand2	library	1.000000
r85/U1_B_487	nand2	library	1.000000
r85/U1_B_488	nand2	library	1.000000
r85/U1_B_489	nand2	library	1.000000
r85/U1_B_490	nand2	library	1.000000
r85/U1_B_491	nand2	library	1.000000
r85/U1_B_492	nand2	library	1.000000
r85/U1_B_493	nand2	library	1.000000
r85/U1_B_494	nand2	library	1.000000
r85/U1_B_495	nand2	library	1.000000
r85/U1_B_496	nand2	library	1.000000
r85/U1_B_497	nand2	library	1.000000
r85/U1_B_498	nand2	library	1.000000
r85/U1_B_499	nand2	library	1.000000
r85/U1_B_500	nand2	library	1.000000
r85/U1_B_501	nand2	library	1.000000
r85/U1_B_502	nand2	library	1.000000
r85/U1_B_503	nand2	library	1.000000
r85/U1_B_504	nand2	library	1.000000
r85/U1_B_505	nand2	library	1.000000
r85/U1_B_506	nand2	library	1.000000
r85/U1_B_507	nand2	library	1.000000
r85/U1_B_508	nand2	library	1.000000
r85/U1_B_509	nand2	library	1.000000
r85/U1_B_510	nand2	library	1.000000
<hr/>			
Total 9587 cells			17261.000000

Placement and Routing:

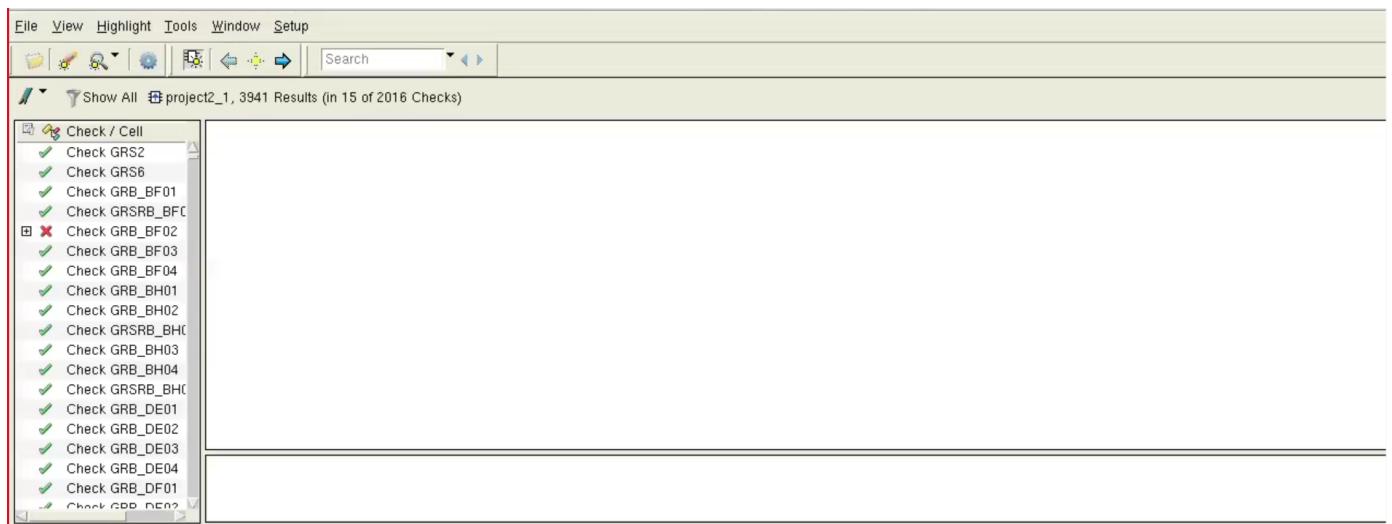


Layout View with measurements:

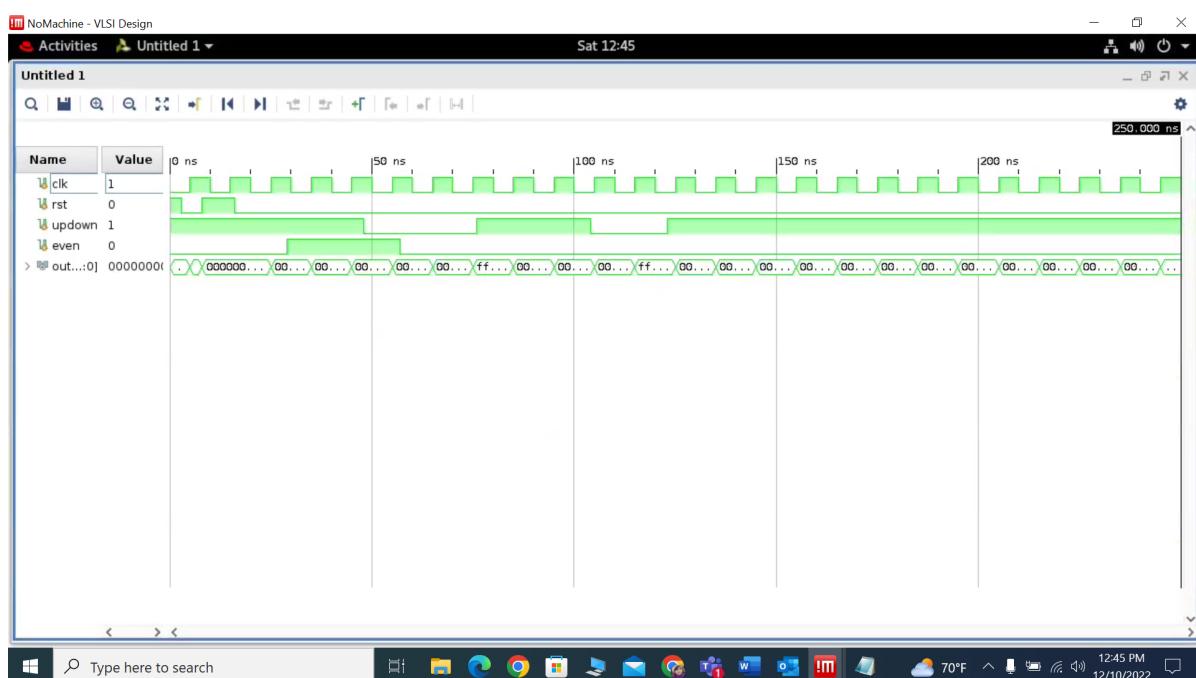


SIMULATION AND TESTING:

DRC Check - Zero DRC Errors:



Simulation Waveforms:



Static Time Analysis - Prime time:

U7027/A (NOR2)	0.14	0.00	67.80 f
U7027/C (NOR2)	0.01	0.48	67.89 r
U9717/A (NAND2)		0.48	67.89 r
U9717/C (NAND2)	0.01	0.13	68.02 f
U7805/B (XOR2)		0.13	68.02 f
U7805/C (XOR2)	0.00	0.11	68.12 f
U440/A (NAND2)		0.11	68.12 f
U440/C (NAND2)	0.00	0.04	68.17 r
U439/B (NAND2)		0.04	68.17 r
U439/C (NAND2)	0.00	0.03	68.21 f
U438/C (AOI21)		0.03	68.21 f
U438/OUT (AOI21)	0.00	0.04	68.24 r
U437/B (NAND2)		0.04	68.24 r
U437/C (NAND2)	0.00	0.03	68.27 f
out_reg[511]/D (dff)		0.03	68.27 f
data arrival time			68.27
clock clk' (fall edge)	0.00	70.00	70.00
clock network delay (ideal)		0.00	70.00
clock reconvergence pessimism		0.00	70.00
out_reg[511]/CLK (dff)			70.00 f
library setup time		-0.04	69.96
data required time			69.96
data required time			69.96
data arrival time			-68.27
slack (MET)			1.68

Worst Case Delay : 68.27

clock clk' (fall edge)	0.00	0.00	0.00
clock network delay (ideal)		0.00	0.00
out_reg[511]/CLK (dff)	0.00	0.00	0.00 f
out_reg[511]/OUT (dff)	2.02	3.75	2.74 r
r85/U1_A_511/A (XOR2)		3.75	0.00
r85/U1_A_511/C (XOR2)	0.00	0.03	0.16
U10359/IN (INVERTER)		0.03	0.00
U10359/OUT (INVERTER)	0.00	0.02	0.02
U438/A (AOI21)		0.02	0.00
U438/OUT (AOI21)	0.00	0.02	0.04
U437/B (NAND2)		0.02	0.00
U437/C (NAND2)	0.00	0.02	0.02
out_reg[511]/D (dff)		0.02	0.00
data arrival time			2.98
clock clk' (fall edge)	20.00	0.00	0.00
clock network delay (ideal)		0.00	0.00
clock reconvergence pessimism		0.00	0.00
out_reg[511]/CLK (dff)			0.00 f
library hold time		1.29	1.29
data required time			1.29

data required time			1.29
data arrival time			-2.98

slack (MET)			1.68

Design : project2_1
 Version: 0-2018.06-SP1
 Date : Sat Dec 10 11:47:34 2022

Attributes

i - Including register clock pin internal power
 u - User defined power group

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
clock network	6.417e-06	4.646e-05	2.007e-09	5.287e-05	(8.96%)	i
register	3.435e-05	3.975e-04	1.167e-07	4.320e-04	(73.20%)	
combinational	5.356e-05	5.131e-05	4.090e-07	1.053e-04	(17.84%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
Net Switching Power	= 4.953e-04		(83.93%)			
Cell Internal Power	= 9.433e-05		(15.98%)			
Cell Leakage Power	= 5.278e-07		(0.09%)			

Total Power	= 5.902e-04		(100.00%)			

TRADEOFFS AND CONCLUSION:

Currently, Our cell height is 8.606um which can be reduced furthermore. In the same way the pin pitch can be reduced by choosing a lower value of n.

Conclusion:

The 256 Bit Even/Odd Up-down Counter cell library is designed we can say that the Up-down Counter has met all the specifications