AN48399

WirelessUSB™ LP/LPstar Transceiver PCB Layout Guidelines

Author: Dave Amaranto, Mahesh Kiwalkar

Associated Project: No

Associated Part Family: WirelessUSB™ LP/LPstar Transceiver (CYRF6936,CYRF6986)

Software Version: None

Related Application Notes: AN48610

Abstract

AN48399 provides guidelines for PCB layout design and manufacture of the WirelessUSB™ LP/LPstar transceiver chip. These recommendations help in saving time and money in the development of an integrated wireless solution, by avoiding costly layout changes late in the design cycle. There is also an increased robustness through reduction in power supply noise, receiver sensitivity degradation, crystal pulling, and antenna detuning.

Introduction

The recommendations in this application note helps you in saving time and money in the development of an integrated wireless solution, by avoiding costly layout changes late in the design cycle. The recommendations are described in the following sections:

- Power Supply
- Ground
- Crystal
- Matching Network
- Antenna
- Manufacturing Considerations
- Test Points

Power Supply

The WirelessUSB LP/LPstar chip can be designed to operate from either an “unlimited” power supply or a battery power supply. The power supply type is dependent on the resources available to the device in the target application and determines the amount of power supply noise. Power supply noise can significantly degrade the analog performance of the radio chip.

External components are used to filter out noise. The configuration and values of these external filters may vary depending on the design of the power subsystem. The recommended components are discussed in the WirelessUSB LP/LPstar datasheet and Technical Reference Manual. Proper power bus trace routing and placement of vias and decoupling capacitors are irrespective of power subsystem design variations.

Power supply trace routing must be implemented keeping noisy power traces away from sensitive RF pins (10 to 13) and matching network components, as shown in Figure 1 and Figure 2.

Figure 1. Power Bus Routing

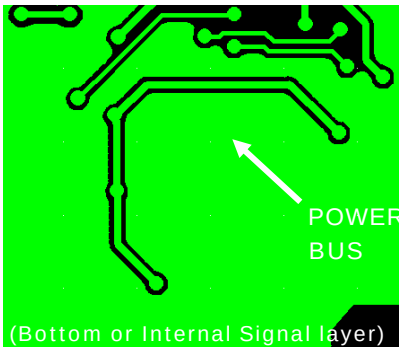
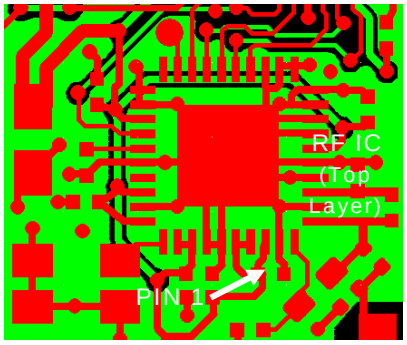
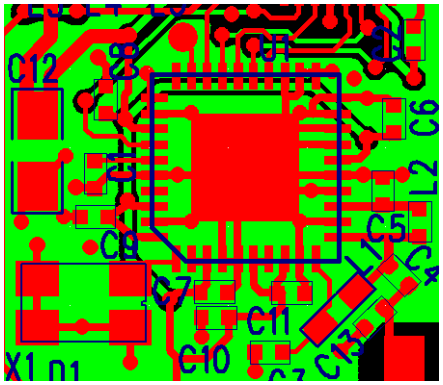


Figure 2. Chip Placement and Orientation



Most of the power bus is routed on the bottom layer with the rest of the area covered by GND pour. In a 4-layer design, the internal layer farthest from the RF IC's layer must be used for signal routing and is the best place to route this power bus. After the power bus and chip orientation are laid out, best design practices place low ESR decoupling capacitors on the same layer as the radio IC as close to its pins as possible. This brings power up from the power bus through vias. The parasitic inductance associated with vias helps to provide isolation between the power bus and the IC pin and decoupling capacitor node. It is also important to place these vias between the decoupling capacitor's pad and its associated power pin. However, due to board size constraints it may be useful to place the vias directly under the capacitor's pad. Figure 3 shows how decoupling capacitors (C6, C8, C9, C7, C10/C11) isolate power for pins (16, 33, 38/40, 3, 6/7/8) respectively. This implementation is a star distribution of power, in contrast to a series (homerun) distribution. Series distribution delivers power to all power pins though a long meandering trace, which is undesirable because it couples noise between different blocks of silicon.

Figure 3. Decoupling Capacitor and Vias Placement



A good power supply routing and properly designed power supply filters improves overall system performance by maximizing output power and receiver sensitivity.

Ground

Ground layout is extremely critical to the success of any radio design. Ground is more significant in 2.4 GHz analog designs than in common digital designs. Radio best practices implement ground as a key subsystem with the goal of providing an ample and uninterrupted return path. Its layout can no longer be an afterthought of what to do with excess board area. Due to the variety of board sizes and components used in different designs, there are no "copy exact" solutions for ground layout strategies. However, some fundamentals can be followed to achieve a successful radio design. Designs with better ground layouts have better manufacturing yields. Conversely, it is very difficult to achieve satisfactory manufacturing yields without implementing an effective ground layout.

2-Layer verses 4-Layer

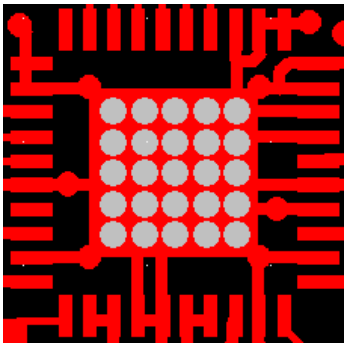
Cypress strongly recommends using 4-layer PCBs on any radio design. The 4-layer designs should use the following layer stack up to free area on the external layers. This provides substantial top and bottom ground copper pours.

- **Top** (Components: Radio IC, crystal, decoupling capacitors, matching network components, and antenna)
- **Internal 1** (GND Plane)
- **Internal 2** (V_{CC} Plane)
- **Bottom** (Components: Miscellaneous)

E-Pad

The E-pad is a metal ground paddle connection underneath the chip. Best practices recommend having a corresponding pad on the radio IC's PCB footprint that overlays an array (for example: 3x3, 5x5) of evenly distributed standard 12 and 25 vias. Figure 4 illustrates a 5x5 via array. These vias provide a substantial connection to the bottom ground copper pour (and to an internal GND plane layer in a 4-layer design), which contributes to the overall ground layout strategy.

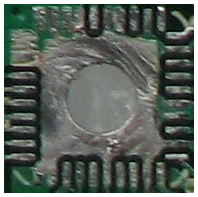
Figure 4. E-Pad Via Array



Remember to keep this area free from solder mask as that prevents the metal on the RFIC from forming a solder connection to the ground copper on the PCB. Figure 5 and Figure 6 are examples of both bad and good E-pad solder masking. Both images have an inspection hole in the E-pad used to visually inspect the solder connection. This technique is good for initial manufacturing builds. However, it compromises the function of providing a solid ground connection and should be eliminated for mass production.

Figure 5. Bad E-Pad Solder Mask

Figure 6. Good E-Pad Solder Mask (Reworked)



External Layer Copper Pours

Another important ground connection to consider is the one between the E-pad and top copper pour. Figure 7 shows a good top copper pour and E-pad connection. Both top and bottom copper pours should provide an ample return path to the power supply's negative connection, either the GND pin on a connector or negative battery. Figure 7 and Figure 8 are examples of substantial copper pours.

Figure 7. Substantial Top Copper Pour

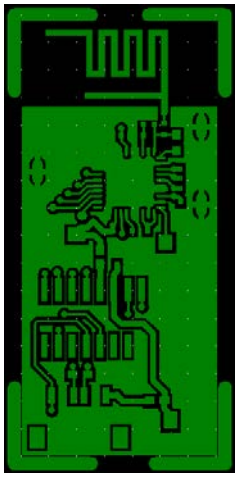
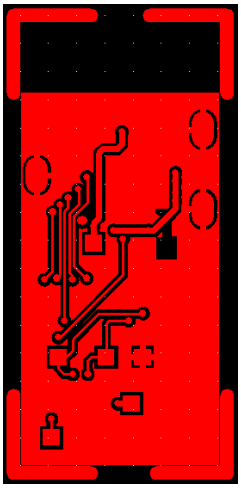


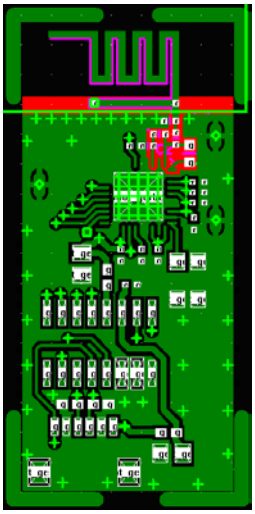
Figure 8. Substantial Bottom Copper Pour



Via Stitching

The top and bottom layer copper pours provide an uninterrupted return path. This is maximized by the distribution of ground vias connecting the two layers. The internal ground plane of 4-layer designs also provide uninterrupted return path by connecting areas of copper that may otherwise be islands that do not contribute to the return path. The term "via stitching" describes the practice of placing evenly spaced vias around the board. Figure 9 shows a good distribution of ground vias with each via marked by a '+'. The row of more densely distributed vias along the top edge of the board is the applied antenna ground and is required to maximize the RF performance of the device.

Figure 9. Via Stitching



Manufacturing

A successful ground strategy does not end with a properly implemented E-pad via array, good external layer copper pours, and ample via stitching. Careful consideration of stencil design, selection of solder paste type, and reflow profile is required because they play a major role in system ground performance. The manufacturing process establishes the quality of the solder connection between the radio IC's paddle and the board's ground return path. This can be a fundamental bottle neck between the radio chip's silicon die and power supply's negative connection. Figure 10, Figure 11, and Figure 12 show X-rays of varying E-pad solder connection quality.

A moderate quality E-pad solder connection can cause receiver sensitivity degradation, especially at temperature extremes. This malfunction can also be indicative of a PCB's inadequate ground layout, manufactured with a good quality E-pad connection. Moderate quality connections have voids and micro-fractures that are seen by X-ray or CSAM analysis. Figure 11 shows moderate voiding.

A poor quality E-pad solder connection can cause yields to experience high rates of total failures and intermittently failing devices. Poor quality connections have excessive voids, micro-fractures, and cold solder joint that are seen by X-ray or CSAM analysis. Figure 12 shows excessive voiding and Figure 13 is a photograph of a PCB with the radio IC removed to show solder paste that is still in the stencil's 3x3 array. This is physical evidence of an inadequate reflow profile. It occurs because the solder paste underneath the chip did not achieve its time above liquid (TAL) or minimum peak temperature, recommended specifications by the solder paste manufacturer that must be met to form a good solder connection. QFN pads require more time and temperature to heat up. Therefore, special attention must be paid to thermocouple placement when measuring the profile.

Figure 10. X-Ray of Good E-Pad Solder Connection

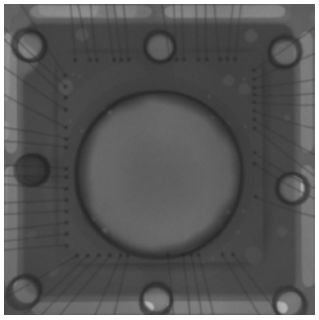


Figure 11. X-Ray of Moderate E-Pad Solder Connection

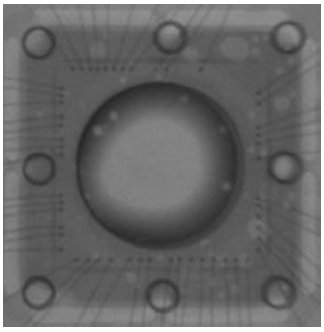


Figure 12. X-Ray of Poor E-Pad Solder Connection

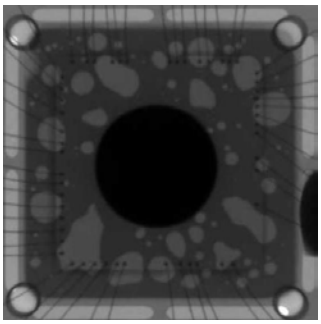
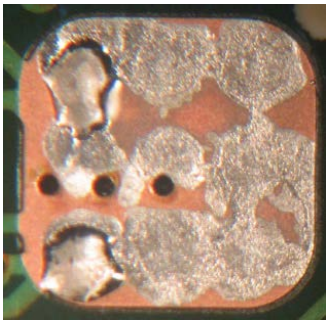


Figure 13. Photo of Solder Paste Remains due to Inadequate Reflow Profile (Radio IC Removed)



Note that inadequate reflow can also lead to residual material left on the board, particularly with no-clean solder pastes. This can cause problems in RF designs.

Lead Free Manufacturing

The move to lead free materials also affects the overall manufacturability of the design. Although many vendors have converted or are in the process of converting to Pb-free, some assembly houses are still learning to overcome the challenges. Two significant concerns of Pb-free manufacturing are: Pb-free solders have a reduced whetting force relative to previous tin-lead alloys and they require a higher reflow temperature.

The reduced whetting force means that the solder does not pull up strongly onto the adjacent metal surfaces. It has a higher tendency to stay in the same position, in which it was placed on the PCB through the solder stencil. This behavior can lead to several potential defects, including:

- Inadequate coverage of pads.
- The IC may not sit level on the PCB, particularly for ICs with large center pads, resulting in increased defects for some of the perimeter leads.
- Parts not aligned well when placed are less likely to self-align during reflow.
- Higher potential for bridging between adjacent pins (solder is not wicked away from the gap and onto the leads as readily).
- Inadequate fill of plated through-holes.
- Fillets may not properly form around leads.

Higher reflow temperatures mean more work by assembly houses to tune their process, given their well established leaded flows. Hand rework of functional line failures, a common practice for yield recovery of minor defects, can be less successful. The number of overall rework attempts that a board can tolerate is also reduced.

Moving to Pb-free is unavoidable, so being aware of and proactive to the pitfalls is critical. Solutions to these problems require early engagement with the assembly house, careful selection of materials, adherence to solder paste manufacturer recommendations, close monitoring of the early manufacturing builds, and retuning of the process as yields are evaluated in mass production.

Manufacturing analog RF products requires a tighter adherence to process related variations than high speed digital or standard analog products. Pb-free processes have special challenges that also require additional attention to establish a reliable and robust process.

Crystal

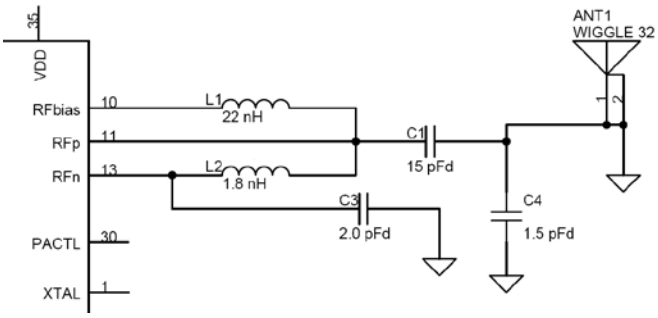
Best practices place the crystal on the same side of the PCB as the radio chip and as close to the XTAL pin (1) as possible. If the board size permits, avoid the following: placing the crystal directly underneath matching network and antenna traces, placing the crystal physically close to any known noise sources, long meandering trace paths, and the use of vias.

On multilayer PCBs it is important to void any internal layers directly beneath the active crystal pad and trace to avoid parasitic capacitance. Parasitic capacitance produces load capacitance, thus “pulling” the oscillator slower and possibly out of the ±30 ppm tolerance of the radio chip.

Crystal layouts should be as close to identical as possible for all radios in the system. By keeping layouts identical, the crystal’s load capacitance is similar for each radio in the system.

Matching Network

Figure 14. Matching Network Schematic for CY6936



As shown in Figure 14, RFp and RFn are the differential output impedance pins on the WirelessUSB LP radio. A component matching network connects these pins to the antenna. Because the RFp and RFn pins connect to the antenna, it is important that the matching network transforms the impedances at the RFp and RFn pins to match the input impedance of the antenna to increase transmission and reception range. Details of the measured impedances at the RFp and RFn pins of the WirelessUSB LP radio for single ended and differential modes are found in application note AN48610.

For LPstar, see the application example or reference design for the matching network schematic details.

Primary functions of this matching network are as follows:

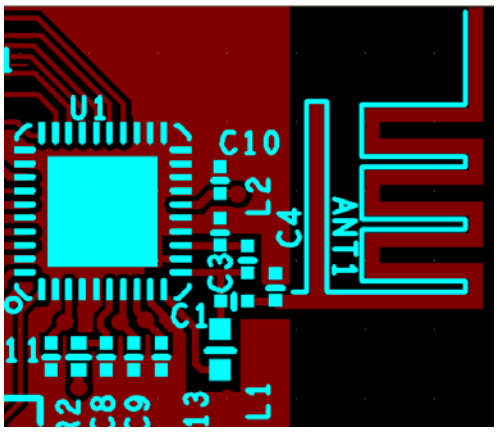
- **50 Ohm Match:** Efficiently matches radio chip output impedance to the antenna input impedance, thereby providing efficient TX power output to antenna and acceptable RX sensitivity.
- **Balun:** Acts as the balun, transforming the balanced radio chip output to the unbalanced antenna.
- **DC Blocking:** Blocks DC from getting to the antenna output.
- **Harmonic Suppression:** Rejects harmonics and out of band emissions to meet regulatory compliance testing.

The antenna matching network element values are selected by optimization simulations. All the matching components are made from the same package size to mount on 0402 pads. The placement of these components and the dimensions of the transmission lines used in this network play a significant role in its impedance. The

recommended placement of these elements is shown in Figure 15 and Figure 16.

Figure 15. Matching Network Layout on CY3630M Module

Figure 16. Matching Network Layout

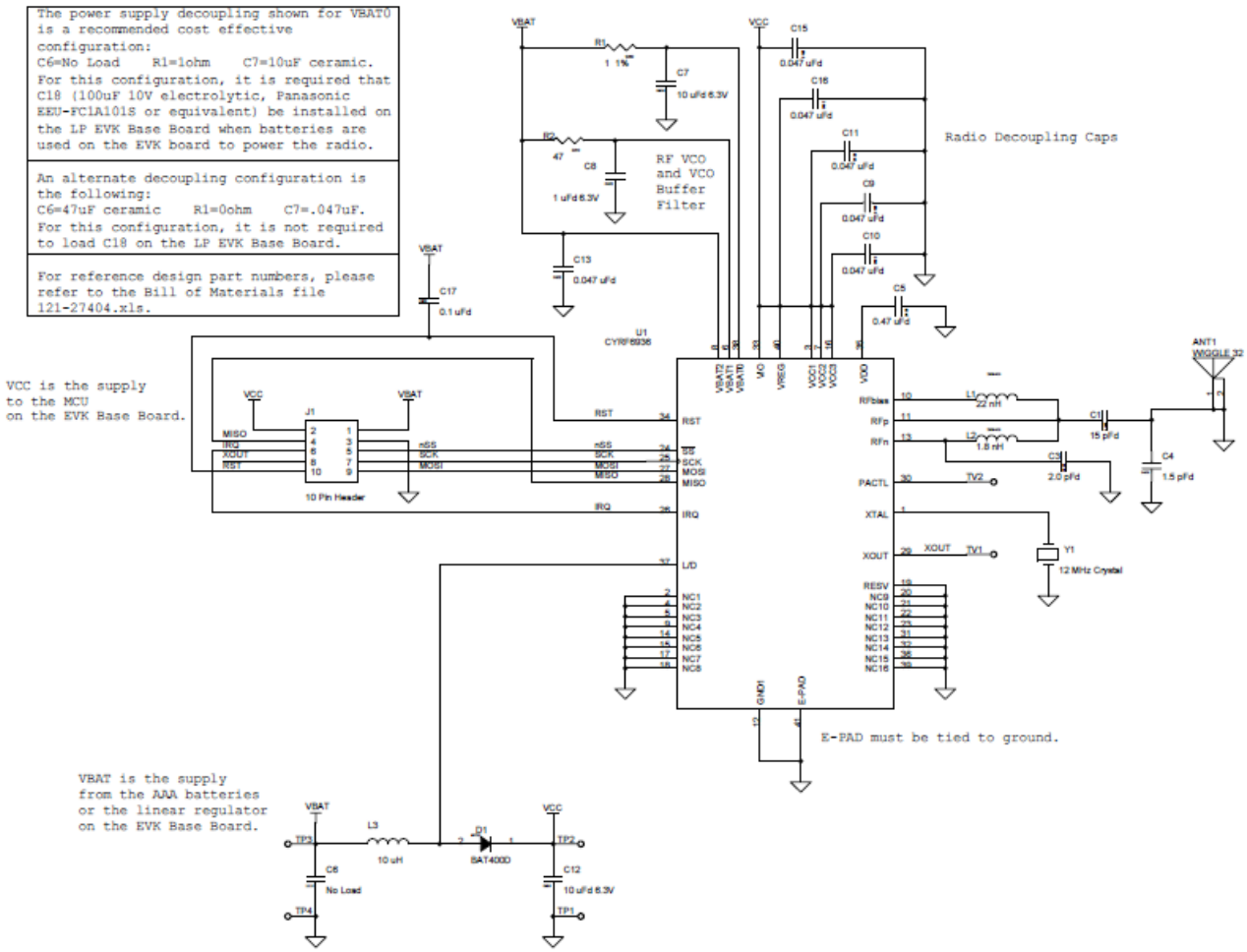


Matching network on the Cypress reference design boards are designed such that impedance looking at the junction of C1 and C4 is approximately matched to 50 ohms at 2.4 GHz. This measurement can be made on a network analyzer using an SMA connector at the junction of C1 and C4. Cypress provides the CY3630M SMA module for this purpose. This also permits using an external antenna as long as its input impedance is matched to 50 ohms.

Some of the recommendations that Cypress makes on the matching network layout to optimize RF board performance are as follows:

- Limit the number of signal vias in the matching network path as they add unaccounted inductance to the circuit.
- In contrast, use a large number of vias to tie the front and backside ground plane regions together along the antenna. This is known as applied antenna ground and is illustrated in Figure 9.
- Refrain from placing the crystal under the matching network – antenna section. This contributes to unnecessary sideband noise or noise coupling from the antenna back into the PLL and VCO circuitry.
- Make sure that the components which connect to ground do not have any isolated GND islands.
- Orient the chip in the layout such that the RF input and output pins are closest to the antenna. Running longer traces affect the impedance of the network.
- Use shortest path traces between components in the matching network.
- Avoid sharp bends in the traces – use standard straight line connections, 45 degree bends, and 90 degree bends, in that order.

Schematics of CY3630M

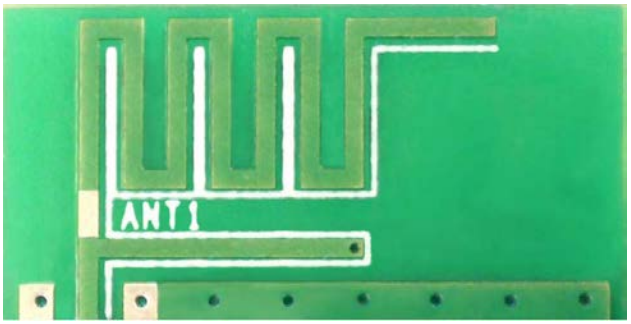


Antenna

One of the most important tasks in designing short range radio data communication system is antenna design. The key parameters for antenna design are the antenna size, cost of implementation, radiation effectiveness, ease of manufacturability, and range performance. A properly designed antenna facilitates the evaluation, characterization, and production test correlation of the WirelessUSB LP/LPstar radio.

The primary functions of an antenna are to provide the transfer of electromagnetic energy to and from the atmosphere and match the impedance of the transmission line feed (typically 50 ohms) and the impedance of free space (377 ohms). The selection of the antenna for a WirelessUSB solution has a big impact on wireless communication system performance, system form factor, and cost.

Figure 17. PCB Wiggle Antenna



An antenna essentially provides a means of converting electrical energy into electromagnetic waves for transmission and reconverting the electromagnetic waves into electrical energy for reception. There are several properties of the antenna that affect the performance of wireless communication systems using the Cypress

WirelessUSB system radio chip. This application note describes design considerations and implementation guidelines pertaining to a printed trace wiggle antenna for incorporating the WirelessUSB radio system chip into product applications in the ISM frequency band 2.4 to 2.5 GHz. These recommendations have been tested and proven by Cypress Semiconductor to ensure optimal radio performance when combining RF analog circuitry with other low frequency analog and digital board components.

The radio module printed circuit board is implemented on a two-layer board using low cost FR-4 material. The picture of the wiggle antenna as implemented on Cypress reference radio module is shown in Figure 17.

The antenna is implemented as a wiggle PCB trace on the top component side of the PCB. The ground plane underneath the wiggle trace (along the entire length of the antenna) must be removed from the backside of the PCB. The suggested antenna design requires no more than 435 x 280 mils of space. Details of the antenna design are shown in Figure 18.

Layout Recommendations

Some of the recommendations that Cypress makes on the antenna layout to optimize RF performance are as follows:

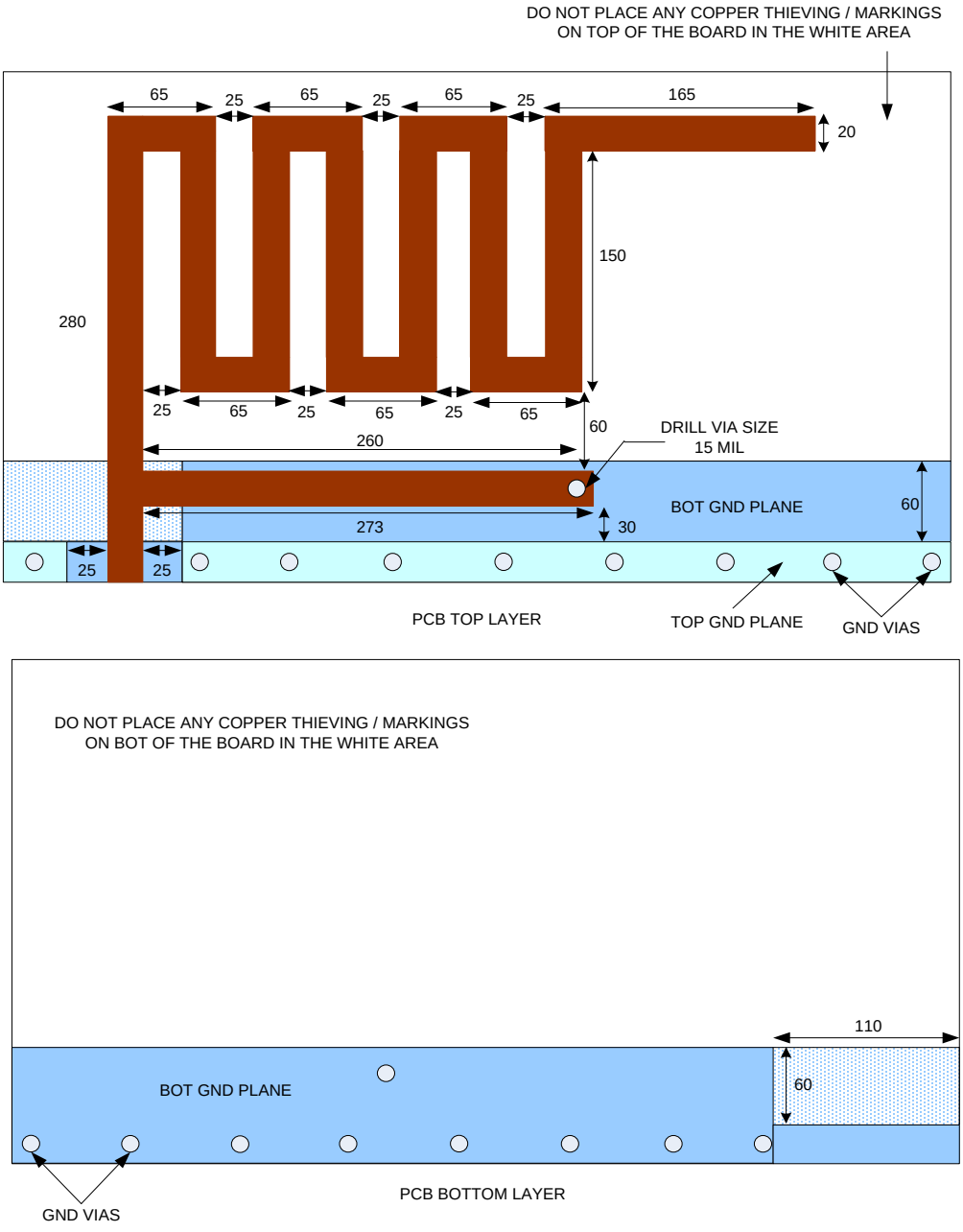
- Do not place components or ground plane near the tip of the antenna. This is because the coupling of the antenna radiation to ground reduces the effective range of operation.
- For a multilayer board, there should not be any ground plane near the tip of the antenna on any of the layers.
- The horizontal stub, which runs to ground with the GND via is instrumental in increasing the return loss of the antenna.
- Antenna tip length can be changed to optimize the antenna design for different board thickness.
- Avoid in-circuit test pins on RF nodes as they create small antennas and may result in possible FCC issues and degrade RF performance.
- Large, continuous ground plane surfaces provide better radiation performance than small surfaces.

Note Details of the wiggle antenna's dependence on PCB thickness and measured antenna radiation patterns are found in the application note, AN48610.

The thumb rules for antenna selection and implementation are as follows:

- Do not use any form of EMI and RFI shield coatings on plastic housing to solve EMI problems without considering the effect of shielding on antenna placement and location.
- Eliminate connectors and interconnect transmission lines to avoid insertion loses on transmit power and receive sensitivity on the receiver.
- Product applications using keypads, LCD or other types of displays, battery packs, and other metallic surfaces affect and degrade the symmetry of the radiation pattern, reflections, and multipath. Therefore, the location of the antenna placement is critical. Place the antenna to balance the distribution of these objects.
- When using an external antenna, if you connect the antenna with a coaxial cable assembly, the cable routing must be kept away from motors and battery packs.
- The orientation of the device and the product usage model during the operation should be considered in mounting the antenna inside the device.
- Note that the performance of the antenna depends on its immediate surroundings, packaging, and proximity to the ground plane. The placement of antenna position should be identified early in the design process.
- The effects of human body and the operator's hand should be examined and validated away during the product operation. By keeping the antenna away, the Specific Absorption Rate (SAR) is reduced and pattern symmetry is improved.

Figure 18. Wiggle Antenna Layout Information



Test Points

Test points provide access to signals that require monitoring in manufacturing or bench test environments.

Cypress strongly recommends placing test points on the following signals (in order of priority):

- XOUT
- SPI Bus (SCK, MISO, MOSI, nSS)
- RST
- IRQ
- PACTL (Only for LP)
- V_{CC}, $V_{BAT,}$ and GND

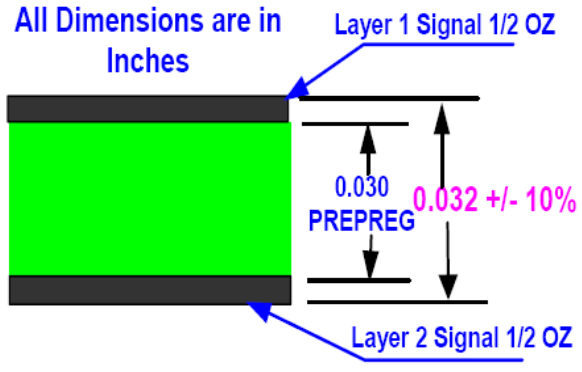
Cypress recommends NEVER placing test points on the following signals:

- XTAL
- RF_{BIAS}, RF_P, and RF_N
- Any Matching Network Trace
- Antenna

Manufacturing Considerations

PCB designers provide manufacturers with detailed instructions on how a printed circuit board must be constructed. This includes information on material, thickness, and international standards to be followed. These instructions are typically provided in the Fabrication Notes.

Figure 19. PCB Stack Up Details



The following are some Cypress specifications for a two-layer printed circuit board for use with the WirelessUSB radio:

- Material
  - Type FR-4 epoxy glass laminate and prepreg
  - HTE Copper 0.5 oz copper foil external layers
  - Overall metal-to-metal thickness 0.0032 inches ± 10%
- Drilling
  - Diameters in the drill table are finished hole sizes ± 0.003 inch tolerance, unless otherwise specified in the drill table
  - Teardrop allowed on entry of via on every trace layer
- Copper plating
  - In through-holes 0.001 inches minimum
- Silkscreen
  - In white nonconductive epoxy ink on both sides of board, if applicable.
- Solder mask
  - Primary and secondary side of board using liquid photo image mask material over bare copper per IPC-SM-840
- Copper finish
  - Tin or gold plated (10 µ inch minimum)
- Manufactured boards
  - In accordance with performance standard IPC-6011/6012 Class-2 board to be inspected according to IPC-600-A Class-2
- Maximum wrap or twist
  - Must not exceed 0.01 in/in

References

- WirelessUSB LP Datasheet
- WirelessUSB™ LPstar 2.4 GHz Radio SoC
- WirelessUSB™ LP/LPstar and PRoC™ LP/LPstar, Technical Reference Manual
- AN48610 - Design and Layout Guidelines for Matching Network and Antenna for WirelessUSB™ LP Family

Document History

Document Title: WirelessUSB™ LP/LPstar Transceiver PCB Layout Guidelines - AN48399

Document Number: 001-48399

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2625047	DVJA	12/19/08	New Application Note
*A	3130920	CSAI	01/18/2011	Added Schematics of CY3630M.
*B	3248342	KKCN	05/04/2011	Updated the text with LPstar.
*C	3333756	KPMD	08/01/2011	Post to external web.
*D	3503545	CSAI	01/20/2012	Updated template No technical updates

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical Navigation Sensors	cypress.com/go/ons
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/usb
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

Phone : 408-943-2600
Fax : 408-943-4730
Website : www.cypress.com