

# Multi-Channel GPS/GLONASS/Galileo/BeiDou/IRNSS/QZSS S/L1/L2/L3/L5 band RF Front End

## 1. OVERVIEW

NT1066 is a 4-channel RF Front End (3 wideband IQ and 1 narrowband IQ) that covers all GNSS (GLONASS, GPS, Galileo, BeiDou, QZSS, IRNSS) signals at all frequency bands. It makes possible to benefit from all the advantages of acquiring multiple system simultaneously. Channels “A”, “B” and “C” are designed with single conversion low-IF architecture, individually programmable and intended to receive L1, E1, B1, E6, B3, L2, L3, B2, L5, E5 in various combinations. IQ and image suppression modes are available, other options can be discovered in feature list. Channel “D” is dedicated to operate on S band of IRNSS or L2, L3, L5 bands of GNSS and has zero-IF architecture. This special addition makes possible to effectively eliminate ionospheric distortion utilizing large signal base of IRNSS between L5 and S bands. As alternative, channel “D” can be ‘on a fly’ software-reconfigured to receive real-time corrections data transmitted over FM, VHF and UHF bands.

NT1066 does also integrate 4 fractional-N synthesizers that have the common reference (TCXO) input making LO signals coherent in terms of frequency. Wide list of attractive features and high level of customization make NT1066 capable to meet a demand of researchers and OEM developers in special applications: high precision positioning, goniometric, driverless car systems, professional drones and related areas.

## 2. FEATURES

### Overall

- 4 independent, fully customizable IQ channels
- 4 coherent fractional-N PLLs with fully integrated VCOs and autotuning system
- Clock output for correlator with programmable frequency, amplitude and DC level
- Pass-through TCXO reference signal output
- Internal or external sampling frequency for 2-bit ADCs
- 4-wire SPI interface with user friendly registers map
- Individual status indicators of main subsystems (available in SPI registers) and cumulative status indicator (AOK, available both as a separate pin and in SPI registers)
- Embedded temperature sensor
- 12x12mm QFN108 package

### Channels “A”, “B” and “C” feature list:

- Single conversion super heterodyne architecture for L1, L2, L3, L5 bands of GNSS signals reception
- Active antenna detector system including short-protection circuit
- Tunable signal bandwidth up to 60MHz (up to 30MHz of IF BW with autocalibration system)
- IF AGC system or manually programmable gain
- Configurable output type: complex or real with separate upper and lower sideband
- Analog differential output or 2-bit ADC digital output with programmable output logic high level

### Channel “D” feature list:

- Direct conversion architecture with IQ data output for S band of IRNSS or L2, L3, L5 bands of GNSS signals reception or FM 65...110 MHz, VHF 160...240 MHz, UHF 470...862 MHz bands for DGPS data downloading
- Tunable signal bandwidth up to 22MHz (up to 11MHz of IF BW)
- Dual AGC system (RF + IF) or manually programmable gain
- Wide dynamic range with 1dB compression point up to +16 dBm
- Analog differential output or 2-bit ADC digital output with programmable thresholds and output logic high level respectively

### 3. DESCRIPTION

#### 3.1. BLOCK DIAGRAM

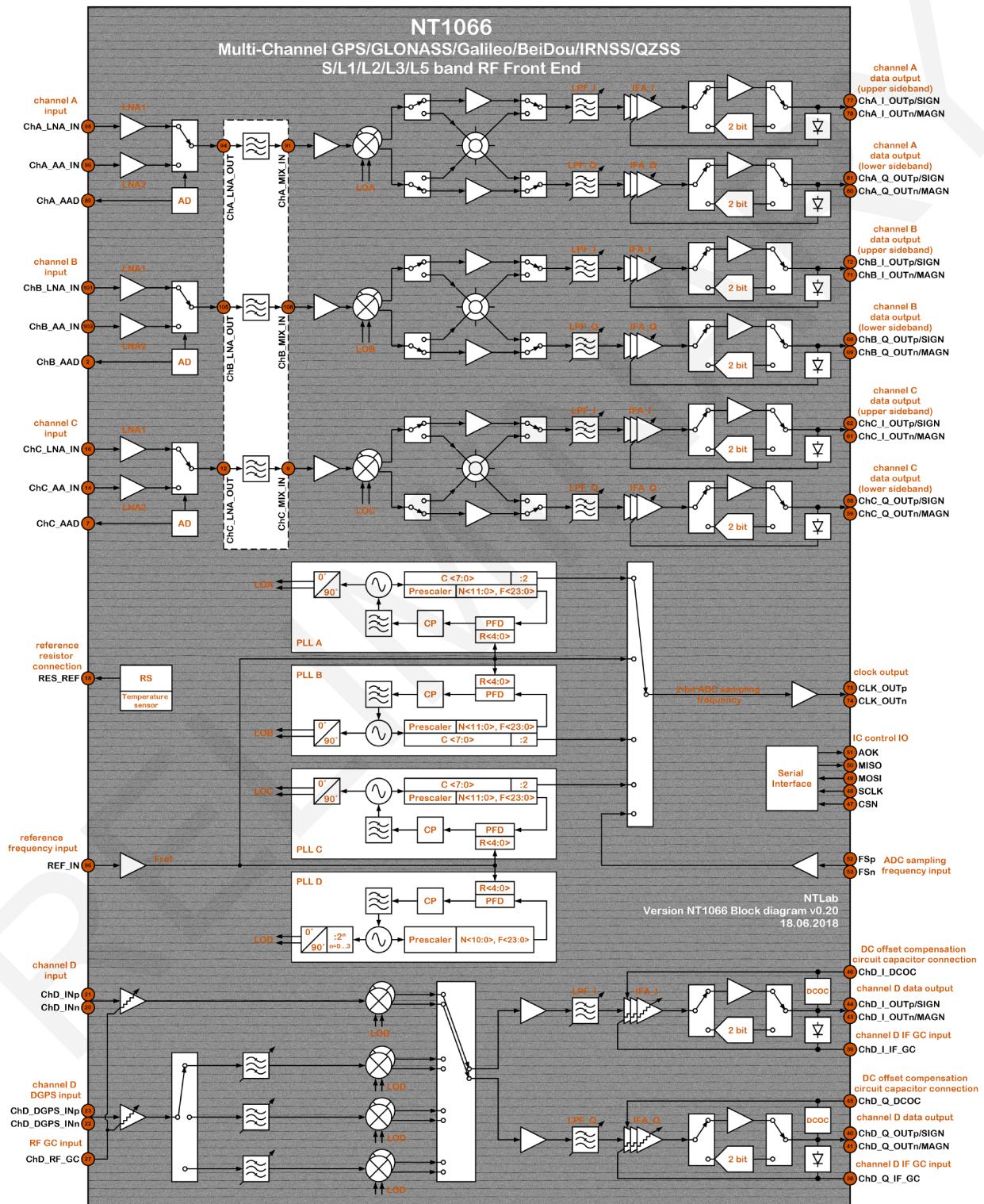


Figure 3.1: NT1066 Block diagram

### 3.2. APPLICATION SCHEMATIC

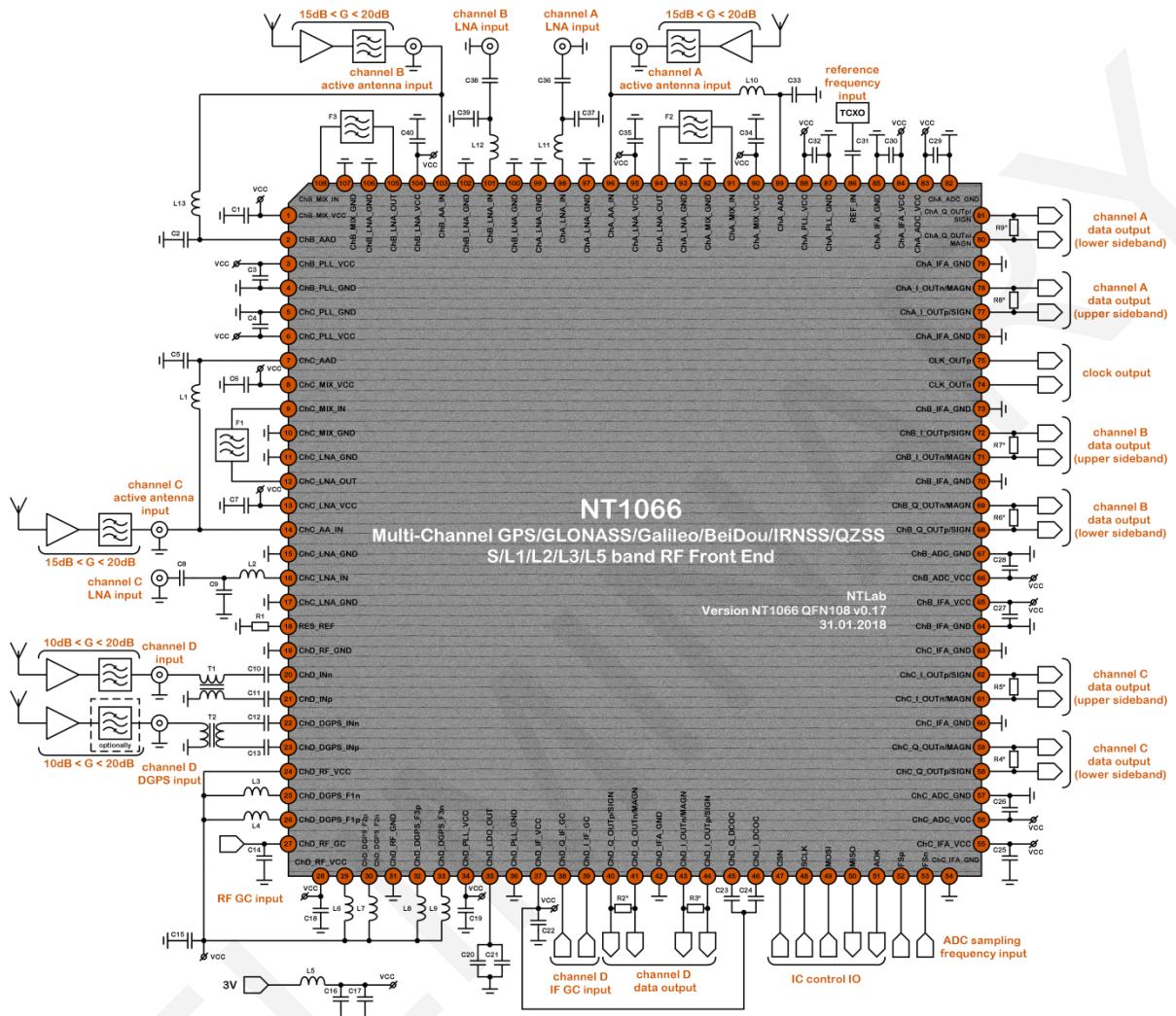


Figure 3.2: NT1066 Application schematic

Table 3.1: External component description

Component	Nominal value	Tolerance	Notes
C1	100nF	±10%	Supply voltage filter capacitor
C2	1nF	±10%	Filtering capacitor
C3	100nF	±10%	Supply voltage filter capacitor
C4	100nF	±10%	Supply voltage filter capacitor
C5	1nF	±10%	Filtering capacitor
C6	100nF	±10%	Supply voltage filter capacitor
C7	100nF	±10%	Supply voltage filter capacitor
C8	18pF	±10%	DC blocking capacitor
C9*	1.3pF	±5%	Matching network capacitor for L1 band
	1.8pF	±5%	Matching network capacitor for L3, L3, L5 bands
C10	100pF	±5%	Blocking capacitor
C11	100pF	±5%	Blocking capacitor
C12	220pF	±5%	Blocking capacitor
C13	220pF	±5%	Blocking capacitor
C14	10nF	±10%	RF AGC capacitor
C15	100nF	±10%	Supply voltage filter capacitor
C16	10nF	±10%	Supply voltage filter capacitor

<b>Component</b>	<b>Nominal value</b>	<b>Tolerance</b>	<b>Notes</b>
C17	10uF	$\pm 10\%$	Supply voltage filter capacitor
C18	100nF	$\pm 10\%$	Supply voltage filter capacitor
C19	100nF	$\pm 10\%$	Supply voltage filter capacitor
C20	1nF	$\pm 10\%$	LDO output filtering capacitor
C21	100nF	$\pm 10\%$	LDO output filtering capacitor
C22	100nF	$\pm 10\%$	Supply voltage filter capacitor
C23	4.7uF	$\pm 10\%$	X7R DCOC capacitor
C24	4.7uF	$\pm 10\%$	X7R DCOC capacitor
C25	100nF	$\pm 10\%$	Supply voltage filter capacitor
C26	100nF	$\pm 10\%$	Supply voltage filter capacitor
C27	100nF	$\pm 10\%$	Supply voltage filter capacitor
C28	100nF	$\pm 10\%$	Supply voltage filter capacitor
C29	100nF	$\pm 10\%$	Supply voltage filter capacitor
C30	100nF	$\pm 10\%$	Supply voltage filter capacitor
C31	1nF	$\pm 10\%$	Blocking capacitor
C32	100nF	$\pm 10\%$	Supply voltage filter capacitor
C33	1nF	$\pm 10\%$	Filtering capacitor
C34	100nF	$\pm 10\%$	Supply voltage filter capacitor
C35	100nF	$\pm 10\%$	Supply voltage filter capacitor
C36	18pF	$\pm 10\%$	DC blocking capacitor
C37*	1.3pF	$\pm 5\%$	Matching network capacitor for L1 band
	1.8pF	$\pm 5\%$	Matching network capacitor for L3, L3, L5 bands
C38	18pF	$\pm 10\%$	DC blocking capacitor
C39*	1.3pF	$\pm 5\%$	Matching network capacitor for L1 band
	1.8pF	$\pm 5\%$	Matching network capacitor for L3, L3, L5 bands
C40	100nF	$\pm 10\%$	Supply voltage filter capacitor
L1	56nH ( $Q \geq 40$ )	$\pm 5\%$	AC blocking inductor
L2*	6.8nH	$\pm 5\%$	Matching network inductor for L1 band
	11nH	$\pm 5\%$	Matching network inductor for L3, L3, L5 bands
L3	180nH ( $Q \geq 40$ )	$\pm 5\%$	Tracking filter inductor
L4	180nH ( $Q \geq 40$ )	$\pm 5\%$	Tracking filter inductor
L5	120Ω / 100MHz	$\pm 20\%$	Supply voltage filter inductor
L6	8.2nH ( $Q \geq 40$ )	$\pm 5\%$	Tracking filter inductor
L7	8.2nH ( $Q \geq 40$ )	$\pm 5\%$	Tracking filter inductor
L8	82nH ( $Q \geq 40$ )	$\pm 5\%$	Tracking filter inductor
L9	82nH ( $Q \geq 40$ )	$\pm 5\%$	Tracking filter inductor
L10	56nH ( $Q \geq 40$ )	$\pm 5\%$	AC blocking inductor
L11*	6.8nH	$\pm 5\%$	Matching network inductor for L1 band
	11nH	$\pm 5\%$	Matching network inductor for L3, L3, L5 bands
L12*	6.8nH	$\pm 5\%$	Matching network inductor for L1 band
	11nH	$\pm 5\%$	Matching network inductor for L3, L3, L5 bands
L13	56nH ( $Q \geq 40$ )	$\pm 5\%$	AC blocking inductor
R1	61.9kΩ	$\pm 1\%$	High precision resistor
R2*	1.5kΩ	$\pm 5\%$	Load resistor if analog differential output
	--Ω	-	DNP if 2-bit ADC output
R3*	1.5kΩ	$\pm 5\%$	Load resistor if analog differential output
	--Ω	-	DNP if 2-bit ADC output
R4*	510kΩ	$\pm 5\%$	Load resistor if analog differential output
	--Ω	-	DNP if 2-bit ADC output
R5*	510kΩ	$\pm 5\%$	Load resistor if analog differential output
	--Ω	-	DNP if 2-bit ADC output
R6*	510kΩ	$\pm 5\%$	Load resistor if analog differential output
	--Ω	-	DNP if 2-bit ADC output
R7*	510kΩ	$\pm 5\%$	Load resistor if analog differential output
	--Ω	-	DNP if 2-bit ADC output
R8*	510kΩ	$\pm 5\%$	Load resistor if analog differential output

Component	Nominal value	Tolerance	Notes
R9*	--Ω	-	DNP if 2-bit ADC output
	510kΩ	±5%	Load resistor if analog differential output
	--Ω	-	DNP if 2-bit ADC output
F1*	TA1104A	-	SAW filter for L3 and L5 band
F2*	TA1658A	-	SAW filter for L1 band
F3*	TA0871A	-	SAW filter for L2 band
T1	TC1-1-43A	-	Transformer
T2	MABA-007681-CT2010	-	Transformer

\* – defined depending on PCB construction and purpose

### 3.3. PINS DESCRIPTION

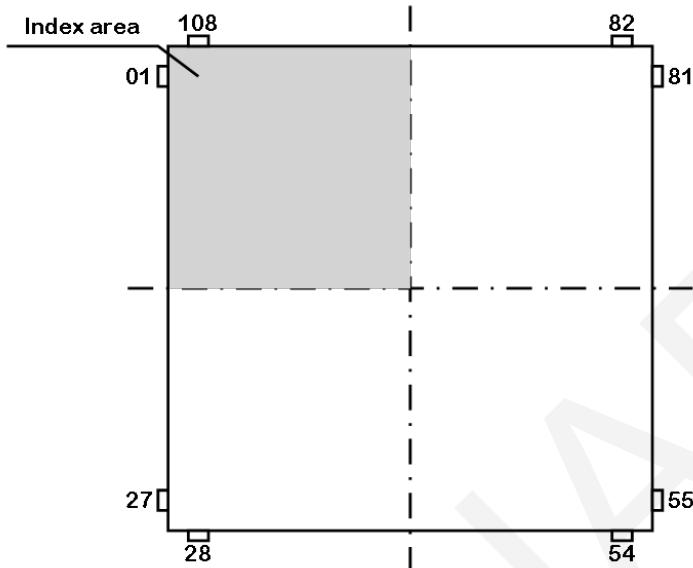


Figure 3.3: Pin configuration

Table 3.2: NT1066 pin description

#	Name	Description
1	ChB_MIX_VCC	Channel “B” mixer supply voltage
2	ChB_AAD	Channel “B” active antenna supply voltage output
3	ChB_PLL_VCC	Channel “B” PLL supply voltage
4	ChB_PLL_GND	Channel “B” PLL ground
5	ChC_PLL_GND	Channel “C” PLL ground
6	ChC_PLL_VCC	Channel “C” PLL supply voltage
7	ChC_AAD	Channel “C” active antenna supply voltage output
8	ChC_MIX_VCC	Channel “C” mixer supply voltage
9	ChC_MIX_IN	Channel “C” mixer input
10	ChC_MIX_GND	Channel “C” mixer ground
11	ChC_LNA_GND	Channel “C” LNA ground
12	ChC_LNA_OUT	Channel “C” LNA output
13	ChC_LNA_VCC	Channel “C” LNA supply voltage
14	ChC_AA_IN	Channel “C” active antenna input
15	ChC_LNA_GND	Channel “C” LNA ground
16	ChC_LNA_IN	Channel “C” LNA input
17	ChC_LNA_GND	Channel “C” LNA ground
18	RES_REF	External resistor for reference current source
19	ChD_RF_GND	Channel “D” RF ground
20	ChD_INn	Channel “D” analog input – complement
21	ChD_INp	Channel “D” analog input – true
22	ChD_DGPS_INn	Channel “D” DGPS analog input – complement
23	ChD_DGPS_INp	Channel “D” DGPS analog input – true
24	ChD_RF_VCC	Channel “D” RF circuits supply voltage
25	ChD_DGPS_F1n	Channel “D” FM tracking filter 1 load
26	ChD_DGPS_F1p	Channel “D” FM tracking filter 1 load
27	ChD_RF_GC	Channel “D” RF GC input

#	Name	Description
28	ChD_RF_VCC	Channel "D" RF circuits supply voltage
29	ChD_DGPS_F2p	Channel "D" UHF tracking filter 2 load
30	ChD_DGPS_F2n	
31	ChD_RF_GND	Channel "D" RF ground
32	ChD_DGPS_F3p	Channel "D" VHF tracking filter 3 load
33	ChD_DGPS_F3n	
34	ChD_PLL_VCC	Channel "D" PLL supply voltage
35	ChD_LDO_OUT	Channel "D" LDO output
36	ChD_PLL_GND	Channel "D" PLL ground
37	ChD_IF_VCC	Channel "D" IF supply voltage
38	ChD_Q_IF_GC	Channel "D_Q" IF GC input
39	ChD_I_IF_GC	Channel "D_I" IF GC input
40	ChD_Q_OUTp/SIGN	Channel "D_Q" analog output – true; 2-bit ADC digital output data – SIGN
41	ChD_Q_OUTn/MAGN	Channel "D_Q" analog output – complement; 2-bit ADC digital output data – MAGN
42	ChD_IFA_GND	Channel "D" IFA ground
43	ChD_I_OUTn/MAGN	Channel "D_I" analog output – complement; 2-bit ADC digital output data – MAGN
44	ChD_I_OUTp/SIGN	Channel "D_I" analog output – true; 2-bit ADC digital output data – SIGN
45	ChD_Q_DCOC	Channel "D_Q" DC offset compensation circuit capacitor connection
46	ChD_I_DCOC	Channel "D_I" DC offset compensation circuit capacitor connection
47	CSN	SPI chip select
48	SCLK	SPI clock input
49	MOSI	SPI data input
50	MISO	SPI data output
51	AOK	Cumulative status indicator: "1" valid "0" fail
52	FSp	ADC sampling frequency analog input – true; LVDS input – positive; CMOS input
53	FSn	ADC sampling frequency analog input – complement; LVDS input – negative
54	ChC_IFA_GND	Channel "C" IFA ground
55	ChC_IFA_VCC	Channel "C" IFA supply voltage
56	ChC_ADC_VCC	Channel "C" ADC supply voltage
57	ChC_ADC_GND	Channel "C" ADC ground
58	ChC_Q_OUTp/SIGN	Channel "C_Q" analog output – true; 2-bit ADC digital output data – SIGN
59	ChC_Q_OUTn/MAGN	Channel "C_Q" analog output – complement; 2-bit ADC digital output data – MAGN
60	ChC_IFA_GND	Channel "C" IFA ground
61	ChC_I_OUTn/MAGN	Channel "C_I" analog output - complement; 2-bit ADC digital output data – MAGN

#	Name	Description
62	ChC_I_OUTp/SIGN	Channel “C_I” analog output – true; 2-bit ADC digital output data – SIGN
63	ChC_IFA_GND	Channel “C” IFA ground
64	ChB_IFA_GND	Channel “B” IFA ground
65	ChB_IFA_VCC	Channel “B” IFA supply voltage
66	ChB_ADC_VCC	Channel “B” ADC supply voltage
67	ChB_ADC_GND	Channel “B” ADC ground
68	ChB_Q_OUTp/SIGN	Channel “B_Q” analog output – true; 2-bit ADC digital output data – SIGN
69	ChB_Q_OUTn/MAGN	Channel “B_Q” analog output – complement; 2-bit ADC digital output data – MAGN
70	ChB_IFA_GND	Channel “B” IFA ground
71	ChB_I_OUTn/MAGN	Channel “B_I” analog output – complement; 2-bit ADC digital output data – MAGN
72	ChB_I_OUTp/SIGN	Channel “B_I” analog output – true; 2-bit ADC digital output data – SIGN
73	ChB_IFA_GND	Channel “B” IFA ground
74	CLK_OUTn	Clock frequency analog output – complement; LVDS output – negative
75	CLK_OUTp	Clock frequency analog output – true; LVDS output – positive; CMOS output
76	ChA_IFA_GND	Channel “A” IFA ground
77	ChA_I_OUTp/SIGN	Channel “A_I” analog output – true; 2-bit ADC digital output data – SIGN
78	ChA_I_OUTn/MAGN	Channel “A_I” analog output – complement; 2-bit ADC digital output data – MAGN
79	ChA_IFA_GND	Channel “A” IFA ground
80	ChA_Q_OUTn/MAGN	Channel “A_Q” analog output – complement; 2-bit ADC digital output data – MAGN
81	ChA_Q_OUTp/SIGN	Channel “A_Q” analog output – true; 2-bit ADC digital output data – SIGN
82	ChA_ADC_GND	Channel “A” ADC ground
83	ChA_ADC_VCC	Channel “A” ADC supply voltage
84	ChA_IFA_VCC	Channel “A” IFA supply voltage
85	ChA_IFA_GND	Channel “A” IFA ground
86	REF_IN	Reference frequency (TCXO) input
87	ChA_PLL_GND	Channel “A” PLL ground
88	ChA_PLL_VCC	Channel “A” PLL supply voltage
89	ChA_AAD	Channel “A” active antenna supply voltage output
90	ChA_MIX_VCC	Channel “A” mixer supply voltage
91	ChA_MIX_IN	Channel “A” mixer input
92	ChA_MIX_GND	Channel “A” mixer ground
93	ChA_LNA_GND	Channel “A” LNA ground
94	ChA_LNA_OUT	Channel “A” LNA output
95	ChA_LNA_VCC	Channel “A” LNA supply voltage
96	ChA_AA_IN	Channel “A” active antenna input
97	ChA_LNA_GND	Channel “A” LNA ground

#	Name	Description
98	ChA_LNA_IN	Channel "A" LNA input
99	ChA_LNA_GND	Channel "A" LNA ground
100	ChB_LNA_GND	Channel "B" LNA ground
101	ChB_LNA_IN	Channel "B" LNA input
102	ChB_LNA_GND	Channel "B" LNA ground
103	ChB_AA_IN	Channel "B" active antenna input
104	ChB_LNA_VCC	Channel "B" LNA supply voltage
105	ChB_LNA_OUT	Channel "B" LNA output
106	ChB_LNA_GND	Channel "B" LNA ground
107	ChB_MIX_GND	Channel "B" mixer ground
108	ChB_MIX_IN	Channel "B" mixer input

## 3.4. SERIAL INTERFACE DESCRIPTION

### 3.4.1. PROTOCOL DESCRIPTION

NT1066 can be configured with standard 4-wire SPI. In addition special pin “AOK” (cumulative status indicator) for unexpected system failure tracking is available.

User register map is split up into five parts according to functionality:

- System info
- General settings and status
- CLK settings
- Channels “A”, “B” and “C” settings and status (separate for each channel)
- Channel “D” settings and status

Available settings and statuses are listed subsection in [3.4.2](#).

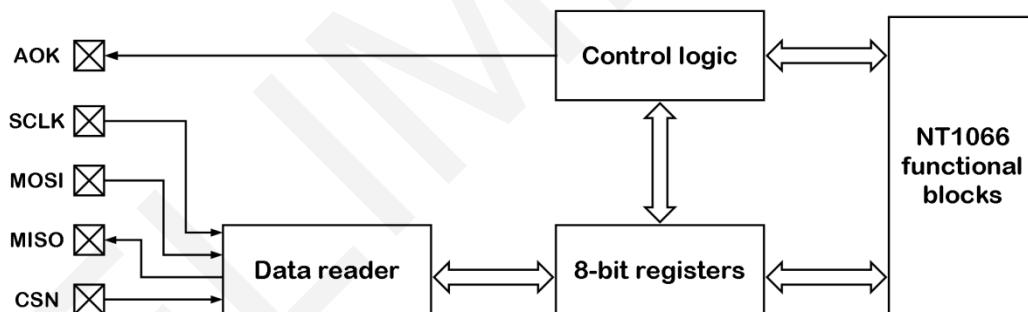
#### 3.4.1.1. GENERAL DESCRIPTION

Serial interface is used to read and change NT1066 data register information. It is intended for status monitoring, mode configuration and parameter adjustment.

Serial interface uses 4 pin communication:

- CSN (serial interface enable chip select signal)
- MISO (serial interface output data)
- MOSI (serial interface input data)
- SCLK (serial interface clock)

Serial interface structure is shown on [Figure 3.4](#).



[Figure 3.4](#): Serial interface structure

Standard information packet (command) consists of three bytes. The first and second bytes are command/address, third – data byte. Data format is always a bit sequence from first MSB to last LSB. All data transfers are framed by CSN signal, which must be low for any data transfer. In “idle” state, when CSN is high, SCLK, MOSI and MISO pins are blocked and don’t respond to external signals. SCLK must be low at the beginning of any data transfer (falling CSN edge).

#### 3.4.1.2. INFORMATION WRITING TO THE REGISTER

Single write reading is shown on [Figure 3.5](#). Communication is initialized by setting Chip Select (CSN) pin low. Bytes are transmitted MSB first. Data are clocked into the NT1066, through the MOSI pin, on the rising edges of SCLK. The first bit of a command/address byte is a read/write attribute: read operation is defined by logic “1” and write operation is defined by logic “0”. The second bit of a command/address byte is a AINC attribute: automatic addition value a command/address is defined by logic “1”. Bits A13...A0 represent the address of the register to be read or written. Third byte (D7...D0 bits) is data written from (or to be read to) the given

address. After the 23<sup>th</sup> rising SCLK edge and turn-off CSN hold time CSN goes high, disabling the interface.

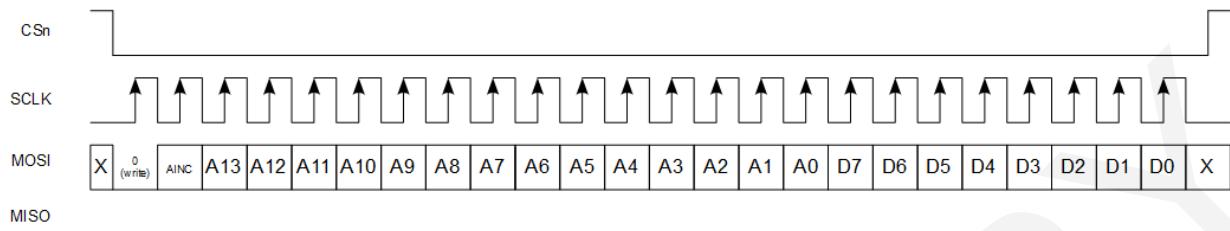


Figure 3.5: Individual register writing

#### 3.4.1.3. INFORMATION READING FROM THE REGISTER

Single register reading is similar to writing. First byte is command byte. Read attribute is logic "1" and A13-A0 bits specify address of register to be read. Data are clocked out the NT1066, through the MISO pin, on the falling edges of SCLK. Output data should be clocked on rising SCLK edges of external SPI master. Bytes are transmitted MSB first. After sending data byte CSN goes high, disabling the interface.

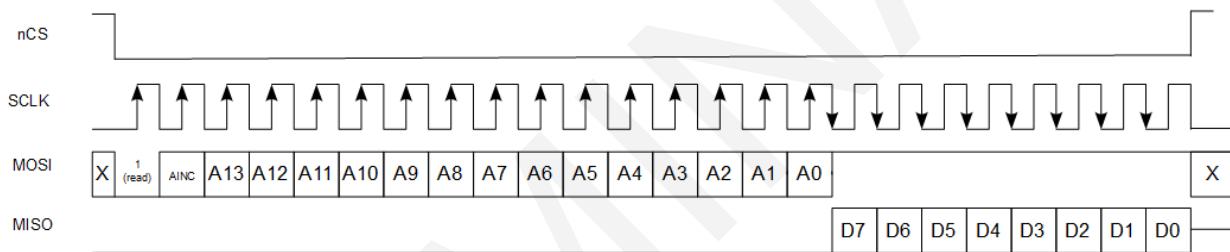


Figure 3.6: Single register reading

#### 3.4.1.4. BURST DATA TRANSFER

NT1066 has a SPI burst-mode data transfer. Unlike single data transfer CSN is continue to be "low" after LSB of data byte. Next bit after LSB is a write/read attribute. CSN goes high to stop burst data transfer. Direction of data transfer can be changed an infinite number of times during burst data transfer. See examples below, please.

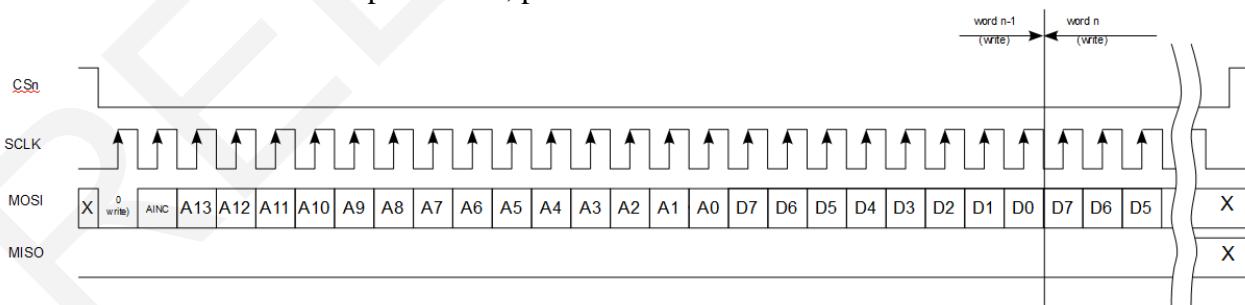


Figure 3.7: Burst data writing

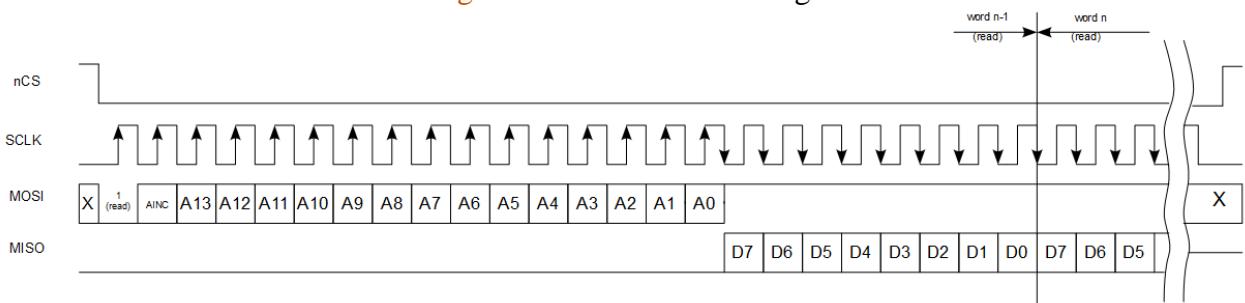


Figure 3.8: Burst data reading

### 3.4.2. PROGRAMMABLE REGISTERS

#### 3.4.2.1. SYSTEM INFO

- Chip serial number, release

Bit number	Description	Default
<b>Reg0, 0x00</b>		
D7-D0 (MSB)	Chip serial number. $(0010000101010)_{dec} = 1066$	“00100001”
<b>Reg1, 0x01</b>		
D7-D3 (LSB)	Continue. Refer to Reg0<D7-D0>.	“01010”
D2-D0	Chip version. $(001)_{dec} = 1$	“001”

#### 3.4.2.2. GENERAL SETTINGS AND STATUS

- General status (common AOK, channel "A" AOK, channel "B" AOK, channel "C" AOK, channel "D" AOK, die temperature)
- Common AOK indicator configuration (4 bits)
- Operation mode (channel “A” enable, channel “B” enable, channel “C” enable, channel “D” enable, CLK output enable)
- TCXO frequency (value in kHz) //valid range is 10-55MHz
- Temperature measurement mode (single, continuous)
- Temperature measurement system execute

Bit number	Description	Default
<b>Reg2, 0x02</b>		
D7-D5	Unused	“000”
D4		
	Common cumulative status indicator: “0” fail “1” valid	-
D3		
	Channel “A” cumulative status indicator: “0” fail “1” valid	-
D2		
	Channel “B” cumulative status indicator: “0” fail “1” valid	-
D1		
	Channel “C” cumulative status indicator: “0” fail “1” valid	-
D0		
	Channel “D” cumulative status indicator: “0” fail “1” valid	-
<b>Reg3, 0x03</b>		
D7-D4	Unused	“0000”
D3		
	Channel “A” cumulative status as common AOK's component: “0” forbidden “1” permitted	“1”
D2		
	Channel “B” cumulative status as common AOK's component: “0” forbidden “1” permitted	“1”
D1		
	Channel “C” cumulative status as common AOK's component: “0” forbidden “1” permitted	“1”

<b>Bit number</b>	<b>Description</b>	<b>Default</b>
D0	Channel “D” cumulative status as common AOK’s component: “0” forbidden “1” permitted	“1”
<b>Reg4, 0x04</b>		
D7-D2	Unused	“000000”
D1-D0 (MSB)	Temperature sensor indicator: $T = 506 - 0.755 * (\text{Reg4}\langle\text{D1-D0}\rangle_{\text{dec}} + \text{Reg5}\langle\text{D7-D0}\rangle_{\text{dec}})$ “0000000000” not valid range ... ... “1000011000” not valid range “1000011001” +100 °C “1001111010” 27 “1011010011” -40 °C “1011010100” not valid range ... ... “1111111111” not valid range	-
<b>Reg5, 0x05</b>		
D7-D0 (LSB)	Continue. Refer to Reg4<D1-D0>.	-
<b>Reg6, 0x06</b>		
D7-D5	Unused	“000”
D4	Clock output enable: “0” disabled “1” enabled	“0”
D3	Channel “D” enable: “0” disabled “1” enabled	“0”
D2	Channel “C” enable: “0” disabled “1” enabled	“0”
D1	Channel “B” enable: “0” disabled “1” enabled	“0”
D0	Channel “A” enable: “0” disabled “1” enabled	“0”
<b>Reg7, 0x07</b>		
D7-D0 (MSB)	Reference oscillator frequency, kHz. <i>Note: Valid range is 10-55MHz.</i>	“00100111”
<b>Reg8, 0x08</b>		
D7-D0 (LSB)	Continue. Refer to Reg7<D7-D0>.	“00010000”
<b>Reg9, 0x09</b>		
D7-D2	Unused	“000000”
D1	Temperature measurement mode: “0” single “1” continuous	“0”
D0	Temperature measurement system execution: “0” finished “1” start (automatically reset to “0” when finished)	“0”

### 3.4.2.3. CLK SETTINGS

- CLK frequency source (PLL "A", PLL "B", PLL "C", external via pins 52-53, TCXO pass-through)
- C-divider ratio (:4, :5 ... :255) //if PLL "A", PLL "B", PLL "C" CLK frequency source
- CLK output type (ECL, LVDS, CMOS)
- CLK amplitude //2 bits if 'ECL' type; 2 bits if 'LVDS' type
- CLK output DC level (2 bits) //if 'ECL' type
- CLK output voltage (3 bits) //if 'CMOS' type
- Sampling frequency input type (LVDS, ECL/CMOS)
- Internal terminator enable //if 'LVDS' type
- Internal terminator value (2 bits) //if 'LVDS' type

Bit number	Description	Default
<b>Reg10, 0x0A</b>		
D7-D5	Unused	"000"
D4-D3	Clock output type: "00" CMOS "01" ECL "10" LVDS "11" high resistance state	"10"
D2-D0	Clock frequency and ADC sampling frequency source: "000" PLL "A" "001" PLL "B" "010" PLL "C" "011" TCXO pass-through "100" external sampling frequency via pins #52-53	"000"
<b>Reg11, 0x0B</b>		
D7-D0	Clock C-divider ratio: "00000100" 4 ... with step of 1 "11111111" 255	"0010110"
<i>Note: If Reg10&lt;D2-D0&gt; = "000", "001", "010".</i>		
<b>Reg12, 0x0C</b>		
D7	Unused	"0"
D6-D5	Clock amplitude: LVDS F <sub>CLK</sub> =6...50MHz ECL F <sub>CLK</sub> =50...100MHz "00" 320 mV 388 mV 320 mV "01" 480 mV 492 mV 420 mV "10" 640 mV 740 mV 600 mV "11" 800 mV 840 mV 690 mV	"01"
<i>Note: If Reg10&lt;D2-D0&gt; ≠ "100".</i>		
D4-D3	Clock output DC level: "00" 1.8-0.25*Reg12<D6-D5> "01" 1.95-0.25*Reg12<D6-D5> "10" 2.7-0.25*Reg12<D6-D5> "11" 2.85-0.25*Reg12<D6-D5>	"11"
<i>Note: If Reg10&lt;D4-D3&gt; = "01". Reg12&lt;D6-D5&gt; - value in mV.</i>		
D2-D0	Clock output voltage: "000" 1.8 V "001" 1.95 V "010" 2.7 V "011" 2.85 V "1XX" VCC-0.1	"011"
<i>Note: If Reg10&lt;D4-D3&gt; = "00".</i>		

Bit number	Description	Default
<b>Reg13, 0x0D</b>		
D7-D4	Unused	“0000”
D3-D2	Internal terminator value: “00” 90 Ohm “01” 100 Ohm “10” 100 Ohm “11” 110 Ohm  <i>Note: If Reg13&lt;D0&gt; = “1”.</i>	“01”
D1	Internal terminator enable: “0” disabled “1” enabled  <i>Note: If Reg13&lt;D0&gt; = “1”.</i>	“0”
D0	External sampling frequency input type: “0” ECL/CMOS “1” LVDS	“1”

#### 3.4.2.4. CHANNELS “A”, “B”, “C” SETTINGS AND STATUS

- Channel status (channel AOK, LNA status, active antenna indicators, PLL lock indicator, VCO voltage comparator status, LPF autocalibration system status)
- Channel AOK configuration (active antenna current indicator, PLL lock indicator, VCO voltage comparator status, LPF autocalibration system status, tuning systems status)
- Channel mode (IQ, lower sideband, upper sideband, lower sideband + upper sideband)
- LO frequency (value in kHz) //valid range is 1550-1615MHz if L1 band;  
1160-1300MHz if L2, L3, L5 bands
- PLL mode (integer-N, fractional-N)
- R-divider ratio (:1, :2 ... :31)//if ‘integer-N’ PLL mode
- N-divider ratio (:16, :17 ... :4095) //if ‘integer-N’ PLL mode
- PLL tuning system execute
- IF I passband (7 bits) //if IQ, lower + upper sidebands or upper sideband
- IF Q passband (7 bits) // if IQ, lower + upper sidebands or lower sideband
- LPF autocalibration system execute
- IF GC mode (automatic, manual via SPI)
- IF I gain (10 bits) //if manual GC mode
- IF Q gain (10 bits)// if manual GC mode
- Output data interface (analog differential output, 2-bit ADC output)
- 2-bit ADC logic-level high (1.8V, 2.0V, 2.5V, VCC)
- 2-bit ADC type (asynchronous, clocked by rising edge, clocked by falling edge)

Bit number	Description	Default
<b>Reg14, 0x0E for Channel “A” / Reg36, 0x24 for Channel “B” / Reg58, 0x3A for Channel “C”</b>		
D7	Channel# LNA1 enable status	-
D6	Channel# LNA2 enable status	-
D5	Channel# PLL status: “0” not locked “1” locked	-
D4-D3	Channel# VCO voltage comparator status: “00” valid “01” upper threshold exceeded (oscillation frequency is too low) “10” lower threshold exceeded (oscillation frequency is too high) “11” unused	-

<b>Bit number</b>	<b>Description</b>	<b>Default</b>
D2	Channel# active antenna connection indicator: “0” not connected (active antenna current is too low) “1” connected (active antenna current is within limits)	-
D1	Channel# active antenna current indicator: “0” valid (active antenna current is within or below limits) “1” upper threshold exceeded (active antenna current is too high)	-
D0	Channel# LPF autocalibration system status: “0” error “1” completed successfully	-

**Reg15, 0x0F for Channel “A” / Reg37, 0x25 for Channel “B” / Reg59, 0x3B for Channel “C”**

D7-D5	Unused	“000”
D4	Channel# PLL status as channel AOK's component: “0” forbidden “1” permitted	“1”
D3	Channel# VCO voltage comparator status as channel AOK's component: “0” forbidden “1” permitted	“1”
D2	Channel# tuning systems status as channel AOK's component: “0” forbidden “1” permitted	“1”
D1	Channel# active antenna current indicator as channel AOK's component: “0” forbidden “1” permitted	“1”
D0	Channel# LPF autocalibration system status as AOK's component: “0” forbidden “1” permitted	“1”

**Reg16, 0x10 for Channel “A” / Reg38, 0x26 for Channel “B” / Reg60, 0x3C for Channel “C”**

D7-D2	Unused	“000000”
D1-D0	Channel# mode: “00” IQ “01” lower sideband “10” upper sideband “11” lower sideband + upper sideband	“00”

**Reg17, 0x11 for Channel “A” / Reg39, 0x27 for Channel “B” / Reg61, 0x3D for Channel “C”**

D7	Unused	“0”
D6-D0 (MSB)	Channel# LO frequency, kHz.	Ch “A” “0011000” Ch “B” “0010010” Ch “C” “0010010”

**Reg18, 0x12 for Channel “A” / Reg40, 0x28 for Channel “B” / Reg62, 0x3E for Channel “C”**

D7-D0	Continue. Refer to <b>Reg17&lt;D6-D0&gt;</b> for Channel “A” / <b>Reg39&lt;D6-D0&gt;</b> for Channel “B” / <b>Reg61&lt;D6-D0&gt;</b> for Channel “C”.	Ch “A” “01000010” Ch “B” “11011000” Ch “C” “00101000”
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**Reg19, 0x13 for Channel “A” / Reg41, 0x29 for Channel “B” / Reg63, 0x3F for Channel “C”**

D7-D0 (LSB)	Continue. Refer to <b>Reg17&lt;D6-D0&gt;</b> for Channel “A” / <b>Reg39&lt;D6-D0&gt;</b> for Channel “B” / <b>Reg61&lt;D6-D0&gt;</b> for Channel “C”.	Ch “A” “11110000” Ch “B” “00111000” Ch “C” “01110000”
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Bit number	Description	Default
<b>Reg20, 0x14 for Channel “A” / Reg42, 0x2A for Channel “B” / Reg64, 0x40 for Channel “C”</b>		
D7-D1	Unused	“0000000”
D0	Channel# PLL mode: “0” integer-N “1” fractional-N	“1”
<b>Reg21, 0x15 for Channel “A” / Reg43, 0x2B for Channel “B” / Reg65, 0x41 for Channel “C”</b>		
D7-D5	Unused	“000”
D4-D0	Channel# R-divider ratio: “00000” unused “00001” 1 ... with step of 1 “11111” 31	“00001”
<i>Note: If Reg20&lt;D0&gt; for Channel “A” / Reg42&lt;D0&gt; for Channel “B” / Reg64&lt;D0&gt; for Channel “C” is “0”.</i>		
<b>Reg22, 0x16 for Channel “A” / Reg44, 0x2C for Channel “B” / Reg66, 0x42 for Channel “C”</b>		
D7-D4	Unused	“0000”
D3-D0 (MSB)	Channel# N-divider ratio: “000000000000” unused ... unused “000000011111” unused “000000010000” 16 ... with step of 1 “111111111111” 4095	Ch “A” “0001” Ch “B” “0000” Ch “C” “0000”
<i>Note: If Reg20&lt;D0&gt; for Channel “A” / Reg42&lt;D0&gt; for Channel “B” / Reg64&lt;D0&gt; for Channel “C” is “0”.</i>		
<b>Reg23, 0x17 for Channel “A” / Reg45, 0x2D for Channel “B” / Reg67, 0x43 for Channel “C”</b>		
D7-D0 (LSB)	Continue. Refer to Reg22<D3-D0> for Channel “A” / Reg44<D3-D0> for Channel “B” / Reg66<D3-D0> for Channel “C”.	Ch “A” “00111110” Ch “B” “11110111” Ch “C” “11101110”
<b>Reg24, 0x18 for Channel “A” / Reg46, 0x2E for Channel “B” / Reg68, 0x44 for Channel “C”</b>		
D7-D1	Unused	“0000000”
D0	Channel# PLL divider ratio calculation and subband autoselection system execution: “0” finished “1” start (reset to “0” automatically when finished)	“0”
<b>Reg25, 0x19 for Channel “A” / Reg47, 0x2F for Channel “B” / Reg69, 0x45 for Channel “C”</b>		
D7	Unused	“0”
D6-D0	Channel# LPF_I cut-off frequency: “0000000” 9.47 MHz not guaranteed range ... “0010000” 13.54 MHz not guaranteed range “0010001” 13.79 MHz ... “0011001” 15.78 MHz ... “0101011” 20.06 MHz ... “1000001” 25.05 MHz ... “1011001” 30.06 MHz “1011010” 30.26 MHz not guaranteed range ... “1111111” 36.95 MHz not guaranteed range	Ch “A” “1011001” Ch “B” “0101011” Ch “C” “1011001”
<i>Note: If Reg16&lt;D1-D0&gt; for Channel “A” / Reg38&lt;D1-D0&gt; for Channel “B” / Reg60&lt;D1-D0&gt; for Channel “C” is “00”, “10”, “11”.</i>		

Bit number	Description	Default	
<b>Reg26, 0x1A for Channel “A” / Reg48, 0x30 for Channel “B” / Reg70, 0x46 for Channel “C”</b>			
D7	Unused	“0”	
D6-D0	Channel# LPF_Q cut-off frequency: “0000000” 9.47 MHz not guaranteed range	Ch “A” “1011001” Ch “B” “0101011” Ch “C” “1011001”	
	... ...		
	“0010000” 13.54 MHz not guaranteed range		
	“0010001” 13.79 MHz		
	... ...		
	“0011001” 15.78 MHz		
	... ...		
	“0101011” 20.06 MHz		
	... ...		
	“1000001” 25.05 MHz		
	... ...		
	“1011001” 30.06 MHz		
	“1011010” 30.26 MHz not guaranteed range		
	... ...		
	“1111111” 36.95 MHz not guaranteed range		
	<i>Note: If Reg16&lt;DI-D0&gt; for Channel “A” / Reg38&lt;DI-D0&gt; for Channel “B” / Reg60&lt;DI-D0&gt; for Channel “C” is “00”, “01”, “11”.</i>		
	<b>Reg27, 0x1B for Channel “A” / Reg49, 0x31 for Channel “B” / Reg71, 0x47 for Channel “C”</b>		
D7-D1	Unused	“0000000”	
D0	Channel# LPF autocalibration system execution: “0” finished “1” start (reset to “0” automatically when finished)	“0”	
<b>Reg28, 0x1C for Channel “A” / Reg50, 0x32 for Channel “B” / Reg72, 0x48 for Channel “C”</b>			
D7-D6	Unused	“00”	
D5-D4	Channel# 2-bit ADC type: “0X” asynchronous “10” clocked by rising edge “11” clocked by falling edge	“10”	
	<i>Note: If Reg28&lt;D0&gt; for Channel “A” / Reg50&lt; D0&gt; for Channel “B” / Reg72&lt;D0&gt; for Channel “C” is “1”.</i>		
D3-D2	Channel# 2-bit ADC logic-level high: “00” 1.8V “01” 2.0V “10” 2.5V “11” VCC	“11”	
	<i>Note: If Reg28&lt;D0&gt; for Channel “A” / Reg50&lt; D0&gt; for Channel “B” / Reg72&lt;D0&gt; for Channel “C” is “1”.</i>		
	Channel# IFA gain control mode: “0” manual “1” automatic		
	<i>Note: If Reg28&lt;D0&gt; for Channel “A” / Reg50&lt; D0&gt; for Channel “B” / Reg72&lt;D0&gt; for Channel “C” is “1”.</i>		
	Channel# output data interface: “0” analog differential “1” 2-bit ADC		

Bit number	Description	Default
<b>Reg29, 0x1D for Channel “A” / Reg51, 0x33 for Channel “B” / Reg73, 0x49 for Channel “C”</b>		
D7-D2	Unused	“000000”
D1-D0 (MSB)	Channel# IFA_I gain value: “0000000000” 1.12 dB ... “0100001110” 1.30 dB ... “0100101100” 4.55 dB ... “0101001010” 10.00 dB ... “0110000110” 12.98 dB ... “0110100100” 18.82 dB ... “0111000010” 23.31 dB ... “0111111110” 26.10 dB ... “1000011100” 32.03 dB ... “1001011000” 37.79 dB ... “1010010100” 44.38 dB ... “1011010000” 46.52 dB ... “1011101110” 52.13 dB ... “1100001100” 54.62 dB ... “1100101010” 63.04 dB ... “1111000000” 67.25 dB ... “1111011110” 67.30 dB	“01”
	<i>Note: If Reg28&lt;D1&gt; for Channel “A” / Reg50&lt;D1&gt; for Channel “B” / Reg72&lt;D1&gt; for Channel “C” is “0”.</i>	
	Channel# IFA_I digital detector threshold w.r.t. sinewave signal: “0000000000” 0 % ... “0101000000” 30% ... “0111111111” 45% ... “1100110010” 73% ... “1111111111” 96%	
	<i>Note: If Reg28&lt;D0&gt; for Channel “A” / Reg50&lt;D0&gt; for Channel “B” / Reg72&lt;D0&gt; for Channel “C” is “1” and Reg28&lt;D1&gt; for Channel “A” / Reg50&lt;D1&gt; for Channel “B” / Reg72&lt;D1&gt; for Channel “C” is “1”.</i>	
<b>Reg30, 0x1E for Channel “A” / Reg52, 0x34 for Channel “B” / Reg74, 0x4A for Channel “C”</b>		
D7-D0 (LSB)	Continue. Refer to Reg29<D1-D0> for Channel “A” / Reg51<D1-D0> for Channel “B” / Reg73<D1-D0> for Channel “C”.	“00101100”

Bit number	Description	Default
<b>Reg31, 0x1F for Channel “A” / Reg53, 0x35 for Channel “B” / Reg75, 0x4B for Channel “C”</b>		
D7-D2	Unused	“000000”
D1-D0 (MSB)	Channel# IFA_Q gain value: “0000000000” 1.12 dB ... “0100001110” 1.30 dB ... “0100101100” 4.55 dB ... “0101001010” 10.00 dB ... “0110000110” 12.98 dB ... “0110100100” 18.82 dB ... “0111000010” 23.31 dB ... “0111111110” 26.10 dB ... “1000011100” 32.03 dB ... “1001011000” 37.79 dB ... “1010010100” 44.38 dB ... “1011010000” 46.52 dB ... “1011101110” 52.13 dB ... “1100001100” 54.62 dB ... “1100101010” 63.04 dB ... “1111000000” 67.25 dB ... “1111011110” 67.30 dB	“01”
	<i>Note: If Reg28&lt;DI&gt; for Channel “A” / Reg50&lt;DI&gt; for Channel “B” / Reg72&lt;DI&gt; for Channel “C” is “0”.</i>	
	Channel# IFA_Q digital detector threshold w.r.t sinewave signal: “0000000000” 0 % ... “0101000000” 30% ... “0111111111” 45% ... “1100110010” 73% ... “1111111111” 96%	
	<i>Note: If Reg28&lt;D0&gt; for Channel “A” / Reg50&lt;D0&gt; for Channel “B” / Reg72&lt;D0&gt; for Channel “C” is “1” and Reg28&lt;DI&gt; for Channel “A” / Reg50&lt;DI&gt; for Channel “B” / Reg72&lt;DI&gt; for Channel “C” is “1”.</i>	
<b>Reg32, 0x20 for Channel “A” / Reg54, 0x36 for Channel “B” / Reg76, 0x4C for Channel “C”</b>		
D7-D0 (LSB)	Continue. Refer to Reg31<D1-D0> for Channel “A” / Reg53<D1-D0> for Channel “B” / Reg75<D1-D0> for Channel “C”.	“00101100”

### Active antenna detector system:

- Active antenna detector system enable
- Active antenna detector thresholds (4 bits)
- AAD system behavior if short circuit detected (current limitation, minimum current restriction)
- LNA1/LNA2 switching mode (automatic, manual)
- LNA1/LNA2 enable //if manual switching mode

Bit number	Description	Default
<b>Reg33, 0x21 for Channel “A” / Reg55, 0x37 for Channel “B” / Reg77, 0x4D for Channel “C”</b>		
D7-D4	Channel# active antenna detector thresholds: “0000” 0.45...4.0 mA “0001” 0.90...8.0 mA “0010” 1.35...12.0 mA “0011” 1.80...16.0 mA “0100” 2.25...20.0 mA “0101” 2.70...24.0 mA “0110” 3.15...28.0 mA “0111” 3.60...32.0 mA “1000” 4.05...36.0 mA “1001” 4.50...40.0 mA “1010” 4.95...44.0 mA “1011” 5.40...48.0 mA “1100” 5.85...52.0 mA “1101” 6.30...56.0 mA “1110” 6.75...60.0 mA “1111” 7.20...64.0 mA	“0011”
D3-D1	Unused	“000”
D0	Channel# active antenna detector behavior if short circuit detected: “0” current limitation “1” minimum current restriction <i>Note: If Reg34&lt;D2&gt; for Channel “A” / Reg56&lt;D2&gt; for Channel “B” / Reg78&lt;D2&gt; for Channel “C” is “1”.</i>	“0”
<b>Reg34, 0x22 for Channel “A” / Reg56, 0x38 for Channel “B” / Reg78, 0x4E for Channel “C”</b>		
D7-D4	Unused	“0000”
D3	Channel# active antenna detector permission for autoselection of LNA1 or LNA2: “0” forbidden “1” permitted <i>Note: If Reg34&lt;D2&gt; for Channel “A” / Reg56&lt;D2&gt; for Channel “B” / Reg78&lt;D2&gt; for Channel “C” is “1”.</i>	“1”
D2	Channel# active antenna detector enable: “0” disabled “1” enabled	“1”
D1	Channel# LNA enable: “0” disabled “1” enabled <i>Note: If Reg34&lt;D3&gt; for Channel “A” / Reg56&lt;D3&gt; for Channel “B” / Reg78&lt;D3&gt; for Channel “C” is “0”.</i>	“1”
D0	Channel# LNA1 or LNA2 enable: “0” LNA1 “1” LNA2 <i>Note: If Reg34&lt;D3&gt; for Channel “A” / Reg56&lt;D3&gt; for Channel “B” / Reg78&lt;D3&gt; for Channel “C” is “0” and Reg34&lt;D1&gt; for Channel “A” / Reg56&lt;D1&gt; for Channel “B” / Reg78&lt;D1&gt; for Channel “C” is “0”.</i>	“0”

### Calibration and test section:

- IQ phase correction (6 bits)

Bit number	Description	Default
<b>Reg35, 0x23 for Channel "A" / Reg57, 0x39 for Channel "B" / Reg79, 0x4F for Channel "C"</b>		
D7-D6	Unused	"00"
D5-D0	Channel# IQ phase correction: "000000" 74.1° ... "011111" 89.8° "100000" 90° "100001" 90.3° ... "111111" 104.9°	"011111"

### 3.4.2.5. CHANNEL "D" SETTINGS AND STATUS

- Channel status (channel AOK, PLL lock indicator, VCO voltage comparator status, RF gain, IF gain)
- Channel AOK configuration (PLL lock indicator, VCO voltage comparator status, tuning systems status)
- LO frequency (value in KHz) //valid range is 2340-2580MHz if S band; 1170-1290MHz if L2, L3, L5 bands; 65-110MHz if FM band; 160-240MHz if VHF band; 470-862MHz if UHF band
- PLL tuning system execute
- RF GC mode (automatic, manual via SPI, external loop via pin 27)
- RF gain (4 bits) //if manual GC mode
- IF passband (8 bits)
- IF GC mode (automatic, manual via SPI, external loop via pins 38-39)
- IF I gain (9 bits) //if manual GC mode
- IF Q gain (9 bits) //if manual GC mode
- IF AGC thresholds (7 bits) // if 'analog differential' type
- IFA output DC level (2 bits) //if 'analog differential' type
- Output data interface (analog differential output, 2-bit ADC output)
- 2-bit ADC logic-level high (1.8V, 2.0V, 2.5V, VCC)
- 2-bit ADC type (asynchronous, clocked by rising edge, clocked by falling edge)

Bit number	Description	Default
<b>Reg80, 0x50</b>		
D7-D3	Unused	"00000"
D2-D1	Channel "D" VCO voltage comparator status: "00" valid "01" upper threshold exceeded (oscillation frequency is too low) "10" lower threshold exceeded (oscillation frequency is too high) "11" unused	-
D0	Channel "D" PLL status: "0" not locked "1" locked	-
<b>Reg81, 0x51</b>		
D7-D4	Unused	"0000"
D3-D0	Channel "D" RF gain status.	-

<b>Bit number</b>	<b>Description</b>	<b>Default</b>
<b>Reg82, 0x52</b>		
D7-D1	Unused	“0000000”
D0 (MSB)	Channel “D” IFA_I gain status.	-
<b>Reg83, 0x53</b>		
D7-D0 (LSB)	Continue. Refer to Reg82<D0>.	-
<b>Reg84, 0x54</b>		
D7-D1	Unused	“0000000”
D0 (MSB)	Channel “D” IFA_Q gain status.	-
<b>Reg85, 0x55</b>		
D7-D0 (LSB)	Continue. Refer to Reg84<D0>.	-
<b>Reg86, 0x56</b>		
D7-D3	Unused	“00000”
D2	Channel “D” PLL status as channel AOK's components: “0” forbidden “1” permitted	“1”
D1	Channel “D” VCO voltage comparator status as channel AOK's component: “0” forbidden “1” permitted	“1”
D0	Channel “D” tuning systems status as channel AOK's component: “0” forbidden “1” permitted	“1”
<b>Reg87, 0x57</b>		
D7	Unused	“0”
D6-D0 (MSB)	Channel “D” LO frequency, kHz.	“0100110”
<b>Reg88, 0x58</b>		
D7-D0	Continue. Refer to Reg87<D6-D0>.	“00000110”
<b>Reg89, 0x59</b>		
D7-D0 (LSB)	Continue. Refer to Reg87<D6-D0>.	“01100000”
<b>Reg90, 0x5A</b>		
D7-D1	Unused	“0000000”
D0	Channel “D” PLL divider ratio calculation and subband autoselection system execution: “0” finished “1” start (reset to “0” automatically when finished)	“0”

Bit number	Description					Default
<b>Reg91, 0x5B</b>						
D7	Unused					“0”
D6-D3	Channel “D” RF gain:					
	FM	VHF	UHF	L	S	
	“0000”	-7.7 dB	-11.8 dB	-4.9 dB	-6.8 dB	-6.4 dB
	“0001”	-5.3 dB	-9.6 dB	-2.9 dB	-4.7 dB	-4.1 dB
	“0010”	-2.0 dB	-6.5 dB	-0.7 dB	-2.5 dB	-1.7 dB
	“0011”	0.6 dB	-4.0 dB	1.5 dB	-0.1 dB	0.9 dB
	“0100”	3.2 dB	-1.5 dB	3.4 dB	2.2 dB	3.5 dB
	“0101”	6.5 dB	1.8 dB	4.3 dB	4.1 dB	4.6 dB
	“0110”	10.2 dB	5.4 dB	6.2 dB	6.8 dB	6.7 dB
	“0111”	13.1 dB	8.3 dB	8.9 dB	9.8 dB	9.5 dB
	“1000”	18.6 dB	14.6 dB	16.1 dB	14.1 dB	13.5 dB
	“1001”	20.6 dB	17.3 dB	17.0 dB	16.9 dB	14.9 dB
	“1010”	23.5 dB	20.2 dB	19.2 dB	19.7 dB	17.5 dB
	“1011”	26.1 dB	22.9 dB	21.8 dB	22.5 dB	20.3 dB
	“1100”	29.1 dB	26.1 dB	23.5 dB	24.9 dB	22.9 dB
	“1101”	31.3 dB	28.2 dB	26.0 dB	27.5 dB	25.5 dB
	“1110”	31.3 dB	28.2 dB	26.0 dB	27.5 dB	25.5 dB
	“1111”	31.3 dB	28.2 dB	26.0 dB	27.5 dB	25.5 dB
<i>Note: If Reg91&lt;D1-D0&gt; is “00”.</i>						
D2	Unused					“0”
D1-D0	Channel “D” RF gain control mode:					
	“00”	manual				
	“01”	automatic				“00”
	“10”	external loop via pin #27				
<b>Reg92, 0x5C</b>						
D7-D0	Channel “D” LPF cut-off frequency:					
	“00000000”	2.66 MHz	not guaranteed range			
	...	...				
	“00000110”	2.97 MHz	not guaranteed range			
	“00000111”	3.12 MHz				
	...	...				
	“00011011”	4.02 MHz				
	...	...				
	“00110000”	5.05 MHz				
	...	...				
	“01000101”	6.03 MHz				
	...	...				
	“01011010”	7.03 MHz				“10110111”
	...	...				
	“01110010”	8.12 MHz				
	...	...				
	“10001010”	9.15 MHz				
	...	...				
	“10011111”	10.04 MHz				
	...	...				
	“10111001”	11.16 MHz				
	“10111010”	11.21 MHz	not guaranteed range			
	...	...				
	“11111111”	13.92 MHz	not guaranteed range			

<b>Bit number</b>	<b>Description</b>	<b>Default</b>
<b>Reg93, 0x5D</b>		
D7	Unused	“0”
D6-D5	Channel “D” 2-bit ADC type: “0X” asynchronous “10” clocked by rising edge “11” clocked by falling edge <i>Note: If Reg93&lt;D2&gt; is “1”.</i>	“10”
D4-D3	Channel “D” 2-bit ADC logic-level high: “00” 1.8V “01” 2.0V “10” 2.5V “11” VCC <i>Note: If Reg93&lt;D2&gt; is “1”.</i>	“11”
D2	Channel “D” output data interface: “0” analog differential output “1” 2-bit ADC output	“1”
D1-D0	Channel “D” IFA gain control mode: “0X” manual “10” automatic via external pins #38-39 “11” automatic	“11”
<b>Reg94, 0x5E</b>		
D7-D1	Unused	“0000000”
D0 (MSB)	Channel “D” IFA_I gain: “000000000” -6.34 dB ... “000100000” -1.34 dB ... “000111111” 4.14 dB ... “001111111” 13.96 dB ... “011011111” 28.89 dB ... “100100000” 38.40 dB ... “101100000” 48.27 dB ... “110111111” 63.82 dB ... “111111111” 73.74 dB <i>Note: If Reg93&lt;DI-D0&gt; is “0X”.</i>	“0”
	Channel “D” IFA_I digital detector threshold w.r.t sinewave signal: “0000000000” 0 % ... “0101000000” 30% ... “0111111111” 45% ... “1100110010” 73% ... “1111111111” 96%	
	<i>Note: If Reg93&lt;D2&gt; is “1” and Reg93&lt;DI-D0&gt; is “11”.</i>	
<b>Reg95, 0x5F</b>		
D7-D0 (LSB)	Continue. Refer to Reg94<D0>.	“01111111”

Bit number	Description	Default
<b>Reg96, 0x60</b>		
D7-D1	Unused	“0000000”
	Channel “D” IFA_Q gain: “000000000” -6.34 dB ... “000100000” -1.34 dB ... “000111111” 4.14 dB ... “001111111” 13.96 dB ... “011011111” 28.89 dB ... “100100000” 38.40 dB ... “101100000” 48.27 dB	
D0 (MSB)	... “110111111” 63.82 dB ... “111111111” 73.74 dB	“0”
	<i>Note:</i> If Reg93<D1-D0> is “0X”. Channel “D” IFA_Q digital detector threshold w.r.t sinewave signal: “0000000000” 0 % ... “0101000000” 30% ... “0111111111” 45% ... “1100110010” 73% ... “1111111111” 96%	
	<i>Note:</i> If Reg93<D2> is “1” and Reg93<D1-D0> is “11”.	
<b>Reg97, 0x61</b>		
D7-D0 (LSB)	Continue. Refer to Reg96<D0>.	“01111111”

<b>Bit number</b>	<b>Description</b>	<b>Default</b>
<b>Reg98, 0x62</b>		
D7-D0	Channel “D” IFA_I output amplitude upper threshold control: “00000001” 5 mV ... “00000010” 10 mV ... “00100101” 50 mV ... “01010000” 97.8 mV ... “01010010” 100 mV ... “10100000” 200 mV ... “11000100” 300 mV ... “11010100” 400 mV ... “11011100” 500 mV ... “11100010” 600 mV	“01010000”
	<i>Note: If Reg93&lt;DI-D0&gt; is “IX” and Reg93&lt;D2&gt; is “0”.</i>	
<b>Reg99, 0x63</b>		
D7-D0	Channel “D” IFA_I output amplitude lower threshold control: “00000001” 5 mV ... “00000010” 10 mV ... “00100101” 50 mV ... “01001100” 93.5 mV ... “01010010” 100 mV ... “10100000” 200 mV ... “11000100” 300 mV ... “11010100” 400 mV ... “11011100” 500 mV ... “11100010” 600 mV	“01001100”
	<i>Note: If Reg93&lt;DI-D0&gt; is “IX” and Reg93&lt;D2&gt; is “0”.</i>	

<b>Bit number</b>	<b>Description</b>	<b>Default</b>
<b>Reg100, 0x64</b>		
D7-D0	<p>Channel “D” IFA_Q output amplitude upper threshold control:</p> <p>“00000001” 5 mV  ...  “00000010” 10 mV  ...  “00100101” 50 mV  ...  “01010000” 97.8 mV  ...  “01010010” 100 mV  ...  “10100000” 200 mV  ...  “11000100” 300 mV  ...  “11010100” 400 mV  ...  “11011100” 500 mV  ...  “11100010” 600 mV</p>	“01010000”
<p><i>Note: If Reg93&lt;D1-D0&gt; is “IX” and Reg93&lt;D2&gt; is “0”.</i></p>		
<b>Reg101, 0x65</b>		
D7-D0	<p>Channel “D” IFA_Q output amplitude lower threshold control:</p> <p>“00000001” 5 mV  ...  “00000010” 10 mV  ...  “00100101” 50 mV  ...  “01001100” 93.5 mV  ...  “01010010” 100 mV  ...  “10100000” 200 mV  ...  “11000100” 300 mV  ...  “11010100” 400 mV  ...  “11011100” 500 mV  ...  “11100010” 600 mV</p>	“01001100”
<p><i>Note: If Reg93&lt;D1-D0&gt; is “IX” and Reg93&lt;D2&gt; is “0”.</i></p>		
<b>Reg102, 0x66</b>		
D7-D2	Unused	“000000”
D1-D0	<p>Channel “D” IFA output DC level:</p> <p>“00” 0.46*VCC  “01” 0.5*VCC  “10” 0.53*VCC  “11” 0.56*VCC</p>	“01”
<p><i>Note: If Reg93&lt;D2&gt; is “0”.</i></p>		

### Calibration and test section:

- IQ phase correction

Bit number	Description	Default
<b>Reg103, 0x67</b>		
D7-D6	Unused	“00”
Channel “D” IQ phase correction for FM band:		
	“000000” 76.3°	
	... ...	
D5-D0	“011111” 89.8°	“011111”
	“100000” 90°	
	“100001” 90.3°	
	... ...	
	“111111” 106.2°	
<b>Reg104, 0x68</b>		
D7-D6	Unused	“00”
Channel “D” IQ phase correction for VHF band:		
	“000000” 76°	
	... ...	
D5-D0	“011111” 89.8°	“011111”
	“100000” 90°	
	“100001” 90.2°	
	... ...	
	“111111” 101.8°	
<b>Reg105, 0x69</b>		
D7-D6	Unused	“00”
Channel “D” IQ phase correction for UHF band:		
	“000000” 74.3°	
	... ...	
D5-D0	“011111” 89.8°	“011111”
	“100000” 90°	
	“100001” 90.3°	
	... ...	
	“111111” 105.7°	
<b>Reg106, 0x6A</b>		
D7	Unused	“0”
Channel “D” IQ phase correction for L and S bands:		
	L band      S band	
	“0000000” 81.9°	77.4°
	“0000001” 82°	77.6°
	... ...	
D6-D0	“0111111” 89.9°	89.8°
	“1000000” 90°	90°
	“1000001” 90.1°	90.2°
	... ...	
	“1111110” 97.8°	102.2°
	“1111111” 98°	102.4°

## 4. OPERATING CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5...+3.9 V
Maximum input signal level	+10 dBm
Operating temperature range	-40...+85°C
Storage temperature	-55...+125°C
Junction temperature	+150°C
Soldering temperature	+260°C
Thermal resistance:	
• crystal-package	+28 °C/W
Electrostatic discharge rating:	
• HBM (pins 10, 13, 15, 17, 20, 21, 40, 41, 43, 44, 58, 59, 61, 62, 68, 69, 71, 72, 77, 78, 80, 81, 91, 94, 96, 98, 101, 103, 105, 108)	0.5 kV
• HBM (pins 74, 75)	1kV
• HBM (except pins 10, 13, 15, 17, 20, 21, 40, 41, 43, 44, 58, 59, 61, 62, 68, 69, 71, 72, 74, 75, 77, 78, 80, 81, 91, 94, 96, 98, 101, 103, 105, 108)	2 kV

### 4.1. DC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.8$  V to 3.6V,  $T_a = -40 \dots +85^\circ\text{C}$ . Typical values are at  $V_{cc} = 3.0$  V,  $T_a = +27^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Common						
Supply voltage	$V_{cc}$	-	2.8	3.0	3.6	V
Current consumption	$I_{cc}$	Mode 1.1 / Mode 1.2	-	94 / 100	-	mA
		Mode 2.1 / Mode 2.2	-	168 / 176	-	
		Mode 3.1 / Mode 3.2	-	164 / 172	-	
		Mode 4.1 / Mode 4.2	-	34 / 36	-	
		Mode 5.1 / Mode 5.2	-	89 / 90	-	
		Mode 6.1 / Mode 6.2	-	85 / 86	-	
	$I_{shd}$	Shutdown	-	-	1	uA
Die temperature measurement range	$T_j$	-	-40	+25	+100	°C
Die temperature measurement resolution	$\Delta T_j$	-	-	0.8	-	°C
Die temperature measurement accuracy	$\gamma T_j$	-	-	±5	-	°C
Input logic-level low	$V_{IL}$	-	0	-	0.3	V
Input logic-level high	$V_{IH}$	-	$V_{cc}-0.3$	-	$V_{cc}$	V
Output logic-level low	$V_{OL}$	$I_{LOAD}=100\mu\text{A}$	0	-	0.3	V
Output logic-level high	$V_{OH}$	$I_{LOAD}=100\mu\text{A}$	$V_{cc}-0.3$	-	$V_{cc}$	V
Output logic-level high (ADC output)	$V_{OH\_ADC}$	$I_{LOAD}=0 \text{ mA}/2 \text{ mA}$	Preset 1	-	1.8/1.7	V
			Preset 2	-	2.0/1.9	
			Preset 3	-	2.5/2.4	
			Preset 4	-	$V_{cc}/V_{cc}-0.2$	
Output logic-level low (ADC output)	$V_{OL\_ADC}$	$I_{LOAD}=2 \text{ mA}$	0	0.04	0.2	V
ADC external sampling frequency input DC level	$V_{DC\_FS}$	ECL	0.5	-	$V_{cc}-0.5$	V
Clock output DC level	$V_{DC\_CLK}$	ECL	Preset 1	-	$1.8 - V_{CLK}/4$	V
			Preset 2	-	$1.95 - V_{CLK}/4$	
			Preset 3	-	$2.7 - V_{CLK}/4$	
			Preset 4	-	$2.85 - V_{CLK}/4$	
		LVDS	-	1.2	-	

Table "DC electrical characteristics" (continue)

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
<b>Channels “A”, “B” and “C”</b>						
Active antenna output voltage drop	$\Delta V_{AA}$	From supply voltage $V_{cc}$ . $I_{AA}=10\text{mA}$ . <a href="#">Note 1</a>	-	0.12	-	V
Short-circuit protection current	$I_{AS}$	<a href="#">Preset 4. Note 2</a>	-	16.0	-	mA
Active antenna detection current	$I_{AW}$	<a href="#">Preset 4. Note 3</a>	-	1.8	-	mA
IFA output DC level	$V_{DC\_IFA\_ABC}$	-	-	$V_{cc}-1.34$	-	V
<b>Channel “D”</b>						
IFA output DC level	$V_{DC\_IFA\_D}$	<a href="#">Preset1</a>	-	$0.46*V_{cc}$	-	V
		<a href="#">Preset2</a>	-	$0.5*V_{cc}$	-	
		<a href="#">Preset3</a>	-	$0.53*V_{cc}$	-	
		<a href="#">Preset4</a>	-	$0.56*V_{cc}$	-	
RF gain control voltage	$V_{GC\_RF}$	Maximum gain	-	$V_{cc}$	-	V
		Minimum gain	-	0	-	
IF gain control voltage	$V_{GC\_IF}$	Maximum gain	-	$V_{cc}-0.1$	-	V
		Minimum gain	-	0.1	-	

**Notes:**

1. Voltage drop value is evaluated from the equation  $\Delta V = 0.1V + (2\Omega \times I_{AA})$ , where  $I_{AA}$  is active antenna current.
2. Current  $I_{AS} = I_{max}$ , where  $I_{max}$  is active antenna maximal current (for [Reg33<D7-D4>](#) for Channel “A” / [Reg55<D7-D4>](#) for Channel “B”/ [Reg77<D7-D4>](#) for Channel “C” = “0011”).
3. Current  $I_{AW} = I_{min}$ , where  $I_{min}$  is active antenna minimal current (for [Reg33<D7-D4>](#) for Channel “A” / [Reg55<D7-D4>](#) for Channel “B”/ [Reg77<D7-D4>](#) for Channel “C” = “0011”).

**Modes:**

1. **3 channels** (3 various combinations of L1/L2/L3/L5 bands, IQ GNSS @ PLL A, B, C)
  2. **4 channels** (3 various combinations of L1/L2/L3/L5 bands, IQ GNSS @ PLL A, B, C + S band or L2/L3/L5 band, IQ GNSS @ PLL D)
  3. **4 channels** (3 various combinations of L1/L2/L3/L5 bands, IQ GNSS @ PLL A, B, C + DGPS @ PLL D)
  4. **1 channel** (L1/L2/L3/L5 band, IQ GNSS @ PLL A/B/C)
  5. **1 channel** (S band or L2/L3/L5 band, IQ GNSS @ PLL D)
  6. **1 channel** (DGPS @ PLL D)
- \* .1 analog differential output  
\* .2 2-bit ADC output

## 4.2. AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.8$  V to 3.6V,  $T_a = -40 \dots +85^\circ\text{C}$ . Typical values are at  $V_{cc} = 3.0$  V,  $T_a = +27^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit			
			min	typ	max				
<b>Common</b>									
Reference frequency (TCXO) range	$F_{REF}$	-	10	10	50	MHz			
Reference signal input level	$REF_{IN}$	Sine or triangle wave	0.8	1	2	Vp-p			
ADC external input sampling frequency	FS	Can be applied to pins #52-53	10	-	120	MHz			
ADC external sampling signal input level	$FS_{IN}$	ECL	0.4	-	-	Vp-p			
		CMOS	0.4	-	1.2				
		LVDS	0.1	-	0.5				
Clock frequency	$F_{CLK}$	$F_{VCO}/2C = F_{LO}/C$ , where C = <a href="#">Reg11&lt;7:0&gt;</a>	10	72.27	120	MHz			
Peak-to-peak voltage at the clock output	$V_{CLK}$	ECL, $C_{LOAD} = 5\text{pF}$	Preset1	-	320	mVp-p			
			Preset2	-	420				
			Preset3	-	600				
			Preset4	-	690				
		CMOS, $C_{LOAD} = 5\text{pF}$	Preset1	-	1.8	Vp-p			
			Preset2	-	1.95				
			Preset3	-	2.7				
			Preset4	-	2.85				
			Preset5	-	$V_{CC}-0.1$				
	$V_{CLK}$	LVDS	Preset1	-	320	mVp-p			
			Preset2	-	480				
			Preset3	-	640				
			Preset4	-	800				
<b>Channels “A”, “B” and “C”</b>									
<b>Overall</b>									
Input frequency range	$F_{IN\_ABC}$	L1 band		1530	-	1620	MHz		
		L2, L3, L5 band		1150	-	1300			
Total gain	$G_{ABC}$	Referred to LNA1 input		-	99	-	dB		
		Referred to LNA2 input		-	87	-			
Noise figure	$NF_{ABC}$	$G_{IFA} = \min$	Referred to LNA1 input	-	1.35	-	dB		
			Referred to LNA2 input	-	6	-			
			Referred to mixer input	-	8.8	-			
1dB compression point	$P_{1dB\_ABC}$	$G_{IFA} = \min$	Referred to LNA1 input	-	-50	-	dBm		
			Referred to LNA2 input	-	-38	-			
			Referred to mixer input	-	-31	-			
<b>LNA1</b>									
LNA1 noise figure	$NF_{LNA1}$	-		-	1.1	-	dB		
LNA1 gain	$G_{LNA1}$	-		-	19.3	-	dB		
LNA1 input VSWR	$VSWR_{LNA1\_IN}$	With matching circuit	@50Ohm	-	1.5	-	-		
LNA1 output VSWR	$VSWR_{LNA1\_OUT}$	L1 band	@50Ohm	-	1.4	-	-		
		L2, L3, L5 band		-	1.5	-			
LNA1 input 1dB compression point	$P_{1dB\_LNA1}$	L1 band		-	-20.4	-	dBm		
		L2, L3, L5 band		-	-22.3	-			
LNA1 3 <sup>rd</sup> order intercept point	$IIP3_{LNA1}$	L1 band	L2, L3, L5 band	-	-5	-	dBm		
		L2, L3, L5 band		-	-7	-			
<b>LNA2</b>									
LNA2 noise figure	$NF_{LNA2}$	-		-	4.6	-	dB		
LNA2 gain	$G_{LNA2}$	-		-	7.8	-	dB		

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
LNA2 input VSWR	VSWR <sub>LNA2_IN</sub>	L1 band	-	1.3	-	-
		L2, L3, L5 band	@50Ω	-	1.6	
LNA2 output VSWR	VSWR <sub>LNA2_OUT</sub>	L1 band	-	1.4	-	-
		L2, L3, L5 band	@50Ω	-	1.5	
LNA2 input 1dB compression point	P <sub>1dB_LNA2</sub>	L1 band	-	5	-	dBm
		L2, L3, L5 band	-	6	-	
LNA2 3 <sup>rd</sup> order intercept point	IIP3 <sub>LNA2</sub>	L1 band	-	0.7	-	dBm
		L2, L3, L5 band	-	4.4	-	
<b>Mixer&amp;Polyphase filter</b>						
Mixer&Polyphase filter gain	G <sub>MIX_ABC</sub>	-	-	24	-	dB
Mixer input VSWR	VSWR <sub>IN_MIX_ABC</sub>	@50Ω	-	2	-	-
Image rejection	IR <sub>ABC</sub>	Optionally. <a href="#">Channel# mode</a> ≠ "00".	-	25	-	dB
<b>LPF&amp;IFA</b>						
Output frequency range	F <sub>IF_ABC</sub>	Tunable, assured/not guaranteed	2	-	30 / 37	MHz
LPF 3dB cut-off frequency	F <sub>cut_LPF_ABC</sub>	Tunable, assured/not guaranteed	9.5 / 14	-	30 / 37	MHz
IF (LPF&IFA) gain	G <sub>IF_ABC</sub>	Assured/not guaranteed	1	-	56 / 67	dB
IF AGC range	ΔG <sub>IF_ABC</sub>	Assured	-	55	-	dB
Stopband attenuation	S <sub>A_ABC</sub>	F <sub>cut_LPF_ABC</sub> = 30MHz	F = 60 MHz	-	18	-
			F = 90 MHz	-	30	-
Sinusoidal/noise signal peak-to-peak voltage at the differential linear outputs	V <sub>p-p_ABC</sub>	510 Ohm load resistance. <a href="#">Note 1</a>	-	200/ 480	-	mV
IQ phase imbalance	Δφ <sub>ABC</sub>	-	-	±1	±3	degree
IQ amplitude output voltage imbalance	ΔA <sub>ABC</sub>	-	-	-	20	mV
Group time delay ripple	ΔT <sub>GD_ABC</sub>	F <sub>IF</sub> = 2 - 9.5 MHz, F <sub>cut_LPF</sub> = 9.5 MHz	-	10	-	ns
		F <sub>IF</sub> = 2 - 30 MHz, F <sub>cut_LPF</sub> = 30 MHz	-	11	-	
<b>ADC</b>						
ADC resolution	R <sub>ADC</sub>	-	-	2	-	bit
Output logic-level high (ADC output)	V <sub>OH_ADC</sub>	I <sub>LOAD</sub> =0mA/2mA	Preset 1	-	1.8/1.7	V
			Preset 2	-	2.0/1.9	
			Preset 3	-	2.5/2.4	
			Preset 4	-	V <sub>cc</sub> / V <sub>cc</sub> -0.2	
<b>Synthesizer</b>						
LO frequency range	F <sub>LO_ABC</sub>	L1 band	1550	-	1615	MHz
		L2, L3, L5 band	1160	-	1300	
VCO frequency range	F <sub>VCO_ABC</sub>	L1 band	3100	-	3230	MHz
		L2, L3, L5 band	2320	-	2600	
VCO to PFD frequency integer-valued division ratio	N <sub>ABC</sub>	-	16	-	4095	
VCO to PFD frequency fraction-valued division resolution	F <sub>ABC</sub>	-	-	24	-	bit
Quadrature former division ratio	QF <sub>ABC</sub>	-	-	2	-	-
VCO to CLK frequency integer-valued division ratio	C <sub>ABC</sub>	-	4	-	255	-
TCXO to PFD frequency integer-valued division ratio	R <sub>ABC</sub>	-	1	-	31	-

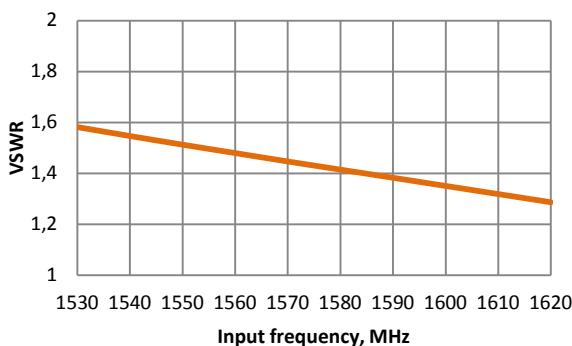
Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
LO phase noise	PN <sub>LO_ABC</sub>	At 10 kHz offset, F <sub>PFD</sub> =10 MHz	L1 band	-	-98	-
			L2, L3, L5 band	-	-100	-
		At 100 kHz offset, F <sub>PFD</sub> =10 MHz	L1 band	-	-94	-
			L2, L3, L5 band	-	-95	-
		At 1 MHz offset, F <sub>PFD</sub> =10 MHz	L1 band	-	-112	-
			L2, L3, L5 band	-	-106	-
LO RMS jitter	J <sub>RMS_ABC</sub>	L1 band	-	1.4	-	ps
		L2, L3, L5 band	-	2.2	-	
PFD frequency range	F <sub>CMP_ABC</sub>	-	1	-	50	MHz
<b>Channel "D"</b>						
<b>Overall</b>						
Input frequency range	F <sub>IN_D</sub>	FM	65	-	110	MHz
		VHF	160	-	240	
		UHF	470	-	862	
		L2, L3, L5 band	1160	-	1300	
		S band	2330	-	2590	
Total gain	G <sub>D</sub>	FM	-	98.5	-	dB
		VHF	-	95.5	-	
		UHF	-	93.4	-	
		L2, L3, L5 band	-	97.5	-	
		S band	-	95.5	-	
Noise figure	NF <sub>D</sub>	FM	-	2.8	-	dB
		VHF	-	3.3	-	
		UHF	-	4.0	-	
		L2, L3, L5 band	-	3.4	-	
		S band	-	4.5	-	
1dB compression point	P <sub>1dB_D</sub>	FM	-	-43.4	-	dBm
		VHF	-	-40.7	-	
		UHF	-	-38.5	-	
		L2, L3, L5 band	-	-37.6	-	
		S band	-	-36.4	-	
Input VSWR	VSWR <sub>IN_D</sub>	FM	-	1.1	-	-
		VHF	-	1.2	-	
		UHF	-	1.2	-	
		L2, L3, L5 band	-	1.9	-	
		S band	-	1.8	-	
<b>LNA&amp;Mixer</b>						
RF gain	G <sub>RF_D</sub>	FM	-7.7	-	31.3	dB
		VHF	-11.8	-	28.2	
		UHF	-4.9	-	26	
		L2, L3, L5 band	-6.8	-	27.5	
		S band	-6.4	-	25.5	
RF AGC range	ΔG <sub>RF_D</sub>	FM	-	39	-	dB
		VHF	-	40	-	
		UHF	-	30.9	-	
		L2, L3, L5 band	-	34.3	-	
		S band	-	31.9	-	
<b>LPF&amp;IFA</b>						
Output frequency range	F <sub>IF_D</sub>	Tunable, assured/not guaranteed	0.05	-	11 / 14	MHz
LPF 3dB cut-off frequency	F <sub>cut_LPF_D</sub>	Tunable, assured/not guaranteed	2.6 / 3	-	11 / 14	MHz
IFA gain	G <sub>IFA_D</sub>	Assured/not guaranteed	-6	-	70 / 74	dB
IFA AGC range	ΔG <sub>IFA_D</sub>	Assured	-	76	-	dB

Parameter	Symbol	Condition		Value			Unit	
				min	typ	max		
Stopband attenuation	$S_{A\_D}$	$F_{cut\_LPF\_D} = 11 \text{ MHz}$	$F = 22 \text{ MHz}$	-	40	-	dB	
			$F = 33 \text{ MHz}$	-	70	-		
Sinusoidal signal peak-to-peak voltage at the differential linear outputs	$V_{p-p\_D}$	Minimal	Note 1	-	50	-	mV	
		Default		-	430	-		
		Maximal		-	1200	-		
Output impedance	$R_{out\_D}$	Analog differential output		-	1.5	-	kΩ	
IQ phase imbalance	$\Delta\phi_D$	FM, VHF, UHF		-	±2	-	degree	
		L2, L3, L5 band, S band		-	±5	-		
IQ amplitude output voltage imbalance	$\Delta A_D$	$V_{p-p\_D} = 50 \text{ mV}$		-	12	-	mV	
		$V_{p-p\_D} = 430 \text{ mV}$		-	35	-		
		$V_{p-p\_D} = 1200 \text{ mV}$		-	45	-		
Group time delay ripple	$\Delta T_{GD\_D}$	$F_{IF} = 0.05 - 3 \text{ MHz}, F_{cut\_LPF\_D} = 3 \text{ MHz}$		-	150	-	ns	
		$F_{IF} = 0.05 - 11 \text{ MHz}, F_{cut\_LPF\_D} = 11 \text{ MHz}$		-	50	-		
<b>ADC</b>								
ADC resolution	$R_{ADC}$	-		-	2	-	bit	
Output logic-level high (ADC output)	$V_{OH\_ADC}$	$I_{LOAD}=0 \text{ mA}/2 \text{ mA}$	Preset 1	-	1.8/1.7	-	V	
			Preset 2	-	2.0/1.9	-		
			Preset 3	-	2.5/2.4	-		
			Preset 4	-	$V_{cc} / V_{cc}-0.2$	-		
<b>Synthesizer</b>								
LO frequency range	$F_{LO\_D}$	FM		65	-	110	MHz	
		VHF		160	-	240		
		UHF		470	-	862		
		L2, L3, L5 band		1170	-	1290		
		S band		2340	-	2580		
VCO frequency range	$F_{VCO\_D}$	VCO 1	FM, VHF, UHF	900	-	1300	MHz	
		VCO 2		1250	-	1820		
		VCO 3	L2, L3, L5 band and S band	4680	-	5160		
VCO to PFD frequency integer-valued division ratio	$N_D$	FM, VHF, UHF		16	-	1023	-	
		L2, L3, L5 band and S band		56	-	2047		
VCO to PFD frequency fraction-valued division resolution	$F_D$	-		-	24	-	bit	
Quadrature former division ratio	$QF_D$	-		-	2	-	-	
VCO to LO frequency integer-valued preliminary division ratio	$QF_{PREDIV\_D}$	FM		-	8	-	-	
		VHF	160-227.5 MHz	-	4	-		
			225-240 MHz	-	2	-		
		UHF		-	1	-		
		L2, L3, L5 band		-	2	-		
		S band		-	1	-		
TCXO to PFD frequency integer-valued division ratio	$R_D$	-		1	-	31	-	
LO phase noise	$PN_{LO\_D}$	At 10 kHz offset, $F_{PFD} = 10 \text{ MHz}$	FM	-	-103	-	dBc/Hz	
			VHF	-	-95	-		
			UHF	-	-86	-		
			L2, L3, L5 band	-	-88	-		
			S band	-	-80	-		
		At 100 kHz offset, $F_{PFD} = 10 \text{ MHz}$	FM	-	-105	-		
			VHF	-	-97	-		
			UHF	-	-85	-		
			L2, L3, L5 band	-	-89	-		
			S band	-	-82	-		

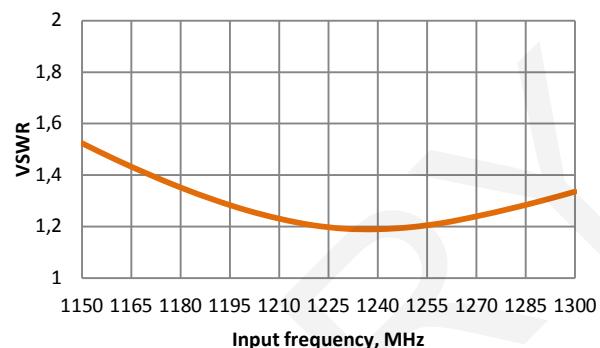
Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
LO phase noise	PN <sub>LO_D</sub>	At 1 MHz offset, F <sub>PFD</sub> = 10 MHz	FM	-	-129	-
			VHF	-	-121	-
			UHF	-	-109	-
			L2, L3, L5 band	-	-114	-
			S band	-	-115	-
LO RMS jitter	F <sub>CMP_D</sub>	FM	-	4.2	-	ps
		VHF	-	4.9	-	
		UHF	-	6.2	-	
		L2, L3, L5 band	-	6.0	-	
		S band	-	6.0	-	
PFD frequency range	J <sub>RMS_D</sub>	-	1	-	50	MHz

Note 1: RMS value measured.  $V_{p-p \sin} = V_{RMS} * 2\sqrt{2}$ ;  $V_{p-p \text{ noise}} = V_{RMS} * 6.6$ . In Channel "D" Vp-p noise can be calculated only for signals in L2/S band.

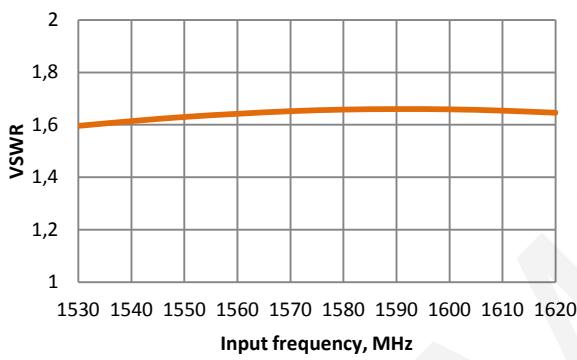
## 5. TYPICAL CHARACTERISTICS



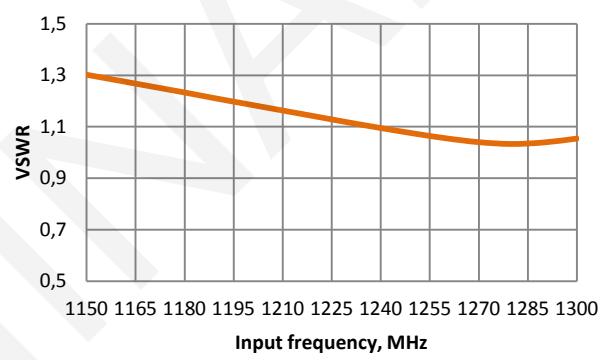
**Figure 5.1:** Input VSWR vs. Input frequency  
Conditions: Channels “A”, “B”, “C”; LNA1 input; L1 band



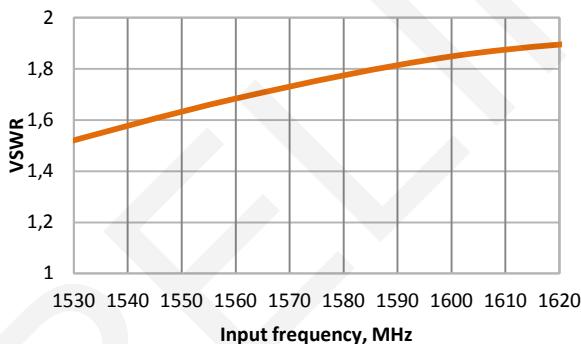
**Figure 5.2:** Input VSWR vs. Input frequency  
Conditions: Channels “A”, “B”, “C”; LNA1 input; L2, L3, L5 bands



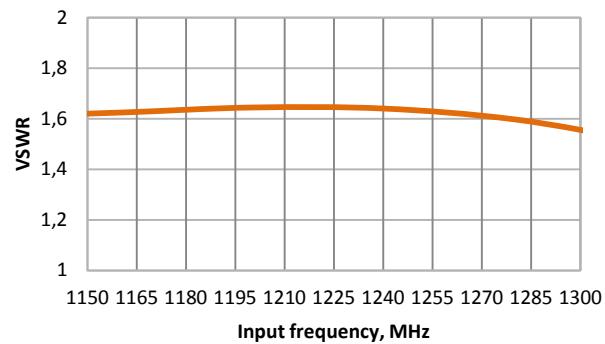
**Figure 5.3:** Input VSWR vs. Input frequency  
Conditions: Channels “A”, “B”, “C”; LNA2 input; L1 band



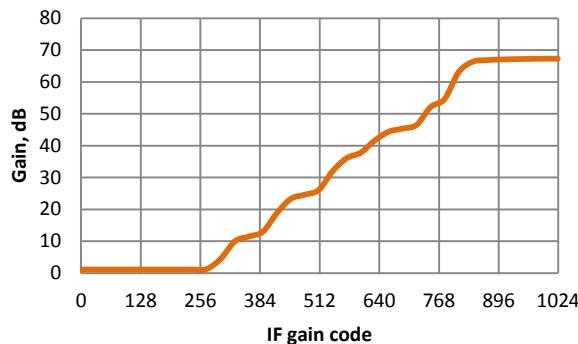
**Figure 5.4:** Input VSWR vs. Input frequency  
Conditions: Channels “A”, “B”, “C”; LNA2 input; L2, L3, L5 bands



**Figure 5.5:** Input VSWR vs. Input frequency  
Conditions: Channels “A”, “B”, “C”; mixer input; L1 band



**Figure 5.6:** Input VSWR vs. Input frequency  
Conditions: Channels “A”, “B”, “C”; mixer input; L2, L3, L5 bands



**Figure 5.7:** IF gain vs. code  
Conditions: Channels “A”, “B”, “C”

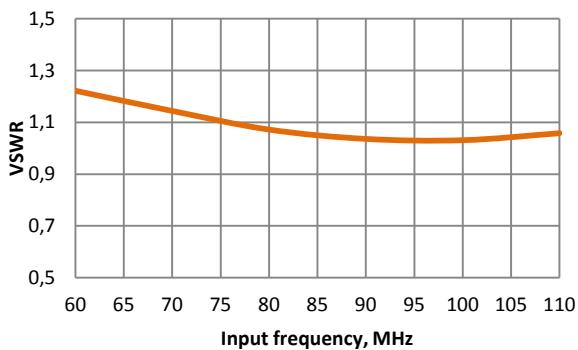


Figure 5.8: Input VSWR vs. Input frequency  
Conditions: Channel “D”; FM band

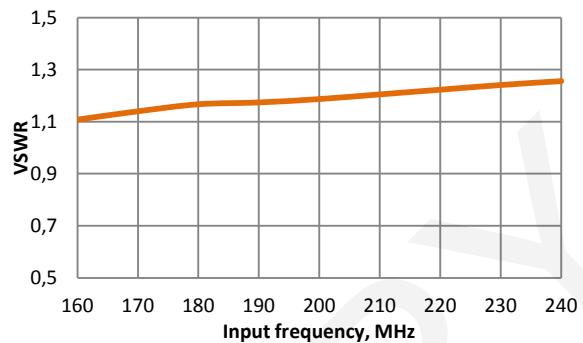


Figure 5.9: Input VSWR vs. Input frequency  
Conditions: Channel “D”; VHF band

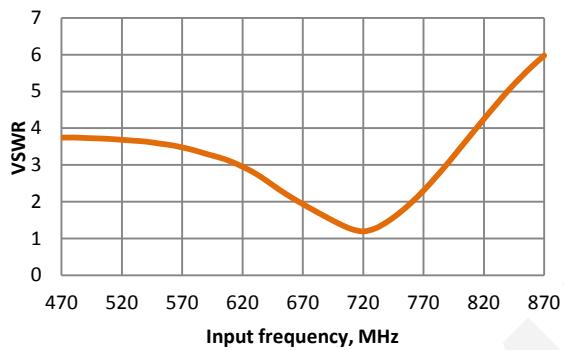


Figure 5.10: Input VSWR vs. Input frequency  
Conditions: Channel “D”; UHF band

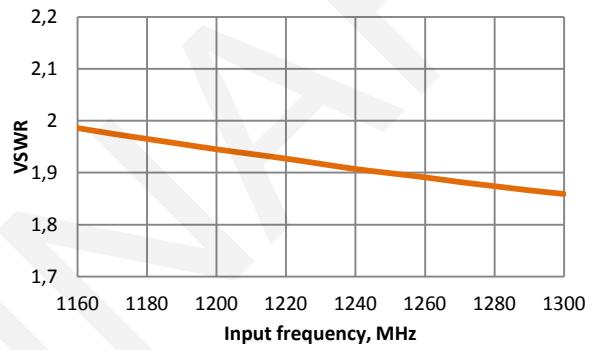


Figure 5.11: Input VSWR vs. Input frequency  
Conditions: Channel “D”; L band

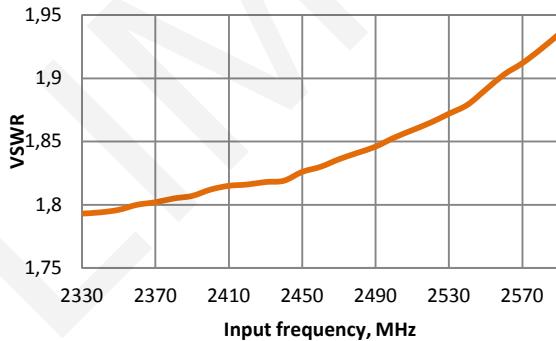


Figure 5.12: Input VSWR vs. Input frequency  
Conditions: Channel “D”; S band

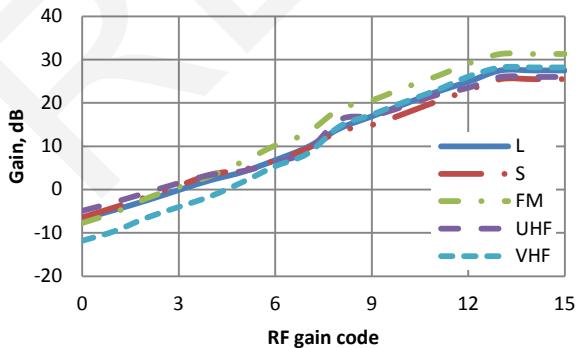


Figure 5.13: RF gain vs. code  
Conditions: Channel “D”

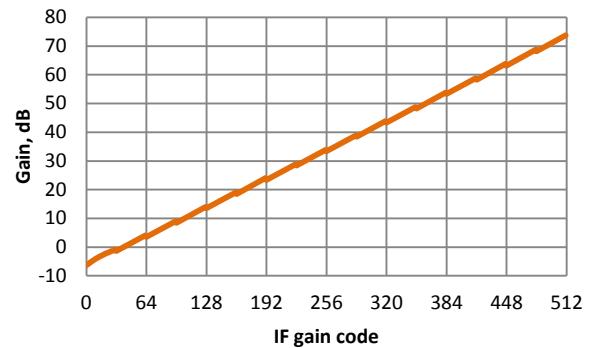
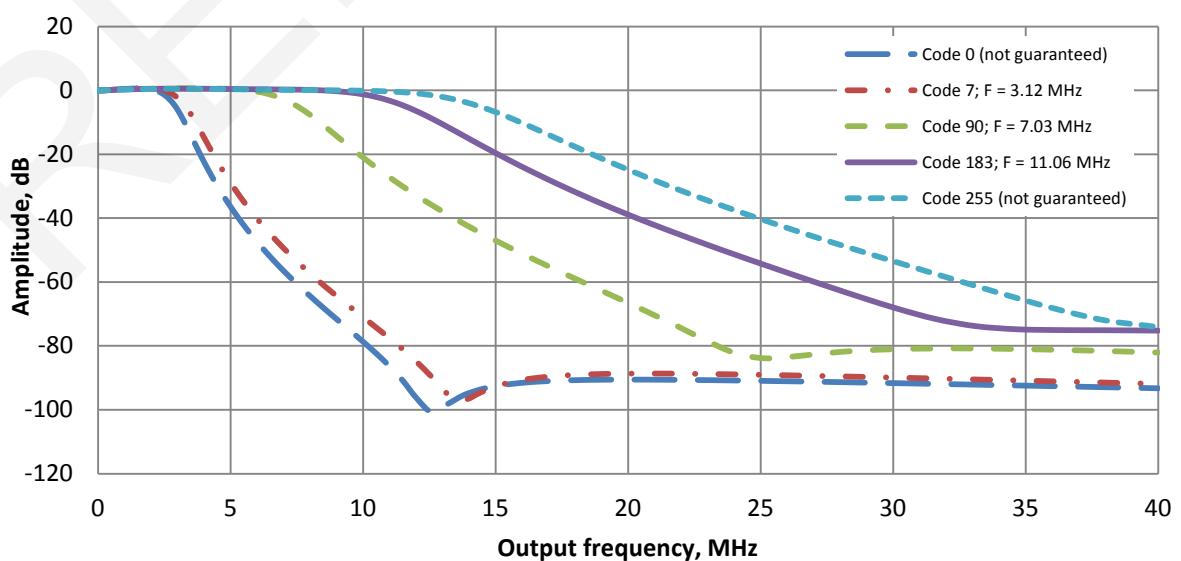
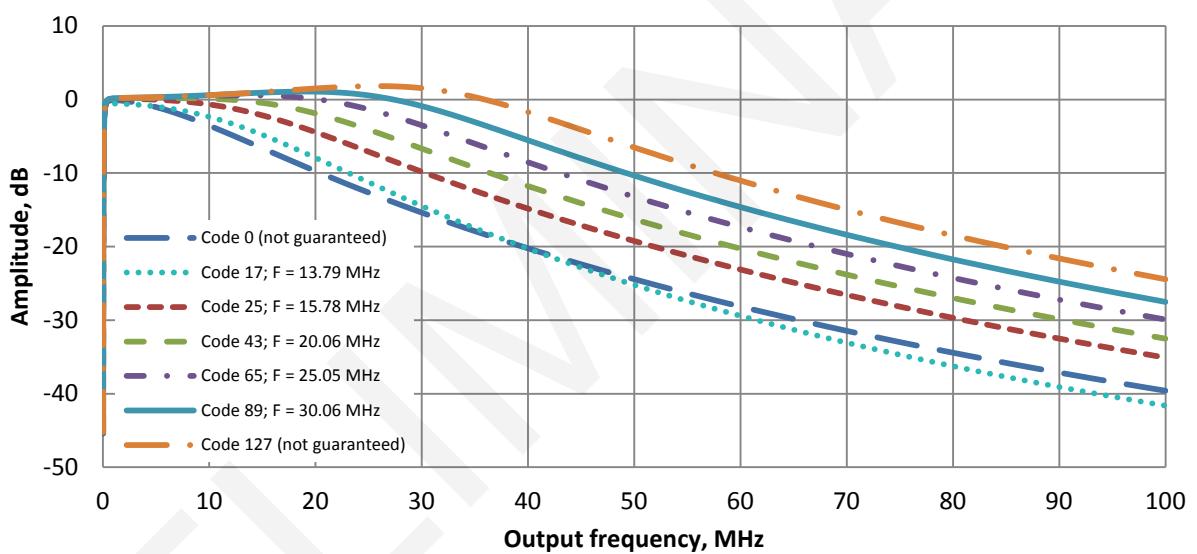
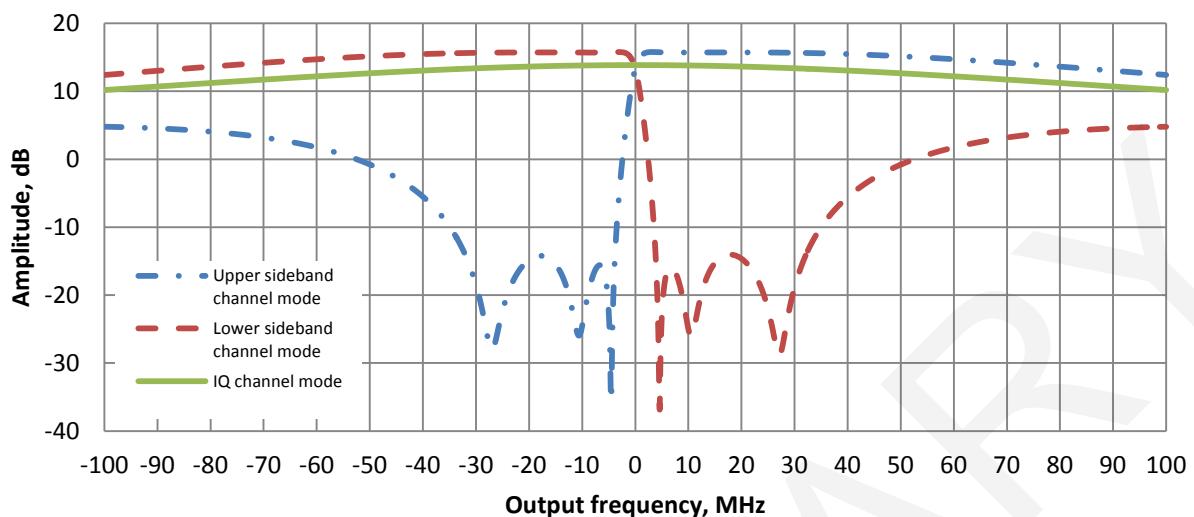
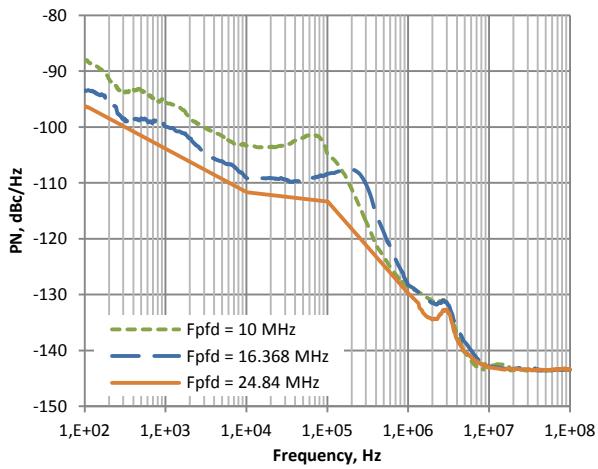
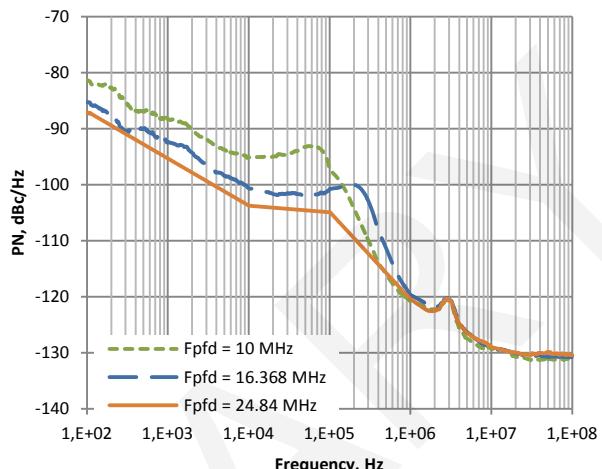


Figure 5.14: IF gain vs. code  
Conditions: Channel “D”

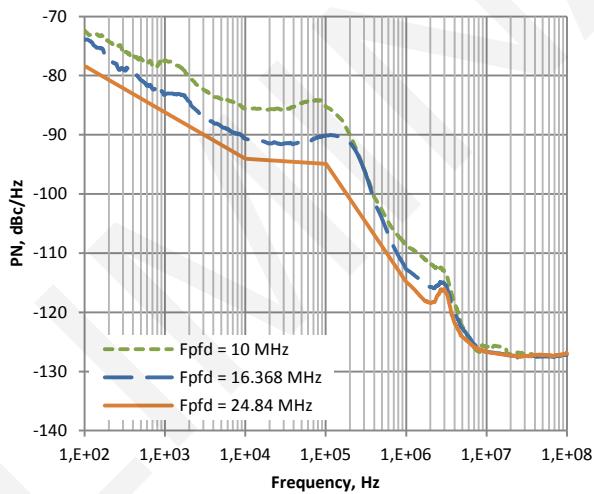




**Figure 5.18:**Typical LO phase noise  
Conditions: Channel “D”; FM band,  $F_{LO} = 87$  MHz



**Figure 5.19:**Typical LO phase noise  
Conditions: Channel “D”; VHF band,  $F_{LO} = 200$  MHz



**Figure 5.20:**Typical LO phase noise  
Conditions: Channel “D”; UHF band,  $F_{LO} = 690$  MHz

## 5.1. TYPICAL S11 PARAMETERS

Will be added in new versions of datasheet.

## 5.2. IBIS MODEL

Will be added in new versions of datasheet.

## 6. APPLICATION NOTES

Some tricks or not obvious actions as well as configuration examples are described in this section.

### 6.1. START UP

NT1066 wakes up in shutdown mode: all channels and clock output are disabled. You can reconfigure NT1066 according to sequences given below. In order to activate chip one of the channels (**Reg6 D[3-0]**) or clock output (**Reg6 D[4]**) should be enabled. If reconfiguration is not required, enable required channels, execute PLL tuning and LPF autocalibration procedures and start working.

### 6.2. REFERENCE FREQUENCY

NT1066 is preconfigured to 10MHz TCXO signal. If another TCXO is used, its value should be written to **Reg7 D[7-0] + Reg8 D[7-0]** to make NT1066 perform properly.

### 6.3. PLL RECONFIGURATION

NT1066 has the following preconfigures:

- PLL “A” is set to L1 band and feeds channel “A” with LO=1590MHz @  $F_{TCXO}=10\text{MHz}$
- PLL “B” is set to L2 band and feeds channel “B” with LO=1235MHz @  $F_{TCXO}=10\text{MHz}$
- PLL “C” is set to L3/L5 bands and feeds channel “C” with LO=1190MHz @  $F_{TCXO}=10\text{MHz}$
- PLL “D” is set to S band and feeds channel “D” with LO=2492MHz @  $F_{TCXO}=10\text{MHz}$

In order to reconfigure PLL “A”, “B” and “C” the following procedure is recommended:

- write LO frequency value to **Reg17 D[6-0] + Reg18 D[7-0] + Reg19 D[7-0]** for channel “A”, to **Reg39 D[6-0] + Reg40 D[7-0] + Reg41 D[7-0]** for channel “B” and to **Reg61 D[6-0] + Reg62 D[7-0] + Reg63 D[7-0]** for channel “C”
- choose PLL mode: integer-N or fractional-N in **Reg20 D[0]** for channel “A”, in **Reg42 D[0]** for channel “B” and in **Reg64 D[0]** for channel “C”
- if integer-N mode:
  - o choose  $R$ , than  $N$  values according to the formula:  $F_{LO} = \frac{F_{TCXO}*N}{2R}$
  - o write  $R$  value to **Reg21 D[4-0]** for channel “A”, to **Reg43 D[4-0]** for channel “B” and to **Reg65 D[4-0]** for channel “C”
  - o write  $N$  value to **Reg22 D[3-0] + Reg23 D[7-0]** for channel “A”, to **Reg44 D[3-0] + Reg45 D[7-0]** for channel “B” and to **Reg66 D[3-0] + Reg67 D[7-0]** for channel “C”
- execute a tuning procedure in **Reg24 D[0]** for channel “A”, in **Reg46 D[0]** for channel “B” and in **Reg68 D[0]** for channel “C”

In order to reconfigure PLL “D” the following procedure is recommended:

- write LO frequency value to **Reg87 D[6-0] + Reg88 D[7-0] + Reg89 D[7-0]**
- execute a tuning procedure in **Reg90 D[0]**

It is necessary to execute tuning procedure for each PLL if TCXO frequency was changed.

PLL lock indicator is available at **Reg14 D[5]** for channel “A”, at **Reg35 D[5]** for channel “B”, at **Reg56 D[5]** for channel “C” and at **Reg80 D[0]** for channel “D”.

Crossing of VCO voltage comparator upper threshold will be indicated by **Reg14 D[4]** for channel “A”, by **Reg37 D[4]** for channel “B”, by **Reg60 D[4]** for channel “C” and by **Reg80 D[2]** for channel “D”.

Crossing of VCO voltage comparator lower threshold will be indicated by **Reg14 D[3]** for channel “A”, by **Reg36 D[3]** for channel “B”, by **Reg58 D[3]** for channel “C” and by **Reg80**

D[1] for channel “D”.

## 6.4. CHANNEL MODE CONFIGURATION

Channels “A”, “B” and “C” can operate in the following modes:

- IQ mode
- Lower sideband real mode
- Upper sideband real mode
- Lower sideband + upper sideband real mode

These modes can be set up in **Reg16 D[1-0]** for channel “A”, in **Reg38 D[1-0]** for channel “B”, **Reg60 D[1-0]** for channel “C”. Channels “A”, “B” and “C” are preconfigured to IQ mode.

Channel “D” operates only in IQ mode.

## 6.5. RF AGC CONFIGURATION

RF GC system of NT1066 in channel “D” starts into the manual operation mode (**Reg91 D[1-0]** is set to “00”). You can change RF gain value manually by setting a corresponding value with **Reg91 D[6-3]**.

To enable the automatic mode **Reg91 D[1-0]** should be switched to “01”. In this case the RF GC system adjusts the RF gain to keep its output power between RF AGC thresholds.

The status of RF gain control register is available at **Reg81 D[3-0]**.

In order to control RF gain externally **Reg91 D[1-0]** should be switched to “10”.

## 6.6. LPF CALIBRATION

LPF autocalibration system is available for channels “A”, “B” and “C”.

LPF automated calibration procedure is intended to compensate influence of temperature dependence and technological scatter on LPF characteristics. In **Reg25 D[6-0]** and **Reg26 D[6-0]** for channel “A”, **Reg47 D[6-0]** and **Reg48 D[6-0]** for channel “B”, **Reg69 D[6-0]** and **Reg70 D[6-0]** for channel “C” and **Reg92 D[7-0]** for channel “D” guaranteed range of LPF cut-off frequency is described for typical conditions. On marginal samples autocalibration system will compensate offset either in low-frequency range or in high-frequency range. After autocalibration you will get 3dB attenuation at the selected setting of guaranteed range for any chip in the specified temperature range.

LPF cut-off frequency should be the same for I and Q channels if complex output type. If output type is real, LPF cut-off frequency can be different for upper and lower sideband.

It is necessary to execute LPF autocalibration procedure in **Reg27 D[0]** for channel “A”, in **Reg49 D[0]** for channel “B” and in **Reg71 D[0]** for channel “C” and in after chip activation or if TCXO frequency was changed. LPF autocalibration system status is available in **Reg14 D[0]** for channel “A”, in **Reg36 D[0]** for channel “B” and in **Reg58 D[0]** for channel “C”.

## 6.7. IF AGC THRESHOLD CONFIGURATION

IF GC system of NT1066 has the differences between the channels.

In channels “A”, “B” and “C” IF GC systems start into the auto operation mode with 2-bit ADC IF outputs. You can change digital detector threshold with respect to sinewave signal with **Reg29 D[1-0] + Reg30 D[7-0]** and **Reg31 D[1-0] + Reg32 D[7-0]** for channel “A”, **Reg51 D[1-0] + Reg52 D[7-0]** and **Reg53 D[1-0] + Reg54 D[7-0]** for channel “B” and **Reg73 D[1-0] + Reg74 D[7-0]** and **Reg75 D[1-0] + Reg76 D[7-0]** for channel “C”.

To enable manual mode set “1” to **Reg28 D[1]** for channel “A”, **Reg50 D[1]** for channel “B” and **Reg72 D[1]** for channel “C”. You can change IF gain value manually by setting a corresponding value with **Reg29 D[1-0] + Reg30 D[7-0]** and **Reg31 D[1-0] + Reg32 D[7-0]** for channel “A”,

**Reg51 D[1-0] + Reg52 D[7-0]** and **Reg53 D[1-0] + Reg54 D[7-0]** for channel “B” and **Reg73 D[1-0] + Reg74 D[7-0]** and **Reg75 D[1-0] + Reg76 D[7-0]** for channel “C”.

In channel “D” IF GC system starts into the auto operation mode with 2-bit ADC IF outputs. You can change digital detector threshold with respect to sinewave signal with **Reg94 D[0] + Reg95 D[7-0]** and **Reg96 D[0] + Reg97 D[7-0]**.

While automatic mode is enabled, the IF AGC system adjusts the IF gain to keep its output power between IF AGC thresholds.

The thresholds correspond to the definite voltage level of the output stage. An upper threshold could be adjusted by **Reg98 D[7-0]** and **Reg100 D[7-0]**. A lower threshold could be adjusted by **Reg99 D[7-0]** and **Reg101 D[7-0]**. Voltage values shown in registers description (section 3.4.2.5) are calculated with respect to output signal power. The upper threshold should always be higher than lower. Also it is strongly recommended to set a code value of upper threshold at least 5 codes higher than lower threshold to guarantee stability of IF AGC loop.

The IF AGC thresholds can be changed in order to achieve the desired output level for the subsequent ADC.

It is strongly recommended not to change thresholds if digital output is selected.

The status of IF gain control register is available in **Reg82 D[0] + Reg83 D[7-0]** and **Reg84 D[0] + Reg85 D[7-0]**.

To enable manual mode the **Reg93 D[1-0]** should be switched to “0X”. You can change IF gain value manually by setting the corresponding value with **Reg94 D[0] + Reg95 D[7-0]** and **Reg96 D[0] + Reg97 D[7-0]**.

To enable an external control mode **Reg93 D[1-0]** should be switched to “10”.

## 6.8. 2-BIT ADC CONFIGURATION

After power up NT1066 is preconfigured to 2-bit ADC output data interface. However, there is an option to set up analog differential outputs in **Reg28 D[0]** for channel “A”, **Reg50 D[0]** for channel “B”, **Reg72 D[0]** for channel “C” and **Reg93 D[2]** for channel “D”. 2-bit ADCs are able to operate in one of three modes:

- asynchronous
- clocked by rising edge
- clocked by falling edge

These modes can be set up in **Reg28 D[5-4]** for channel “A”, in **Reg50 D[5-4]** for channel “B”, in **Reg72 D[5-4]** for channel “C” and in **Reg93 D[6-5]** for channel “D”. For ADCs sampling frequency information, please, refer to the corresponding subsection. In ‘asynchronous’ mode 2-bit ADCs act as voltage level comparators so no any clocking applied. For example, this mode may be useful if several NT1066s should operate simultaneously pushing out digitized data that can be synchronized with single clock on correlator and processor side.

## 6.9. ACTIVE ANTENNA DETECTOR SYSTEM CONFIGURATION

Active antenna detector system is available in channels “A”, “B” and “C”.

Channels “A”, “B”, “C” can operate either with external active antenna or without it. Active antenna detector is intended to detect whether active antenna is connected and whether its current is within acceptable thresholds. If current indicator is valid, you can change current thresholds with **Reg33 D[7-4]** for channel “A”, with **Reg55 D[7-4]** for channel “B” and with **Reg77 D[7-4]** for channel “C”.

Active antenna connection indicator is available in **Reg14 D[2]** for channel “A”, in **Reg36 D[2]** for channel “B” and in **Reg58 D[2]** for channel “C”. Active antenna current indicator is available

in **Reg14 D[1]** for channel “A”, in **Reg36 D[1]** for channel “B” and in **Reg58 D[1]** for channel “C”.

Autoselection permission allows to select active LNA automatically if active antenna detector is enabled. LNA1 and LNA2 status are available in **Reg14 D[7-6]** for channel “A”, in **Reg36 D[7-6]** for channel “B” and in **Reg58 D[7-6]** for channel “C”.

In order to select required LNA manually the following registers should be switched to ‘0’: **Reg34 D[3]** for channel “A”, **Reg56 D[3]** for channel “B” and **Reg78 D[3]** for channel “C”. In this case you should firstly enable LNA in **Reg34 D[1]** for channel “A”, in **Reg56 D[1]** for channel “B” and in **Reg78 D[1]** for channel “C” and then select LNA type in **Reg34 D[0]** for channel “A”, in **Reg56 D[0]** for channel “B” and in **Reg78 D[0]**.

There is an option to disable active antenna detector, it can be done in **Reg34 D[2]** for channel “A”, in **Reg56 D[2]** for channel “B” and in **Reg78 D[2]** for channel “C”. In this case LNA autoselection will be unavailable and you will have to select LNA manually according to the sequence given above.

If upper threshold of active antenna detector is exceeded, i.e. active antenna current is too high, detector can behave in two possible ways: limit current according to the preset threshold or limit current according to the minimum possible threshold. Active antenna detector behavior can be changed in **Reg33 D[0]** for channel “A”, in **Reg55 D[0]** for channel “B” and in **Reg77 D[0]** for channel “C”.

## 6.10. CLK FREQUENCY CONFIGURATION

CLK signal is intended for clocking all 2-bit ADCs as well as clocking external correlator engine. It can be generated from the following sources:

- LO frequency either from PLL “A” or PLL “B” or PLL “C” according to the formula:  
 $F_{CLK} = F_{LO}/C$
- TCXO reference signal pass-through
- external sampling frequency via pins 52-53

At default setup clock source is PLL “A” and its value is 72.3MHz.

CLK source and frequency can be customized by procedure:

- choose CLK source by setting appropriate value to **Reg10 D[2-0]**
- write C value to **Reg11 D[7-0]** if PLL “A”, PLL “B” or PLL “C” source

## 6.11. CLK OUTPUT TYPE USAGE

Although CMOS output is available for usage it is recommended to select LVDS CLK output. It is related to appearing of interferences at the **Ch#\_LNA\_IN** pins and then down converting to IF band. These interferences are caused by CLK signal harmonics and allocated frequencies can be calculated as  $F_{jam} = N * F_{CLK}$ ,  $N = 1,2,3,4 \dots$ .

Clock output type can be changed in **Reg10 D[4-3]**.

## 6.12. TEMPERATURE MEASUREMANT PROCEDURE

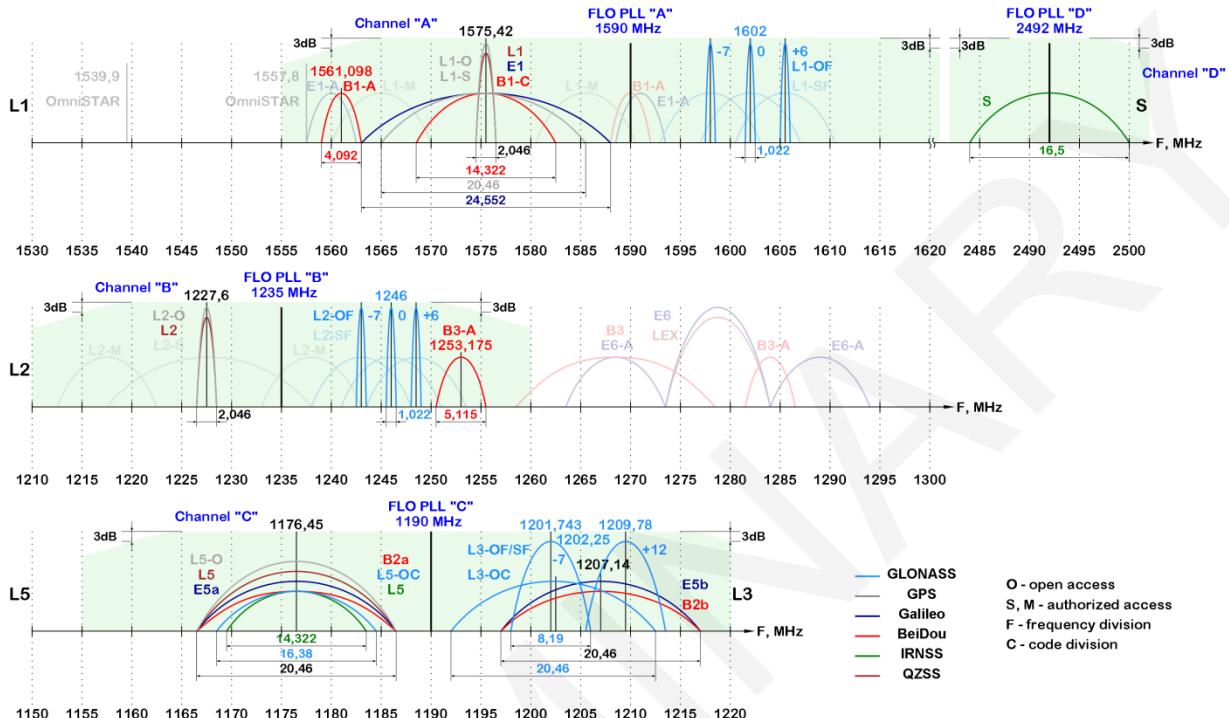
Two modes of temperature modes are available: single and continuous (**Reg9 D[1]**). In single mode the measurement is done once upon request to **Reg9 D[0]** by setting “1” and result will be stored in **Reg4 D[1-0] + Reg5 D[7-0]** after procedure is finished (auto reset to “0” in **Reg9 D[0]** indicates this) until next execution. One temperature measurement procedure time is up to 17 ms. To enter in continuous mode set **Reg9 D[1]** to “1” first then execute with **Reg9 D[0]**. In this case embedded temperature sensor periodically runs the measurement procedure and only the latest

result is stored in **Reg4 D[1-0] + Reg5 D[7-0]**. In order to stop continuous execution **Reg9 D[1]** should be set to “0”.

PRELIMINARY

## 6.13. OPERATION EXAMPLES

### 6.13.1. CONFIGURATION SET #1



#### General settings:

Reference frequency 10 MHz

#### CLK settings:

CLK frequency source PLL "A"  
CLK frequency 72.27 MHz

CLK type LVDS  
CLK amplitude Preset 3

#### PLL settings:

F<sub>LO</sub> PLL "A" 1590 MHz  
F<sub>LO</sub> PLL "B" 1235 MHz  
F<sub>LO</sub> PLL "C" 1190 MHz  
F<sub>LO</sub> PLL "D" 2492 MHz

#### Channel settings:

Channel "A" GNSS GPS L1, QZSS L1, Galileo E1, BeiDou B1, GLONASS L1  
Channel "B" GNSS GPS L2, QZSS L2, GLONASS L2, BeiDou B3-A

Channel "C" GNSS GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, IRNSS L5

Channel "D" GNSS IRNSS S

Channel "A" IF passband 30 MHz  
Channel "B" IF passband 20 MHz  
Channel "C" IF passband 30 MHz  
Channel "D" IF passband 11 MHz

#### GC mode:

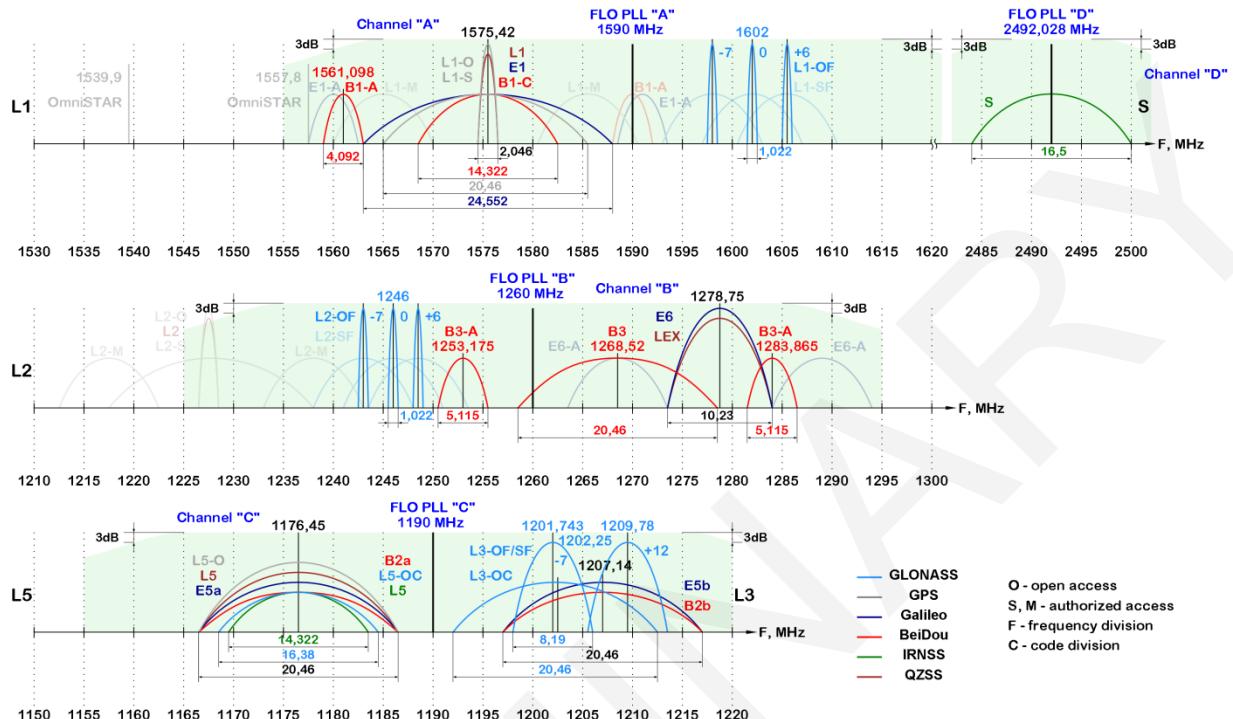
Channel "A"	IF auto
Channel "B"	IF auto
Channel "C"	IF auto
Channel "D"	RF manual + IF auto

#### Output data interface:

Channel "A"	2-bit ADC
Channel "B"	2-bit ADC
Channel "C"	2-bit ADC
Channel "D"	2-bit ADC

ADC output logic-level high ext. (VCC)  
ADC type Clocked by rising edge

### 6.13.2. CONFIGURATION SET #2



#### General settings:

Reference frequency 10 MHz

#### CLK settings:

CLK frequency source PLL "A"

CLK frequency 72.27 MHz

CLK type LVDS

CLK amplitude Preset 3

#### PLL settings:

F<sub>LO</sub> PLL "A" 1590 MHz

F<sub>LO</sub> PLL "B" 1260 MHz

F<sub>LO</sub> PLL "C" 1190 MHz

F<sub>LO</sub> PLL "D" 2492 MHz

#### Channel settings:

Channel "A" GNSS GPS L1, QZSS L1, Galileo E1, BeiDou B1, GLONASS L1

Channel "B" GNSS GLONASS L2, BeiDou B3, Galileo E6, QZSS LEX

Channel "C" GNSS GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, IRNSS L5

Channel "D" GNSS IRNSS S

Channel "A" IF passband 30 MHz

Channel "B" IF passband 30 MHz

Channel "C" IF passband 30 MHz

Channel "D" IF passband 11 MHz

#### GC mode:

Channel "A" IF auto

Channel "B" IF auto

Channel "C" IF auto

Channel "D" RF manual + IF auto

#### Output data interface:

Channel "A" 2-bit ADC

Channel "B" 2-bit ADC

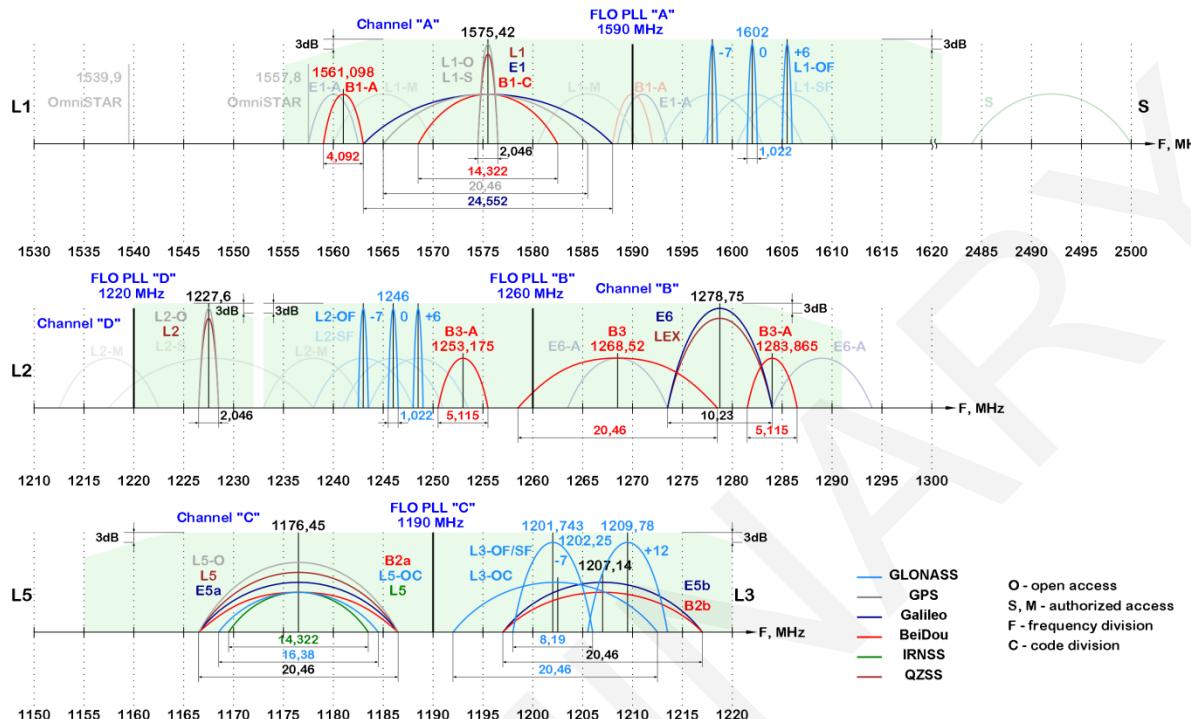
Channel "C" 2-bit ADC

Channel "D" 2-bit ADC

ADC output logic-level high ext. (VCC)

ADC clock type Clocked by rising edge

### 6.13.3. CONFIGURATION SET #3



#### General settings:

Reference frequency 10 MHz

#### CLK settings:

CLK frequency source PLL "A"

CLK frequency 72.27 MHz

CLK type LVDS

CLK amplitude Preset 3

#### PLL settings:

F<sub>LO</sub> PLL "A" 1590 MHz

F<sub>LO</sub> PLL "B" 1260 MHz

F<sub>LO</sub> PLL "C" 1190 MHz

F<sub>LO</sub> PLL "D" 1220 MHz

#### Channel settings:

Channel "A" GNSS GPS L1, QZSS L1, Galileo E1, BeiDou B1, GLONASS L1

Channel "B" GNSS GLONASS L2, BeiDou B3, Galileo E6, QZSS LEX

Channel "C" GNSS GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, IRNSS L5

Channel "D" GNSS GPS L2, QZSS L2

Channel "A" IF passband 30 MHz

Channel "B" IF passband 26 MHz

Channel "C" IF passband 30 MHz

Channel "D" IF passband 11 MHz

#### GC mode:

Channel "A" IF auto

Channel "B" IF auto

Channel "C" IF auto

Channel "D" RF manual + IF auto

#### Output data interface:

Channel "A" 2-bit ADC

Channel "B" 2-bit ADC

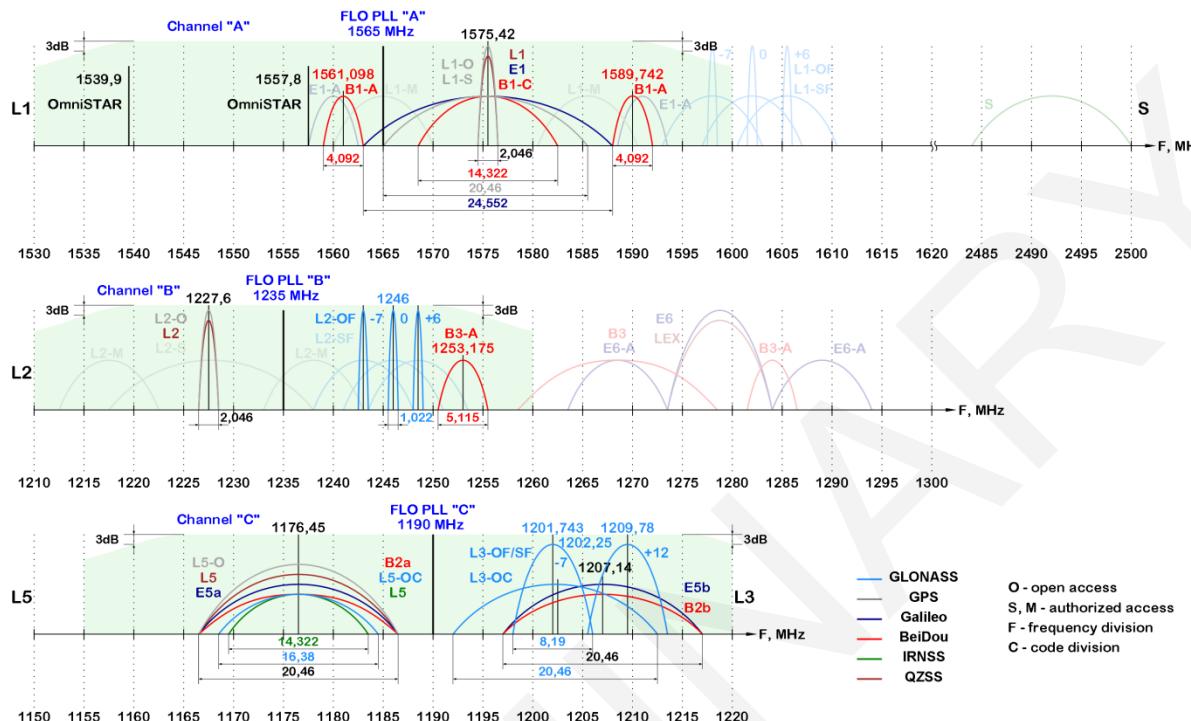
Channel "C" 2-bit ADC

Channel "D" 2-bit ADC

ADC output logic-level high ext. (VCC)

ADC clock type Clocked by rising edge

#### 6.13.4. CONFIGURATION SET #4



##### General settings:

Reference frequency 10 MHz

##### CLK settings:

CLK frequency source PLL "A"  
 CLK frequency 69.77 MHz  
 CLK type LVDS

CLK amplitude Preset 3

##### PLL settings:

F<sub>LO</sub> PLL "A" 1565 MHz  
 F<sub>LO</sub> PLL "B" 1235 MHz  
 F<sub>LO</sub> PLL "C" 1190 MHz  
 F<sub>LO</sub> PLL "D" Unused

##### Channel settings:

Channel "A" GNSS	OmniSTAR 1539.9, OmniSTAR 1557.8, BeiDou B1, GPS L1, Galileo E1, QZSS L1
Channel "B" GNSS	GPS L2, QZSS L2, GLONASS L2, BeiDou B3-A
Channel "C" GNSS	GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, IRNSS L5
Channel "D" GNSS	Unused
Channel "A" IF passband	30 MHz
Channel "B" IF passband	20 MHz
Channel "C" IF passband	30 MHz
Channel "D" IF passband	Unused

##### GC mode:

Channel "A"	IF auto
Channel "B"	IF auto
Channel "C"	IF auto
Channel "D"	RF manual + IF auto

##### Output data interface:

Channel "A"	2-bit ADC
Channel "B"	2-bit ADC
Channel "C"	2-bit ADC
Channel "D"	2-bit ADC
ADC output logic-level high	ext. (VCC)
ADC clock type	Clocked by rising edge

## 6.14. PCB LAYOUT RECOMMENDATIONS

Will be added in new versions of datasheet.

PRELIMINARY

## 7. PACKAGE INFORMATION

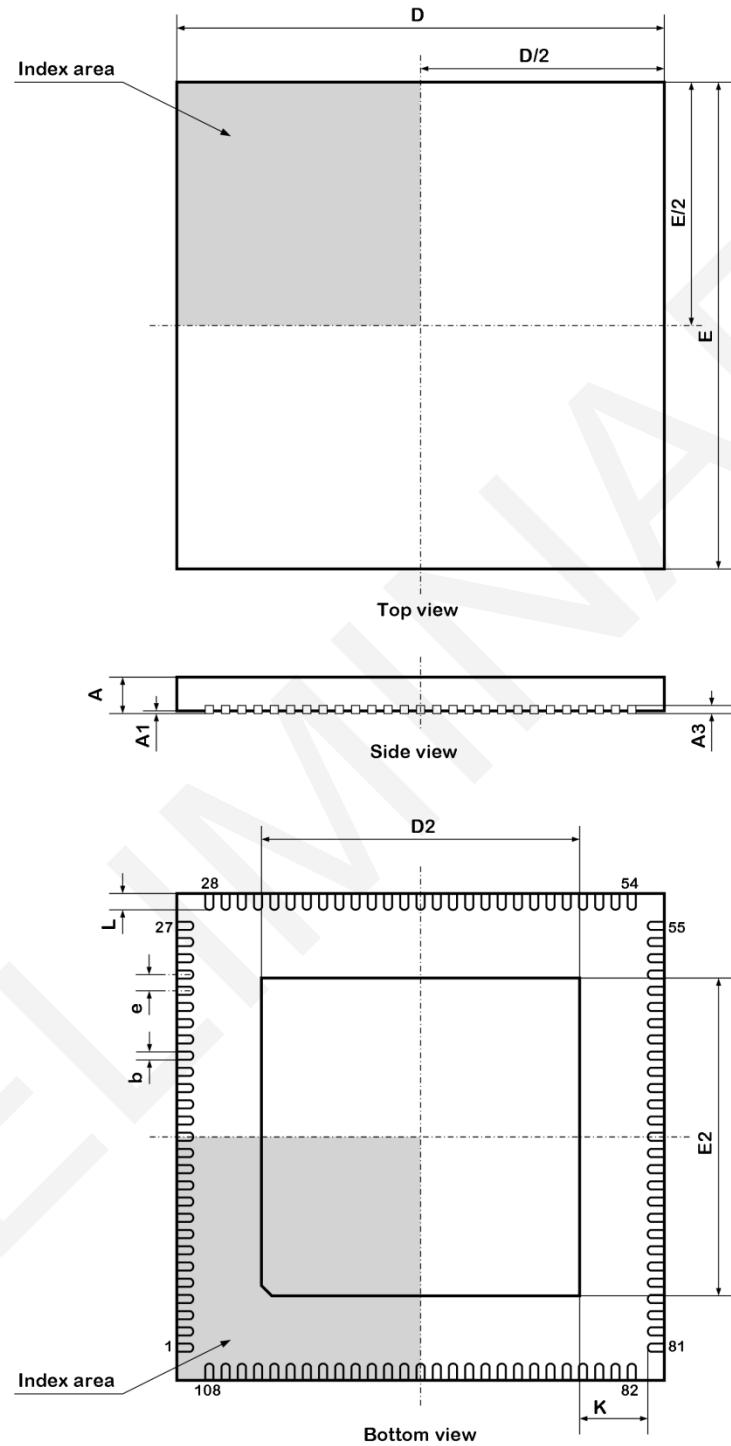


Figure 7.1: Package QFN108-12×12 \*

Table 7.1: Package QFN108-12×12 dimension\*

Unit	A	A1	A3	b	D	D2	E	E2	e	K	L
min, mm	0.80	0.00	0.203	0.15	12.00	7.75	12.00	7.75	0.40	0.20	0.35
typ., mm	0.85	0.02		0.20		7.80		7.80		-	0.40
max, mm	0.90	0.05		0.25		7.85		7.85		-	0.45

\* Package drawing and dimensions are for reference only. Actual values are compliant to JEDEC standard outlines MO-220.