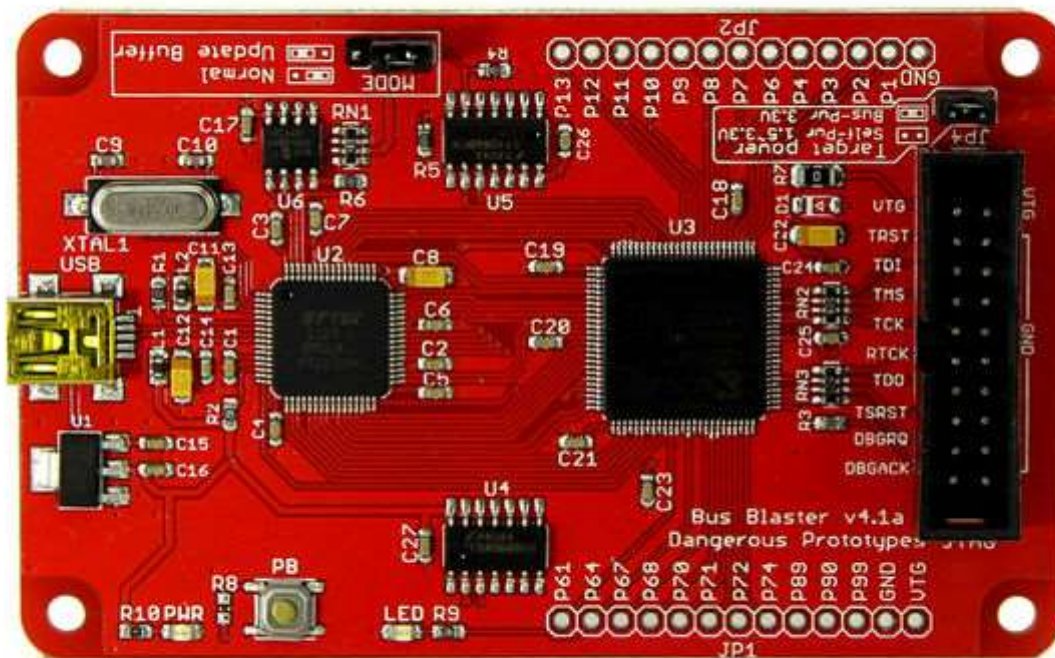DANGEROUSPROTOTYPES
A new open source hardware project every month

- Blog
- Projects
- Forum
- About
- Contact
- Shop
- Free PCBs

Facebook Twitter RSS Comments

Bus Blaster v4 design overview

From DP

You can get a Bus Blaster v4 for $45 (http://www.seeedstudio.com/depot/bus-blaster-v4-p-1416.htm) .

Bus Blaster v4 is an experimental, high-speed JTAG debugger for ARM processors, FPGAs, CPLDs, flash, and more. Thanks to a reprogrammable buffer, a simple USB update makes Bus Blaster v4 compatible with many different JTAG debugger types in the most popular open source software.

- Based on FT2232H with high-speed USB 2.0
- Buffered interface works with 3.3volt to 1.5volt targets
- Reprogrammable buffer is compatible with multiple debugger types
- Compatible with 'jtagkey', 'KT-link' programmer settings in OpenOCD (http://openocd.berlios.de/web/) , urJTAG (http://urjtag.sourceforge.net/) , and more
- Should support Serial Wire Debug when available
- Mini-CPLD development board: self programmable, extra CPLD pins to header
- Open source (CC-BY-SA)

Bus Blaster v4 (http://www.seeedstudio.com/depot/bus-blaster-v4-p-1416.html) is a redesign of v3/v2 that supports SWV, an obscure extension to a reduced pincount JTAG protocol most people will never use. Unless you need it, stick with v3 and save a few bucks!

- Can now support the SWV feature of Cortex microcontroller for advance debugging when software support is available
- SWV is little used and not currently supported in software, most users will be better off with Bus Blaster v4 available here (http://www.seeedstudio.com/depot/bus-blaster-v3-p-1415.html?cPath=63_69)
- Fitted in a DP9056 (90x56 mm) standard PCB
- Added series resistors to input and output pins to protect against damage and noise

Bus Blaster v4 is available now for $45 (http://www.seeedstudio.com/depot/bus-blaster-v4-p-1416.htm) . Each unit is tested with a real JTAG target before it ships.

Read about the design below.

Contents

Overview

The Bus Blaster is used to program and debug devices with a JTAG interface like ARM processors, CPLDs, flash

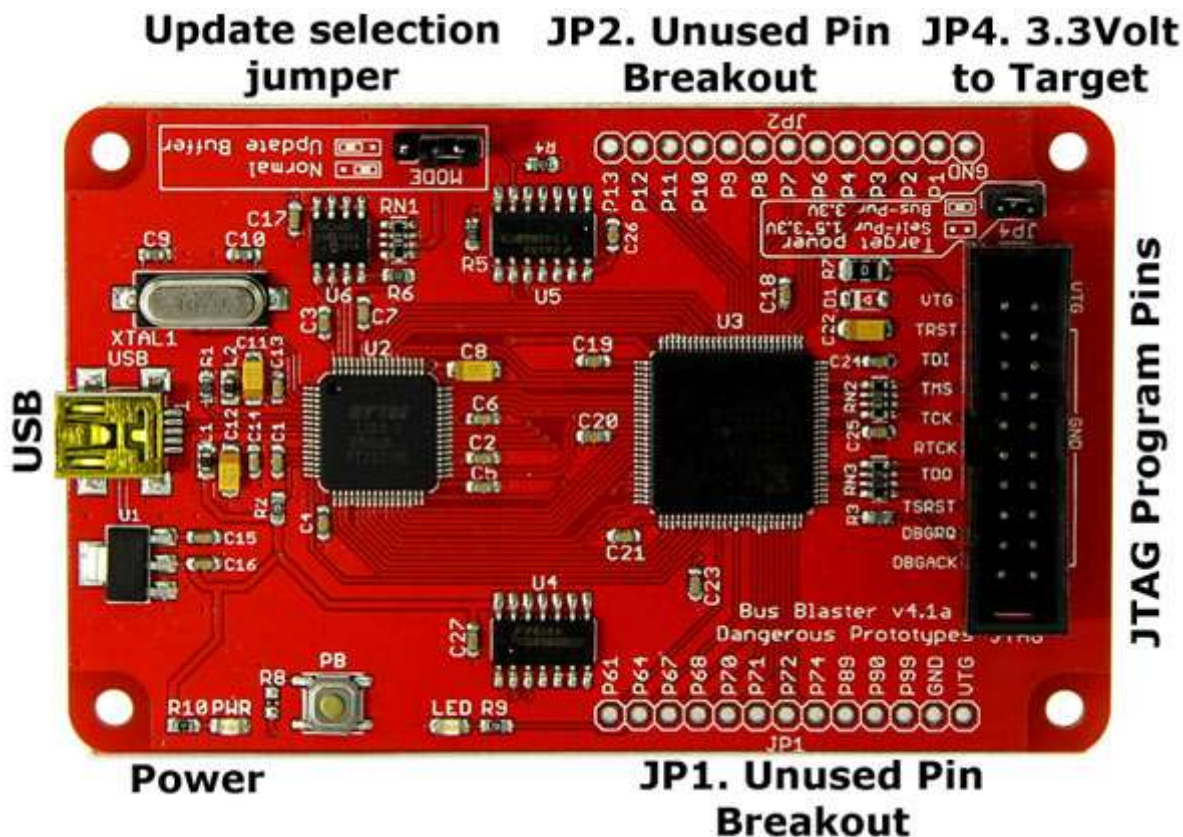| Project Summary	
Name:	Bus Blaster v4 design overview
Buy it:	Get one for $45 at Seeed Studio

memory, and more. A FT2232H USB chip gives us two high-speed JTAG interfaces. The 16 pins of the primary interface are connected to a CoolRunner-II CPLD. The CPLD is a programmable buffer that translates between the FT2232H at 3.3volts, and a 1.5volt to 3.3volt target.

Many JTAG debuggers use the FT2232 chips, but they have slightly different buffers. The CPLD can be programmed to imitate many of them, so it works out of the box with our favorite open source debugging apps. Updates are done over USB using the second JTAG interface on the FT2232H.
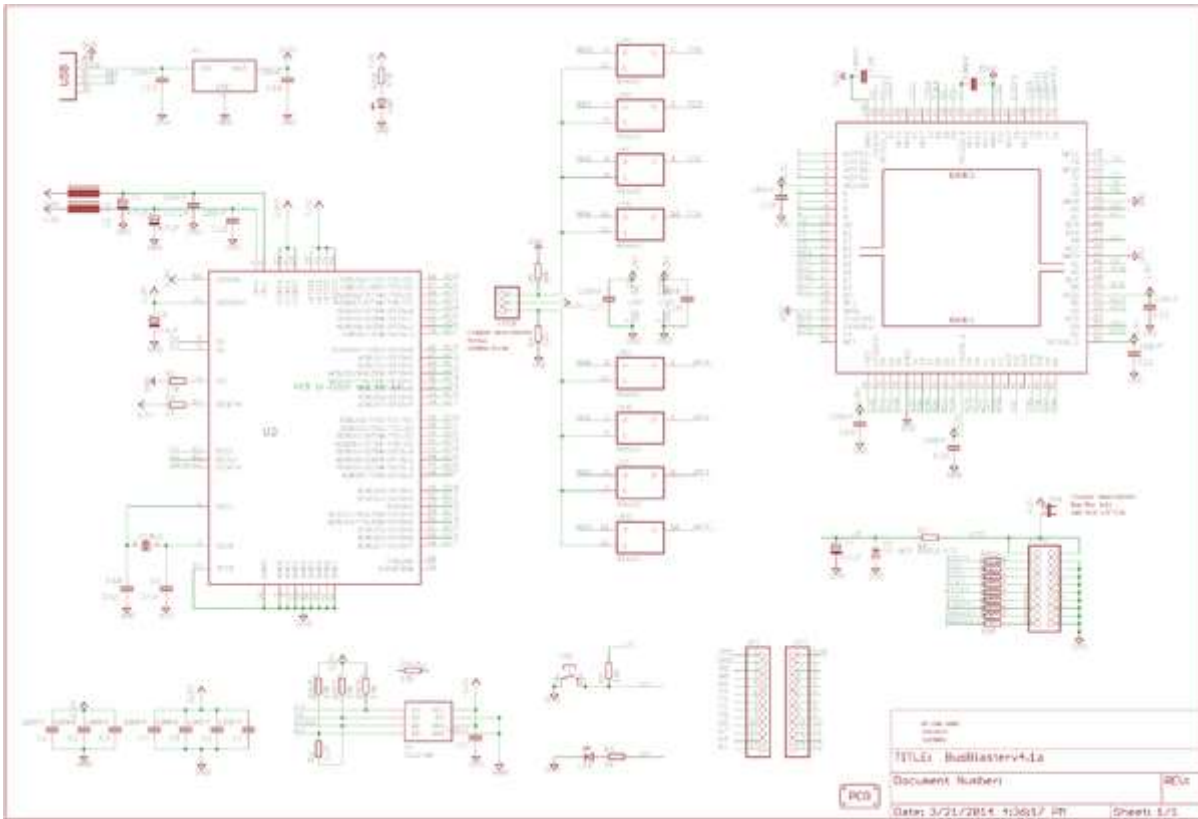
This project was inspired by a forum post (http://dangerousprototypes.com/forum/viewtopic.php?f=37&t=403&start=30#p4092) that linked to a Texas Instruments' XDS100 programmer (http://processors.wiki.ti.com/index.php/XDS100) . TI's design is essentially the same, but we moved the CPLD JTAG connection to the second JTAG interface for easier reprogramming. Bus Blaster v4 was developed in a public forum (http://dangerousprototypes.com/forum/index.php?board=37.0) , and progress was documented on a wiki.

Parts Layout Guide

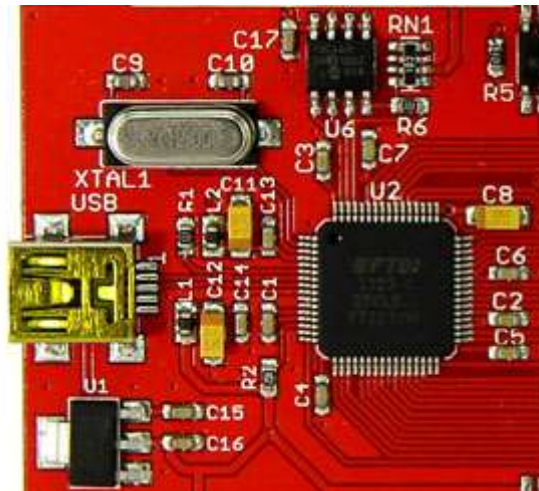# Hardware

Click for a full size schematic image. Schematic and PCB were designed with the freeware version of Cadsoft Eagle (http://www.cadsoft.de) , download the latest project files from our Google Code project page (http://code.google.com/p/dangerous-prototypes-open-hardware/source/browse/#svn%2Ftrunk%2FBusBlasterv2) .
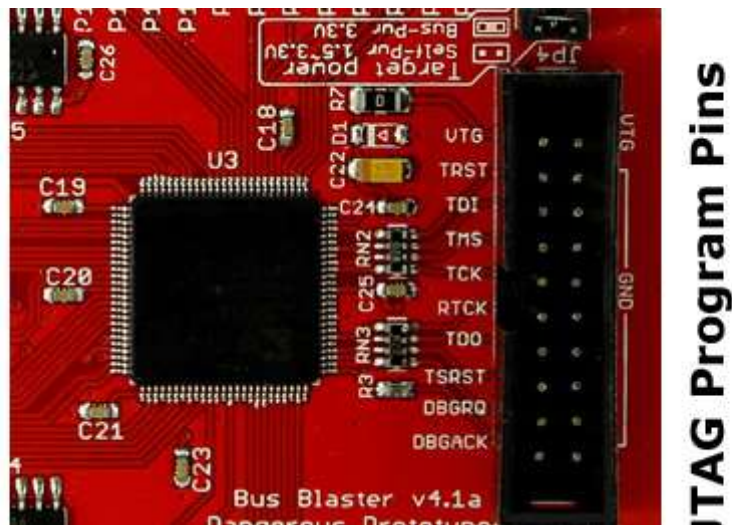
FT2232H

The FT2232H (http://www.ftdichip.com/Products/ICs/FT2232H.htm) (U2) is a powerful USB to serial communication chip. It has an MPSSE feature that provides a simple USB to JTAG converter (and UART, I2C, or SPI). Most DIY JTAG debuggers use this chip, as do many commercial models.

Bus Blaster v4 uses the 'H' version of the chip, the latest 3.3volt revision that supports JTAG adaptive clocking. The circuit is based on a reference design from the FT2232H datasheet.

- See the FT2232H breakout board documentation for a complete explanation of the FT2232H reference circuit

Buffered interface

The buffer translates voltage levels between the FT2232H (3.3volts) and a JTAG device (1.5volts-3.3volts). The four main JTAG IO pins (TDI, TDO, TCK, TMS) are fixed on the FT2232, but the other reset and control pins vary among programmers.

Bus Blaster v4 is buffered by a programmable logic chip (CPLD) that can be updated to imitate many common buffer types. The CPLD programming pins are connected to the secondary JTAG interface on the FT2232, so uploading a new buffer type is done entirely from software over USB.

Reprogramming logic

Bus Blaster v4 was designed primarily to support the SWV feature of advanced Cortex microcontroller debugging. Basically the microcontroller has an extra serial UART channel to send debug or other info back to the programmer. This is implemented by using the second JTAG engine of the FT2232 as a serial UART input and passing the info to the user through a serial terminal or whatever.

The Bus Blaster v2/v3 used the secondary JTAG block to program the CPLD with different buffer interfaces. These pins cannot be recycled for use with SWV in the v2/v3 hardware. In v4 we use two 4066 analog buffers (U4/U5) to switch the secondary JTAG interface between the programming pins of the CPLD and other multipurpose pins.

When the MODE jumper is set to program, the secondary JTAG interface of the FT2232 connects to the JTAG programming interface of the CPLD. When MODE is set to normal, the secondary JTAG interface of the FT2232 is connected to multipurpose pins on the CPLD. This way we can both program the CPLD and use the secondary interface for SWV channel information. The disadvantage is that you now have to swap a jumper to change between modes, though most users will not do this very often.

CPLD
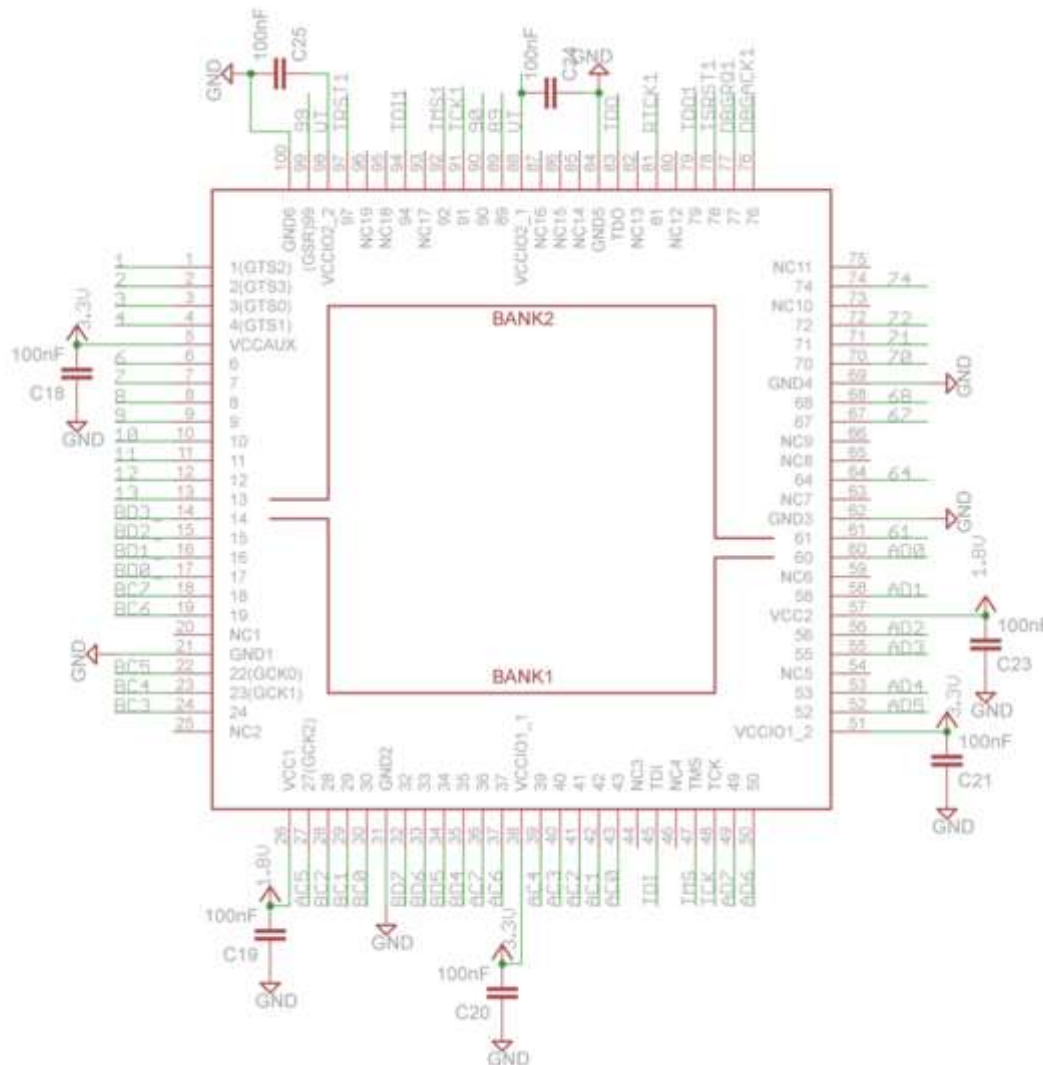
An XC2C64A CoolRunner-II CPLD (U3) is used for the buffer. This is the bigger, 100 pin version of the XC2C32A used in Bus Blaster v2/v3. More CPLD pins are needed to support the SWV protocol.

The CPLD core requires a 1.8volt supply, which is conveniently available from the FT2232. The JTAG and IO pins are powered by a separate supply between 1.5 and 3.3volts. Each supply pin gets a 0.1uF capacitor.

This chip is perfect for voltage translation because the IO pins are divided into two groups that can operate from different power supplies. We connected one group to the FT2232 and the 3.3volt FT2232 power supply. The other group connects to the JTAG target, and operate from a 1.5volt to 3.3volt target supply.

```
You must connect the target power supply to the buffer
The buffer is powered by the target, 1.5volts to 3.3volts only
Put a header on "Target power"/JP4 to power the target from the programmer. 3.3volts max 200mA
The buffer is NOT 5volt compatible.
```

The IO pins on Bus Blaster v4 are buffered with 82ohm series resistors to reduce noise and prevent damage to the programmer.

We brought the extra CPLD pins to a header. The Bus Blaster v4 can also be used as a simple CoolRunner-II CPLD development board.

- See Xilinx CoolRunner-II CPLD quick start guide for more

Buffer logic

New buffer logic is designed using simple schematic entry, Verilog, or VHDL, and the free ISE Webpack software from Xilinx.
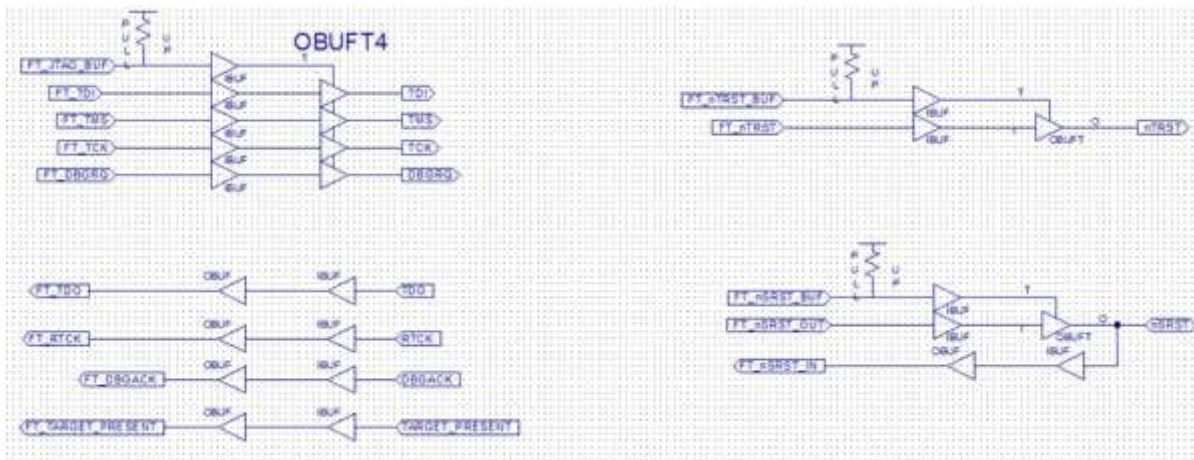
- See CPLD development tutorials

Here are two examples of buffer logic to give you an idea how flexible the design can be.

- See Bus Blaster buffer logic for the latest buffers and programming instructions

Buffer logic for Bus Blaster v4 and Bus Blaster v2/v3 ARE NOT COMPATIBLE!

JTAGkey compatible

The JTAGkey (http://www.amontec.com/jtagkey.shtml) is probably the most commonly used buffer configuration among DIY FT2232-based JTAG programmers. It is compatible with OpenOCD, urJTAG, and more.

Program the Bus Blaster with this buffer and it will work with most applications that support JTAGkey type debuggers.

KT-link compatible
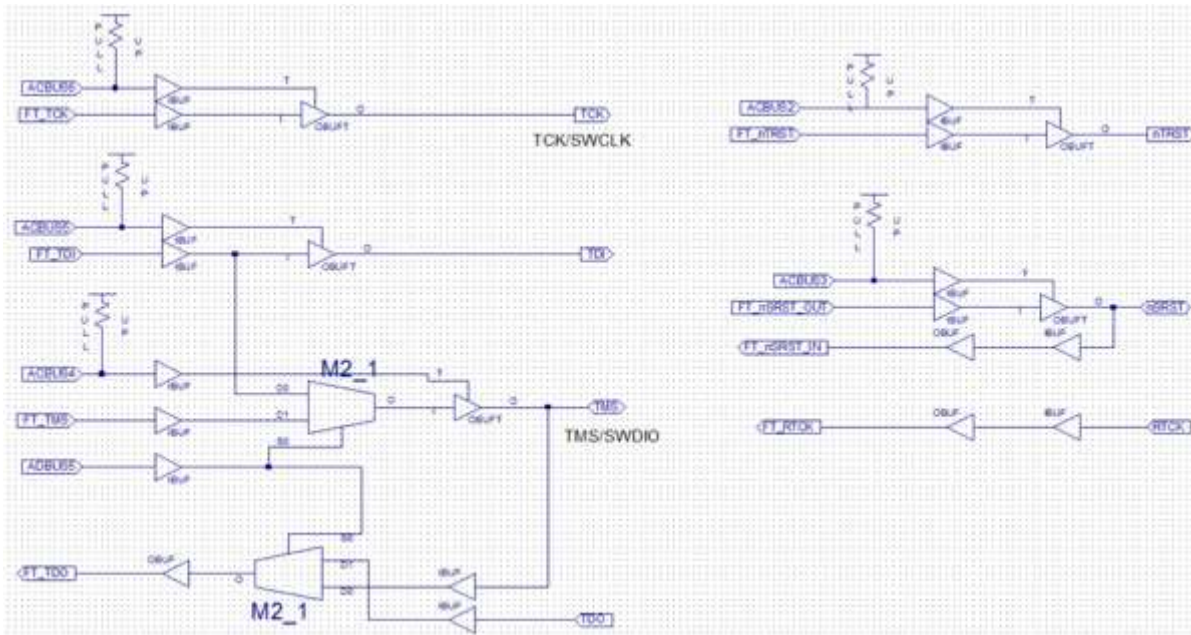
OpenOCD and urJTAG will soon support new Serial Wire Debug and Serial Wire Viewer JTAG protocols via a KT-link (http://www.shop.kristech.eu/product_info.php?products_id=257&language=EN) type buffer.

Program the Bus Blaster with this buffer and it can support SWD in OpenOCD and urJTAG. Special thanks to the developers of libswd (http://sourceforge.net/apps/trac/libswd) for help implementing this buffer on the Bus Blaster.

Pinout
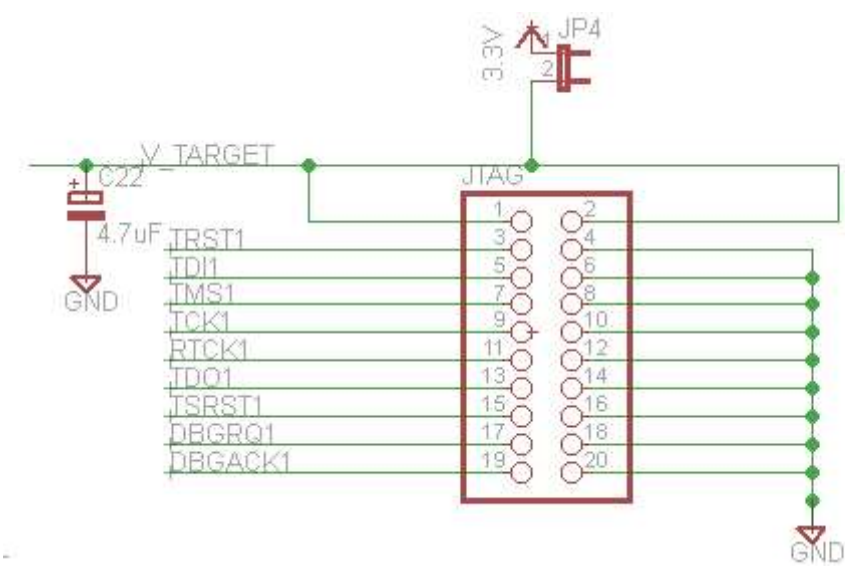
JTAG header pinout

Pin	Fixed FT2232 pin	Description	Direction
VTG		Voltage target	input
TRST		Reset output	output
TDI	ADBUS1	JTAG data in to target	output
TMS	ADBUS3	JTAG state machine update	output
TCK	ADBUS0	JTAG clock in to target	output
RTCK	ADBUS7	System return clock	input

TDO	ADBUS2	JTAG data out from target	input
TSRST		Bi-directional reset pin	inout
DBGRQ		Debug request	output
DBGACK		Debug acknowledge	input

9 CPLD pins are brought to the 20pin JTAG header. The pins are labeled, but the CPLD buffer makes placement totally arbitrary.

Not all pins are supported by all buffers and/or applications

The VTG pin should be connected to the power supply of the device under test. The JTAG pin outputs will then work at the same voltage.

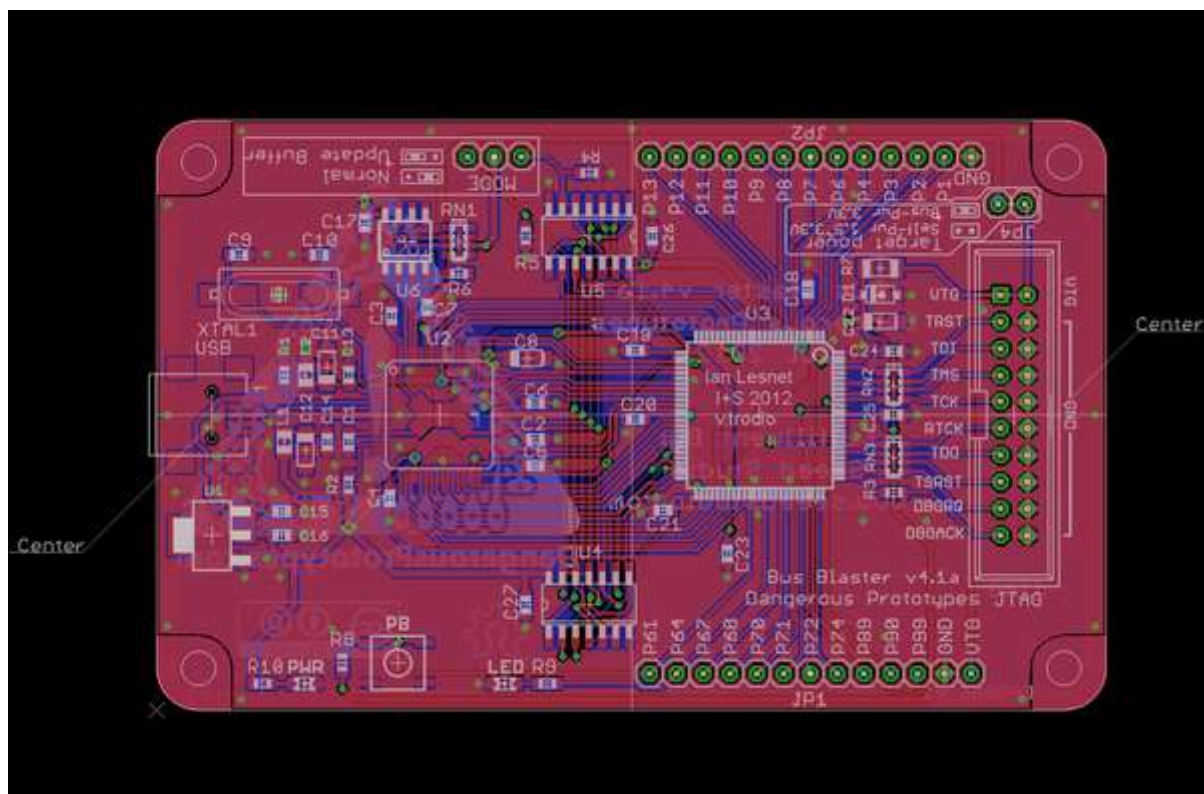The target must generally supply power to the VTG pin!

The JTAG pins can also operate from the 3.3volt on-board power supply by placing a jumper on header JP4. In this configuration the VTG pin can supply up to 100mA @ 3.3volts to the test device.

PCB
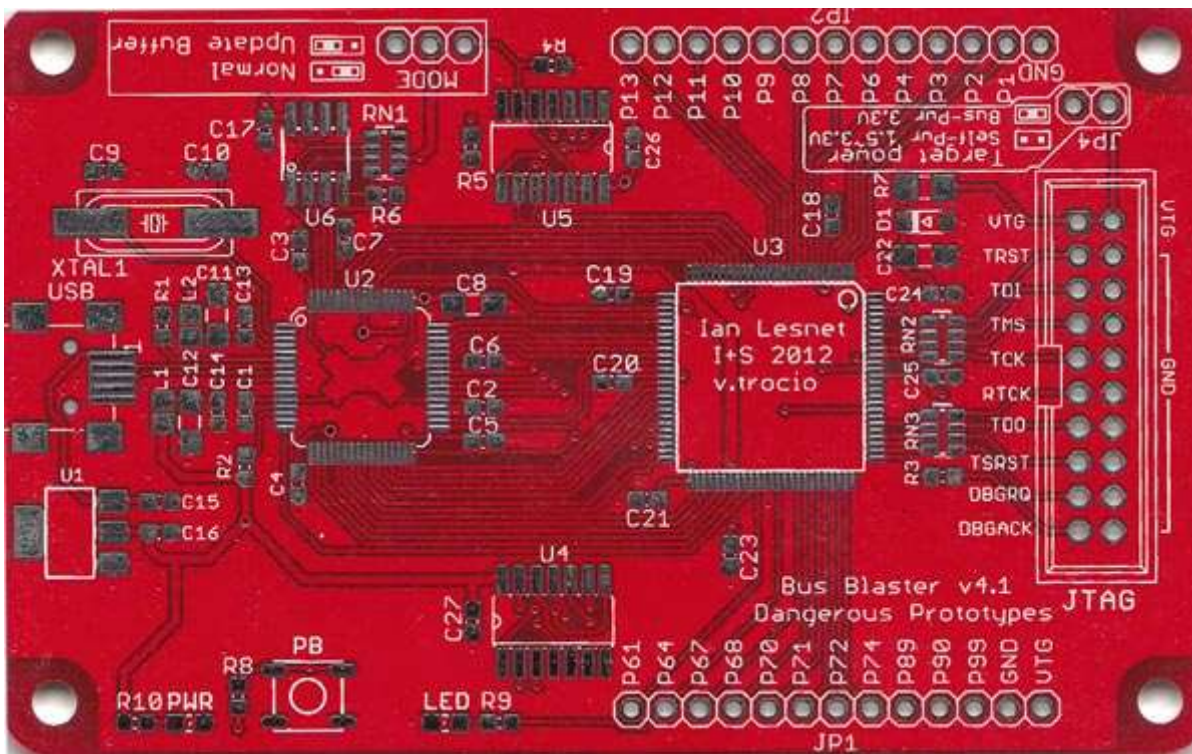
We used the freeware version of Cadsoft Eagle (http://www.cadsoft.de/) to make the schematic and PCB. Download the latest designs and firmware from the project Google Code page (http://code.google.com/p/dangerous-prototypes-open-hardware/source/browse/#svn%2Ftrunk%2FBusBlasterv2) .

Partslist

Click for a full size placement image.

Bus Blaster v4.1a

Part	Quantity	Value	Package
C1-C7,C13-C21,C23-C27	21	100nF	C603
C8	1	3.3uF	SMC_A
C9,C10	2	27pF	C603
C11,C12,C22	3	4.7uF	SMC_A
D1	1	DO NOT POPULATE	SOD-123
JP1,JP2	2	0.1" header	1X13
JP4	1	0.1" header	1X02
JTAG	1	Shrouded header	PINSHRD_PTH_2X10
L1,L2	2	Ferrite bead	FB603
LED	1	LED	LED-805
MODE	1	0.1" header	1X03
PB	1	Push button	TACT_SWITCH_SMALL
PWR	1	LED	CHIPLED_0805
R1	1	12K	R603
R2,R9	2	1K	R603
R3	1	82R	R603
R4,R5,R8	3	10K	R603
R6	1	2.2K	R603
R7	1	0R	R1206
R10	1	470	R603

RN1	1	10k	RN8P-4R-CRA06S
RN2,RN3	2	82R	RN8P-4R-CRA06S
U1	1	LD1117-3.3	SOT223
U2	1	FT2232H	LQFP64@1
U3	1	XC2C64A	VQ100
U4,U5	2	4066D	SO14
U6	1	93LC46B EEPROM	SOIC8
USB	1	USB Mini B	CONN_USB_MINI-B
XTAL1	1	12MHz crystal	HC-49U

The latest sources and distributors are in the master partlist (http://dangerousprototypes.com/docs/Partlist) . See something missing? Please let us know (http://dangerousprototypes.com/forum) .

Taking it further

The reprogrammable buffer logic should future proof Bus Blaster v4. Already we were able to add Serial Wire Debug support by creating a new buffer implementation.

Bus Blaster v4 uses a 100pin CPLD to include support for SWV, another reduced pin-count JTAG protocol. Most people will never need this. Stick with v3 unless you absolutely need the SWV feature.

Get one!

Bus Blaster v4 is available now for $45 (http://www.seeedstudio.com/depot/bus-blaster-v4-p-1416.html) . Each unit is tested with a real JTAG target before it ships.

Your purchases at Seeed Studio keep the open source projects coming, we sincerely appreciate your support!

Links

- Bus Blaster manual
- Bus Blaster discussion forum (http://dangerousprototypes.com/forum/viewforum.php?f=37)
- FT2232H (http://www.ftdichip.com/Products/ICs/FT2232H.htm)
- FTDI2232 datasheet (http://www.ftdichip.com/)
- XC2C64A (http://www.xilinx.com/support/documentation/data_sheets/ds311.pdf) CPLD datasheet

License

Retrieved from "http://dangerousprototypes.com/docs/Bus_Blaster_v4_design_overview"
Categories: Projects | Bus Blaster

jump to

- Projects homepage

- Bus Pirate
- USB Infrared toy
- Web platform
- Bus Blaster
- Logic Sniffer
- CPLD dev boards
- Logic Shrimp
- Breakout boards
- Proto boards
- #twatch network LCD
- Flash Destroyer
- In development
- Partlist and reference
- Recent changes

buy stuff

- Bus Pirate v3
- USB Infrared Toy
- Bus Blaster v2
- Logic Sniffer

Search

[   ] [Go] [Search]

Toolbox

- What links here
- Related changes
- Special pages
- Printable version
- Permanent link

Views

- Page
- Discussion
- View source
- History

Personal tools

- Log in

Site

- This page was last modified on 21 March 2014, at 11:50.

Copyright 2022 Where Labs, LLC.

Connect

- Follow us on Twitter
- Subscribe to our feed
- Subscribe to our comments
- Visit our Facebook page
- Send us an email

Projects

- Get a Bus Pirate v3
- Get a Bus Blaster v2
- Get a USB Infrared Toy
- Get a Logic Sniffer

About Us

Our goal is to make open source hardware that makes hacking fun. Copies of our projects are available through Seeed Studio and our distributors.