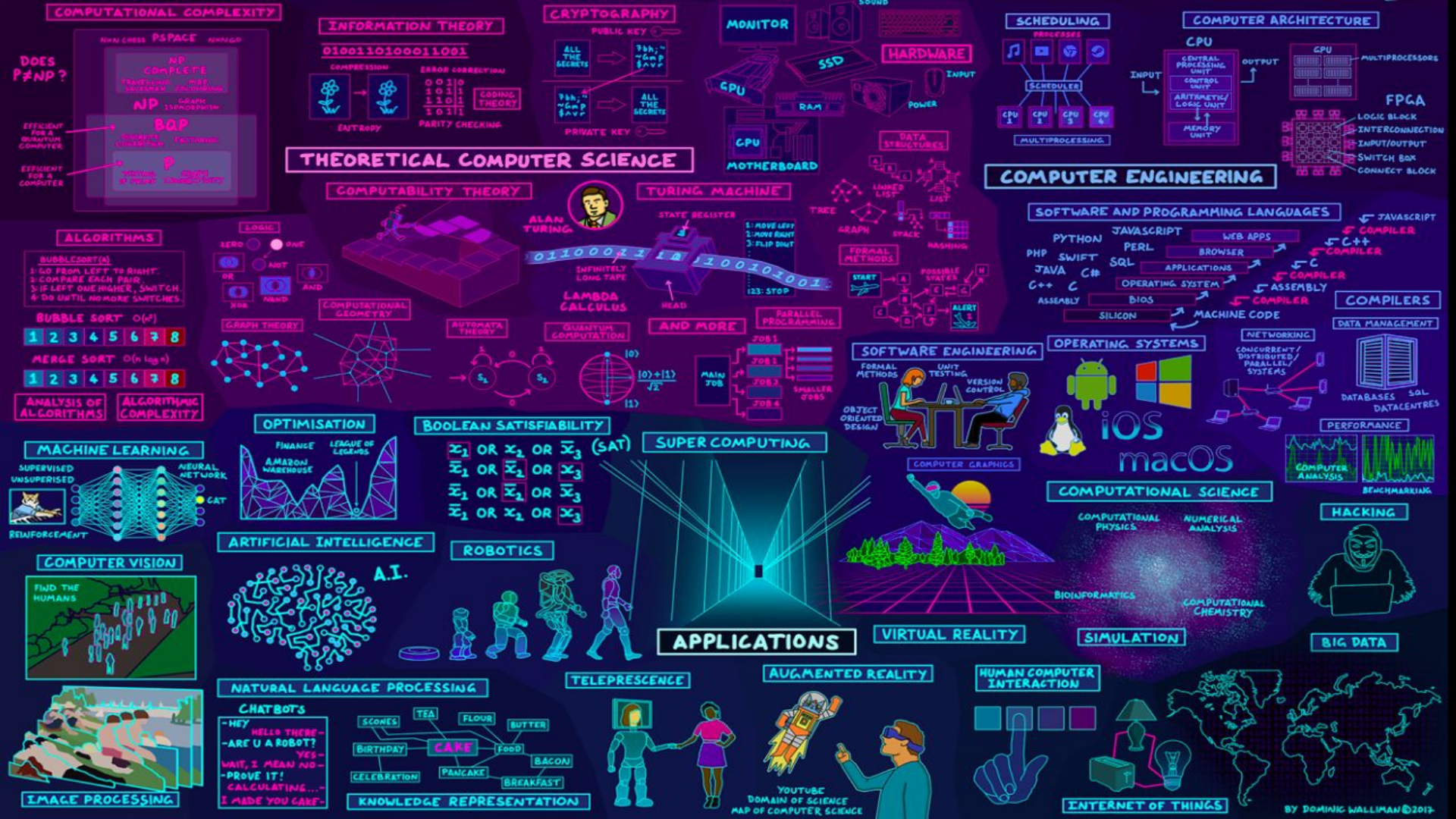
FPGAs for Beginners


COMPUTATIONAL COMPLEXITY
DOES P≠NP?
NP-COMPLETE
NP
BQP
P
EFFICIENT FOR A QUANTUM COMPUTER
EFFICIENT FOR A COMPUTER
INFORMATION THEORY
0100110100011001
COMPRESSION
ENTROPY
ERROR CORRECTION
PARITY CHECKING
CODING THEORY
CRYPTOGRAPHY
PUBLIC KEY
PRIVATE KEY
ALL THE SECRETS
THEORETICAL COMPUTER SCIENCE
COMPUTABILITY THEORY
TURING MACHINE
ALAN TURING
STATE REGISTER
INFINITELY LONG TAPE
HEAD
LAMBDA CALCULUS
ALGORITHMS
BUBBLESORT(A)
BUBBLE SORT O(n²)
MERGE SORT O(n log n)
ANALYSIS OF ALGORITHMS
ALGORITHMIC COMPLEXITY
LOGIC
GRAPH THEORY
COMPUTATIONAL GEOMETRY
AUTOMATA THEORY
QUANTUM COMPUTATION
AND MORE
PARALLEL PROGRAMMING
FORMAL METHODS
DATA STRUCTURES
MONITOR
SOUND
HARDWARE
SSD
RAM
GPU
MOTHERBOARD
POWER
INPUT
SCHEDULING
PROCESSES
SCHEDULER
MULTIPROCESSING
COMPUTER ARCHITECTURE
CPU
CENTRAL PROCESSING UNIT
CONTROL UNIT
ARITHMETIC/LOGIC UNIT
MEMORY UNIT
OUTPUT
MULTIPROCESSORS
FPGA
LOGIC BLOCK
INTERCONNECTION
INPUT/OUTPUT
SWITCH BOX
CONNECT BLOCK
COMPUTER ENGINEERING
SOFTWARE AND PROGRAMMING LANGUAGES
PYTHON
JAVASCRIPT
PHP
SWIFT
PERL
SQL
JAVA
C#
C++
C
ASSEMBLY
WEB APPS
BROWSER
APPLICATIONS
OPERATING SYSTEM
BIOS
SILICON
MACHINE CODE
COMPILER
COMPILERS
SOFTWARE ENGINEERING
FORMAL METHODS
UNIT TESTING
VERSION CONTROL
OBJECT ORIENTED DESIGN
OPERATING SYSTEMS
iOS
macOS
NETWORKING
CONCURRENT/DISTRIBUTED/PARALLEL SYSTEMS
DATA MANAGEMENT
DATABASES
SQL
DATACENTRES
PERFORMANCE
COMPUTER ANALYSIS
BENCHMARKING
MACHINE LEARNING
SUPERVISED
UNSUPERISED
REINFORCEMENT
NEURAL NETWORK
CAT
OPTIMISATION
FINANCE
LEAGUE OF LEGENDS
AMAZON WAREHOUSE
BOOLEAN SATISFIABILITY
(SAT)
SUPER COMPUTING
COMPUTER GRAPHICS
COMPUTATIONAL SCIENCE
COMPUTATIONAL PHYSICS
NUMERICAL ANALYSIS
BIOINFORMATICS
COMPUTATIONAL CHEMISTRY
HACKING
ARTIFICIAL INTELLIGENCE
A.I.
ROBOTICS
COMPUTER VISION
FIND THE HUMANS
IMAGE PROCESSING
APPLICATIONS
VIRTUAL REALITY
SIMULATION
BIG DATA
NATURAL LANGUAGE PROCESSING
CHATBOTS
-HEY
-ARE U A ROBOT?
-PROVE IT!
CALCULATING...
I MADE YOU CAKE
SCONES
TEA
FLOUR
BUTTER
BIRTHDAY
CAKE
FOOD
BACON
CELEBRATION
PANCAKE
BREAKFAST
KNOWLEDGE REPRESENTATION
TELEPRESCENCE
AUGMENTED REALITY
YOUTUBE
DOMAIN OF SCIENCE
MAP OF COMPUTER SCIENCE
HUMAN COMPUTER INTERACTION
INTERNET OF THINGS
BY DOMINIC WALLIMAN ©2017

in HaPra:

- VHDL compiler GHDL
- Wave viewer GTKWave

in Fachprojekt:

- real chip(FPGA)
- Vivado Design Suite
  - Resource Consumption
  - Timing Analysis

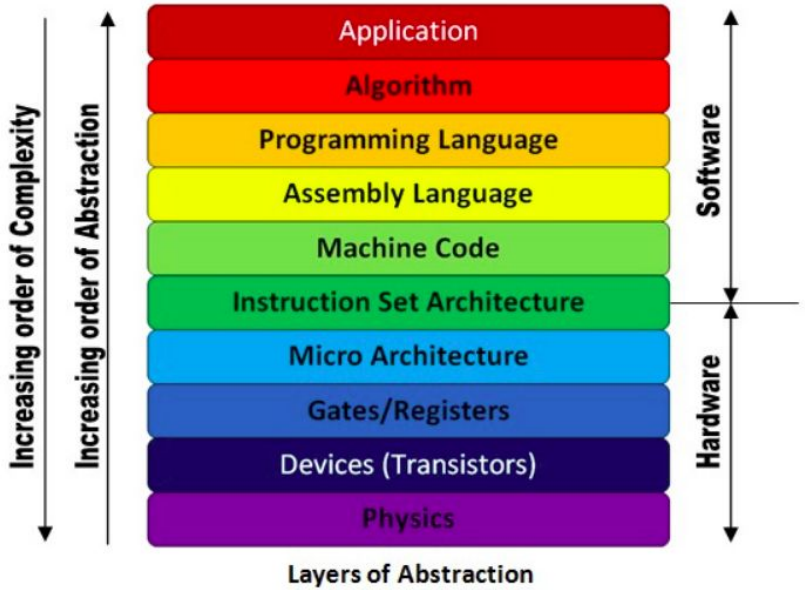


Image: https://electronics.stackexchange.com

FPGAs : What are they and Why should you care?

Michael Krekker
20. Oktober 2021

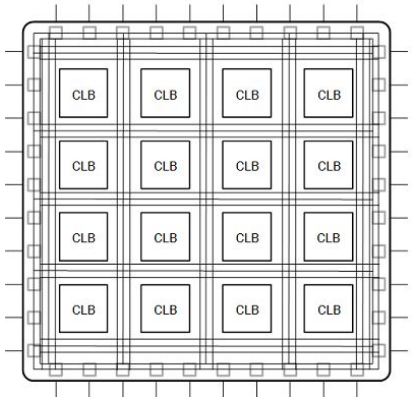
Introduction

- What is FPGA?
- Where FPGA is used?
- FPGA vendors
- FPGA Architecture
- Materials for self study

What is FPGA?

Field Programmable Gate Array

- Field Programmable:
  - Schema is programmed and specified by user

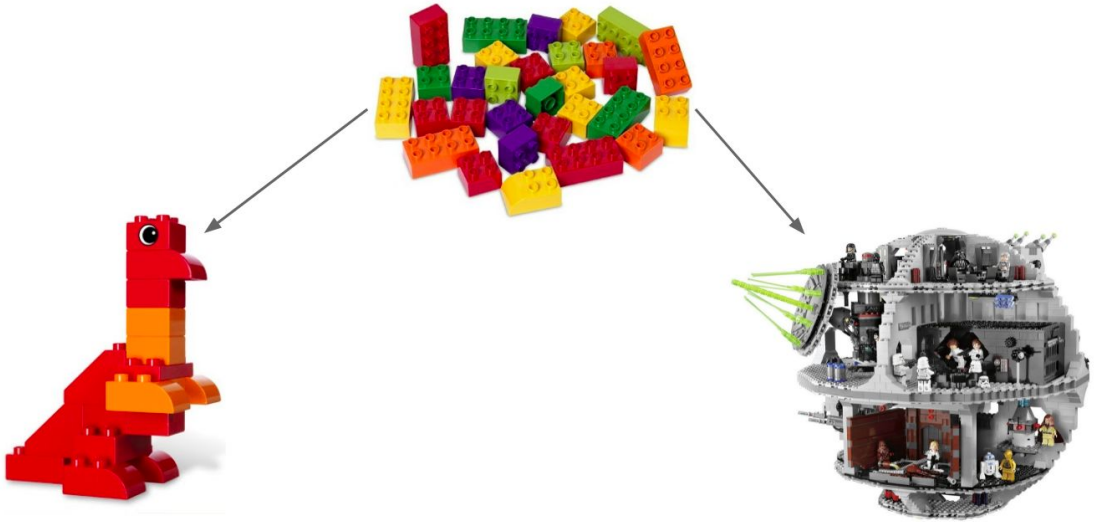


- Gate Array:
  - some gate array, which can be reprogrammed

Michael Krekker
20. Oktober 2021

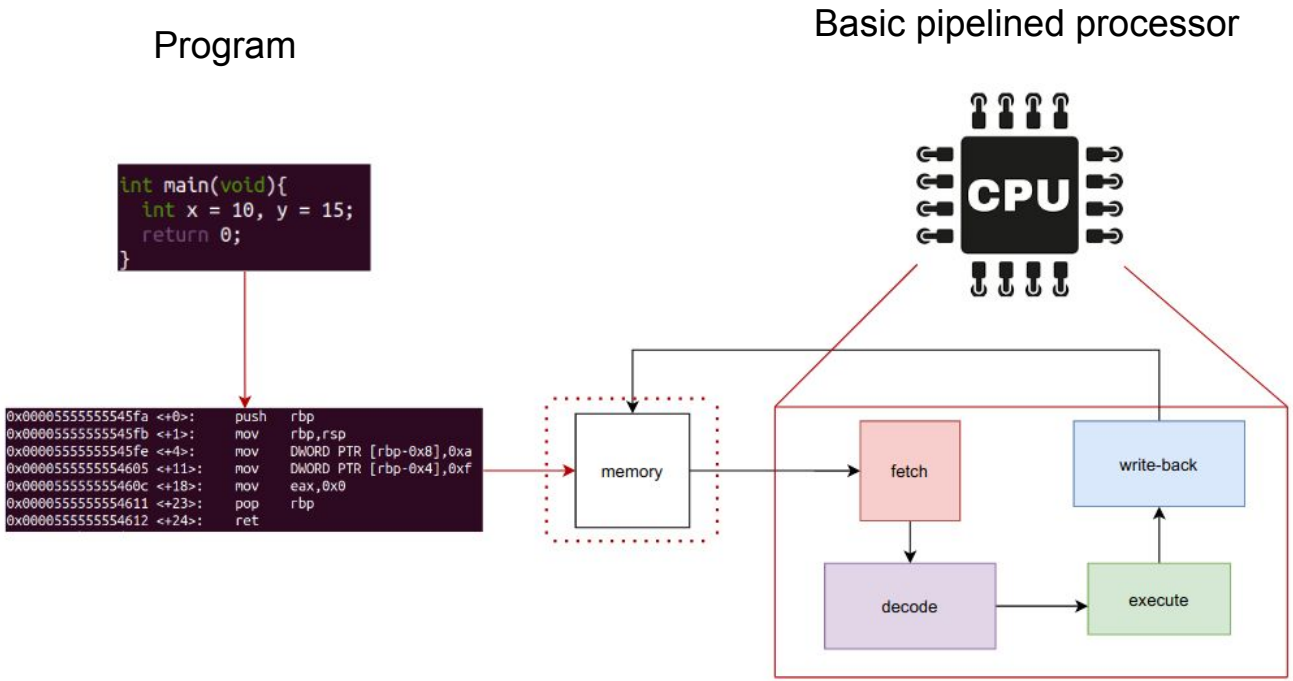
Image: Xilinx. Understanding FPGA Architecture

What is FPGA?

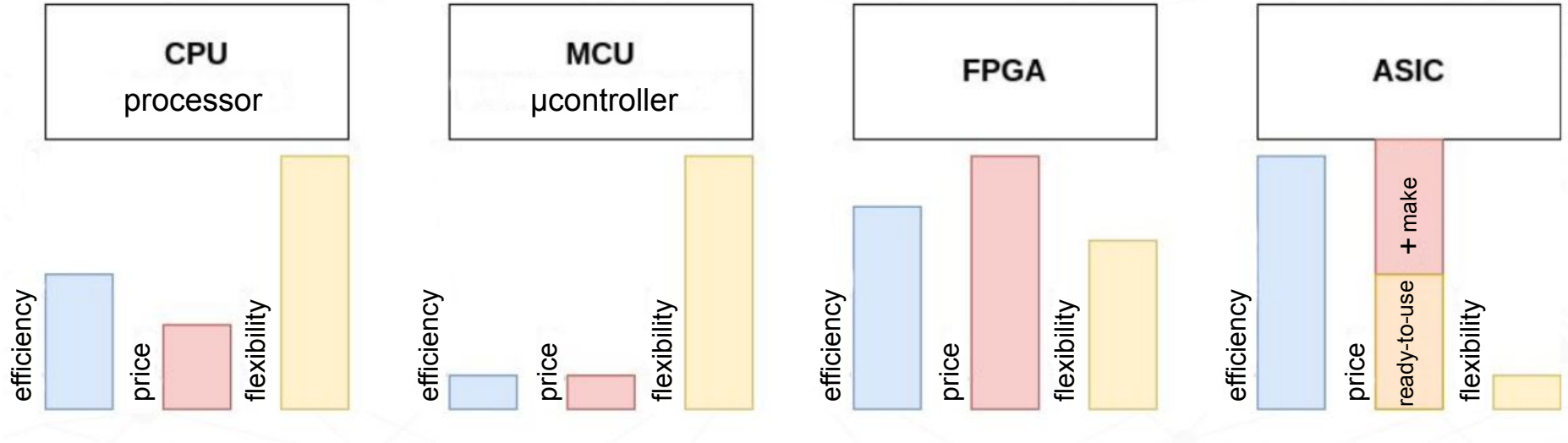


What is FPGA?

FPGA doesn't execute program!



What is FPGA?

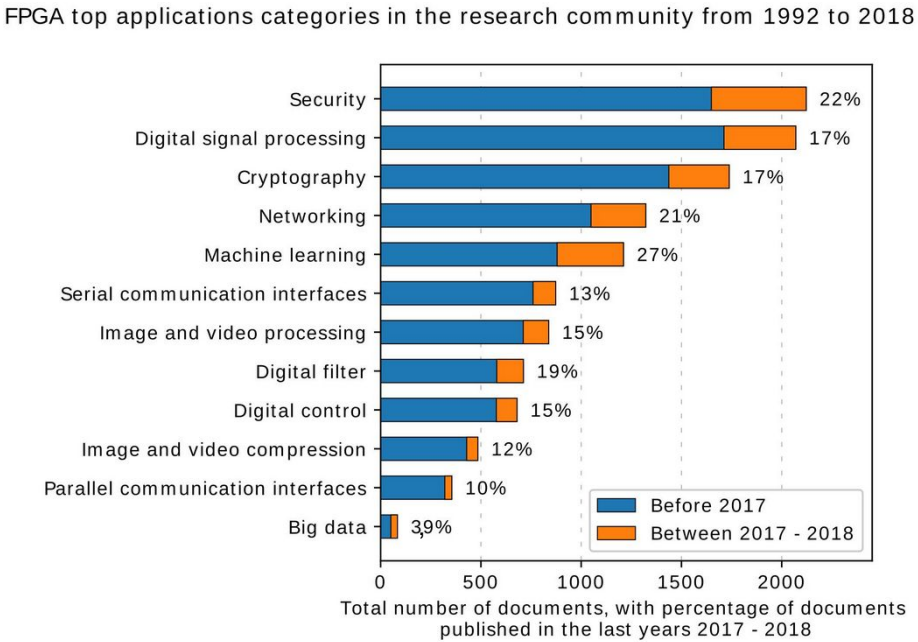


FPGAs will be used, if CPU efficiency is not enough and there are not ready-to-use ASICs

Applications

- **Aerospace & Defense**
  - Radiation-tolerant FPGAs along with intellectual property for image processing, waveform generation, and partial reconfiguration for SDRs.
- **Automotive**
  - Automotive silicon and IP solutions for gateway and driver assistance systems, comfort, convenience, and in-vehicle infotainment.
- **Data Center**
  - Designed for high-bandwidth, low-latency servers, networking, and storage applications to bring higher value into cloud deployments.
- **Video & Image Processing**
  - Computer Vision

Where FPGA is used?



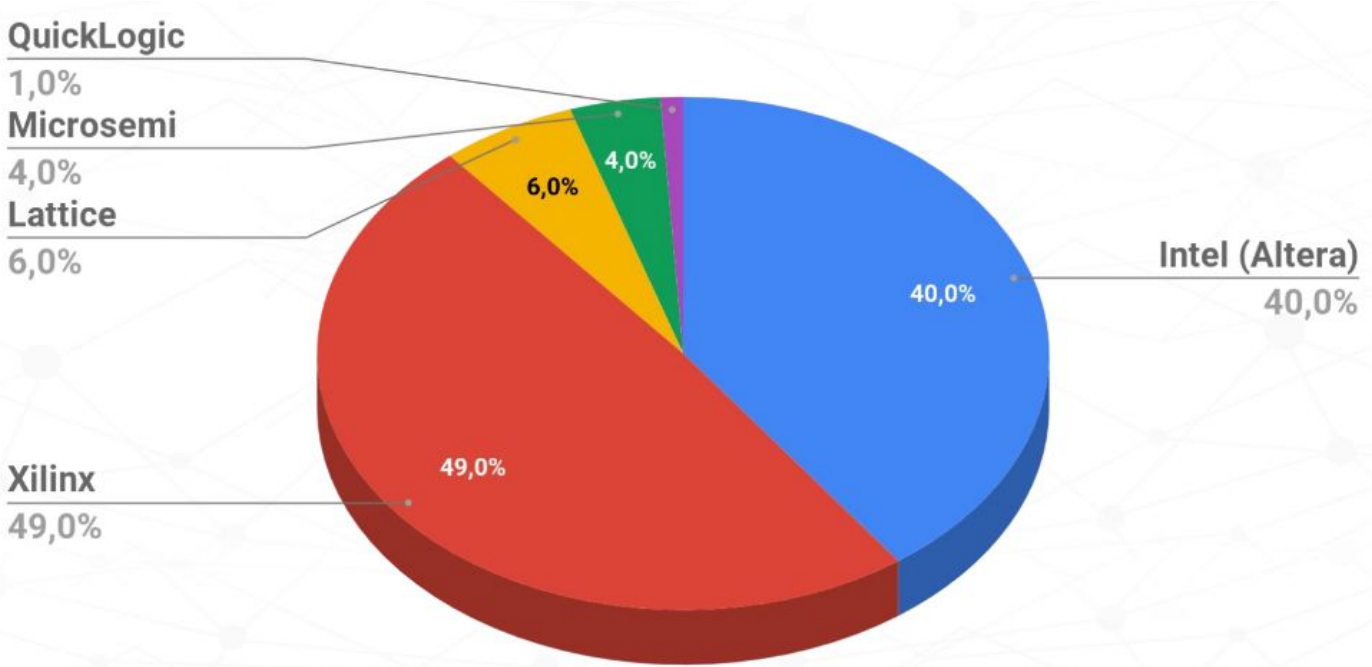
Field Programmable Gate Array Applications - A Scientometric Review

https://www.mdpi.com/2079-3197/7/4/63

FPGA Vendors

- AMD/Xilinx
- Intel/Altera
- Lattice
- Microchip/Microsemi/Actel
- Achronix
- Efinix
- Anlogic
- Quicklogic
- Gowin
- Cologne Chip
- NanoXplore

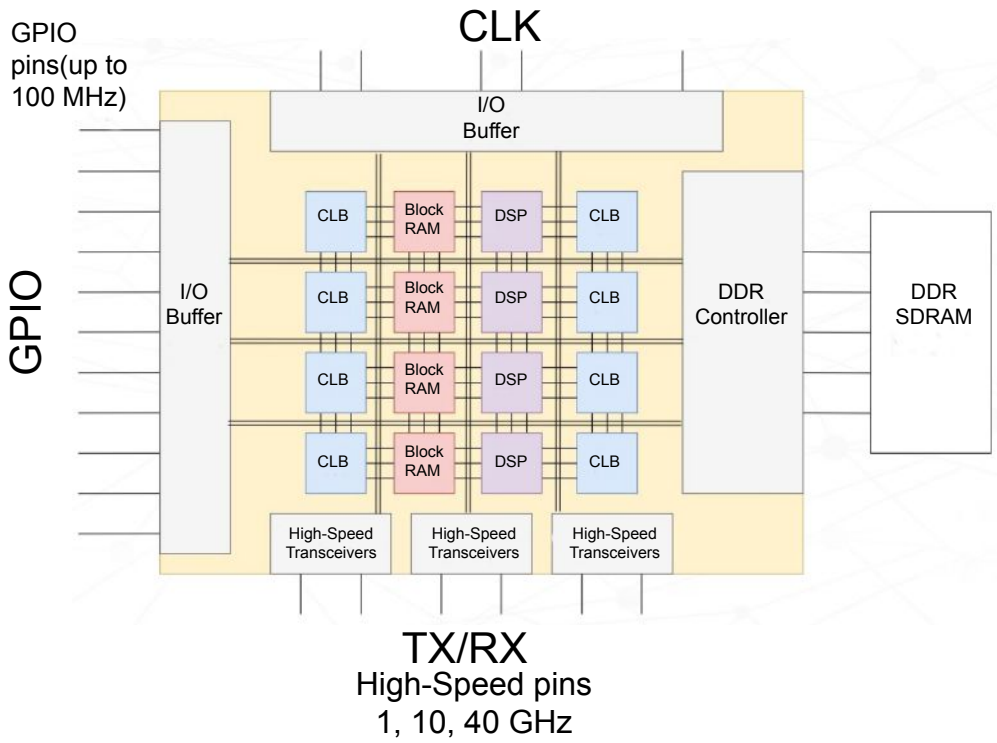
FPGA Vendors



An introduction to FPGAs and Their MPSOCs(2018): [An introduction to FPGAs and Their MPSOCs]

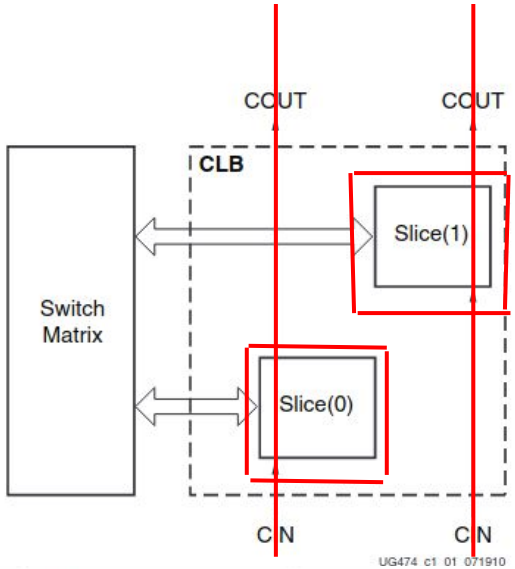
FPGA Architecture

- I/O Buffer
  - Clock buffers
    - connect inputs with special clock lines
  - IO Buffers
    - matching with external circuit
- CLB
  - configurable logic block
- Block RAM
  - internal memory
- DSP
  - hardware multipliers
- Transceivers
  - serializer
  - deserializer



FPGA Architecture

CLB

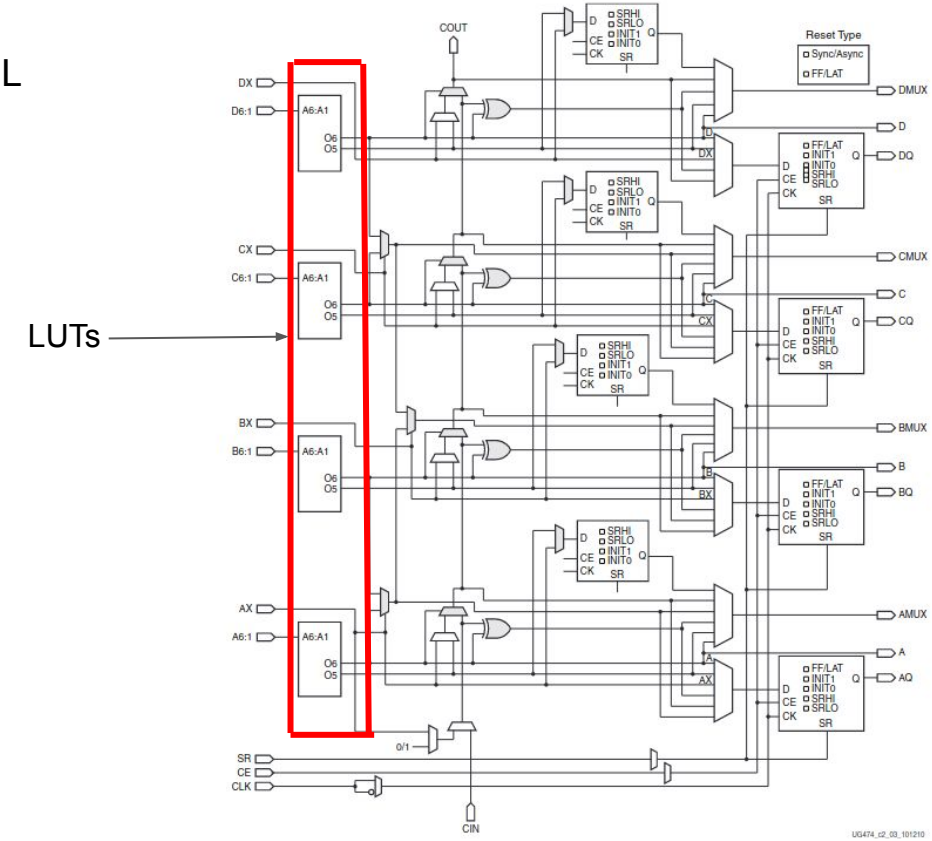


CLB Slice	LUTs	Flip-Flops	Arithmetic and Carry Chains	Wide Multiplexers	Distributed RAM	Shift Registers
SLICEL	8	16	1	F7, F8, F9	N/A	N/A
SLICEM	8	16	1	F7, F8, F9	512 bits	256 bits

Xilinx. 7 Series FPGAs CLB

FPGA Architecture

- **CLB:**
  - SliceL

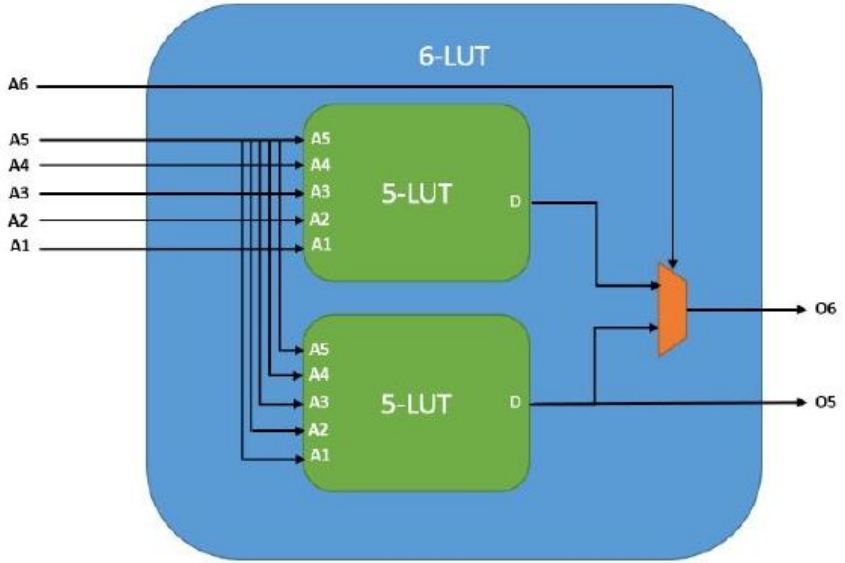


[Xilinx. 7 Series FPGAs CLB]

FPGA Architecture

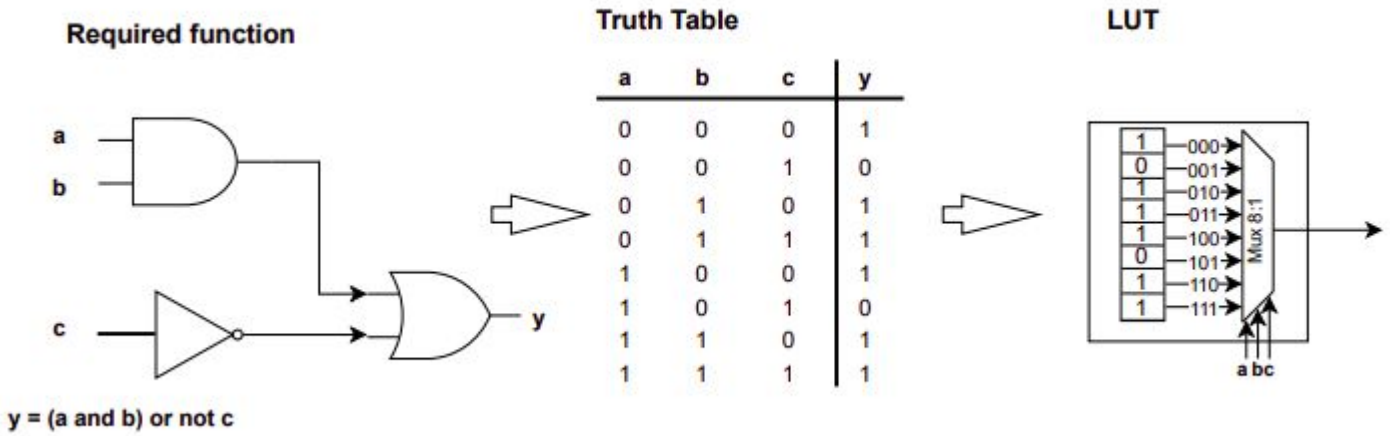
- **Look-Up Table(LUT)**

A six-input function uses:
• A1-A6 inputs
• O6 output
Two five-input or less functions use:
• A1–A5 inputs
• A6 driven High
• O5 and O6 outputs



FPGA Architecture

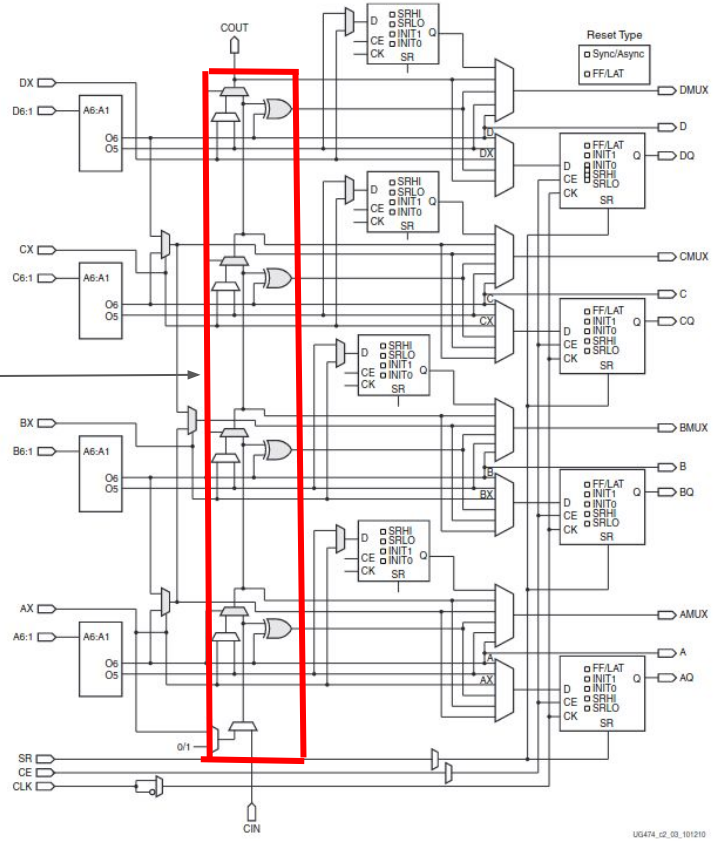
- **Look-Up Table(LUT)**



FPGA Architecture

- **CLB:**
  - SliceL

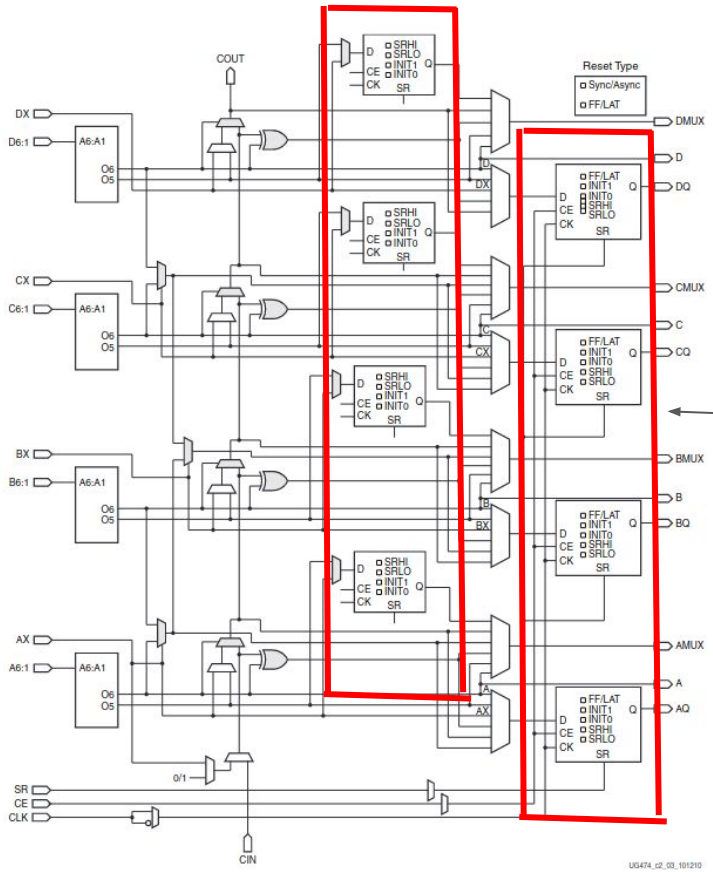
Arithmetic and Carry Chains



[Xilinx. 7 Series FPGAs CLB]

FPGA Architecture

- **CLB:**
  - SliceL

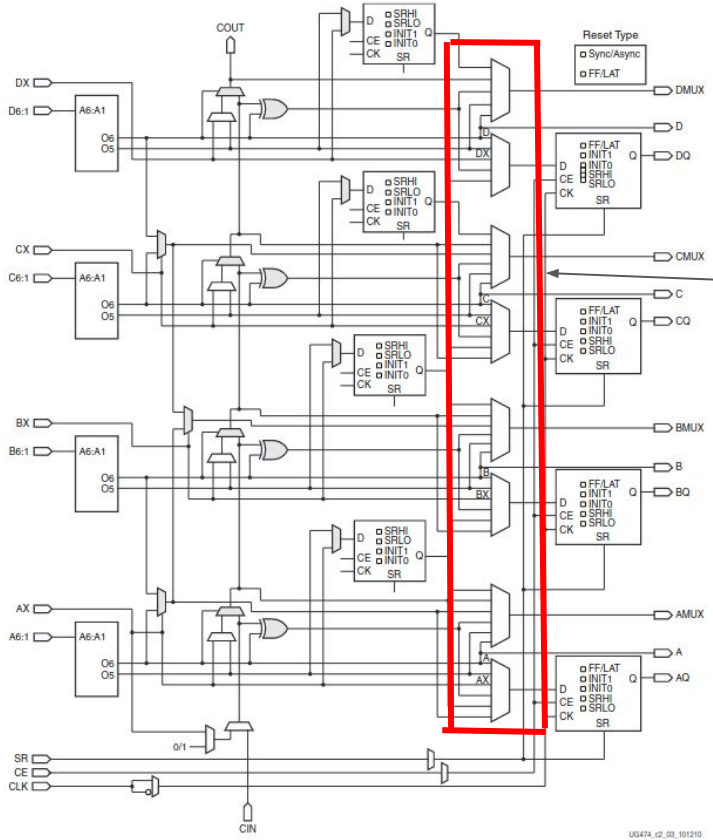


D-type flip-flops

[Xilinx. 7 Series FPGAs CLB]

FPGA Architecture

- **CLB:**
  - SliceL

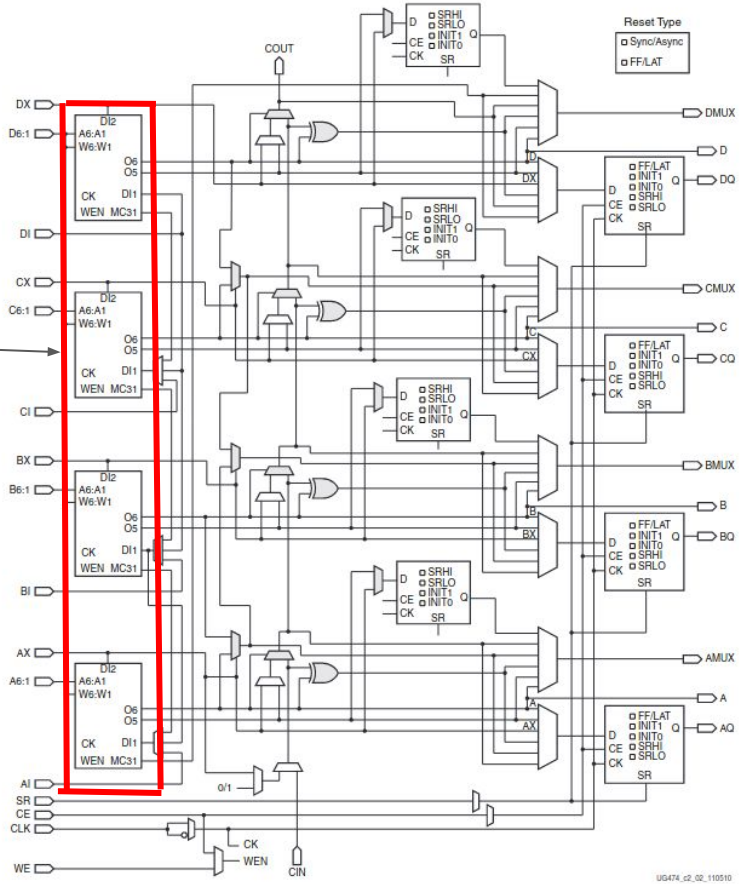


Multiplexers

Xilinx. 7 Series FPGAs CLB

FPGA Architecture

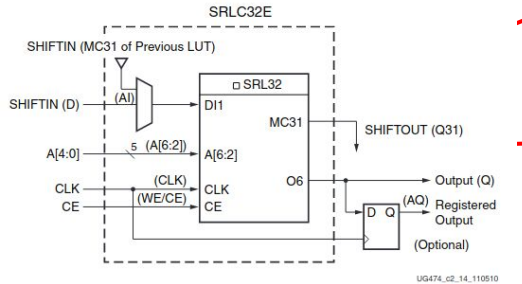
- **CLB:**
  - SliceM

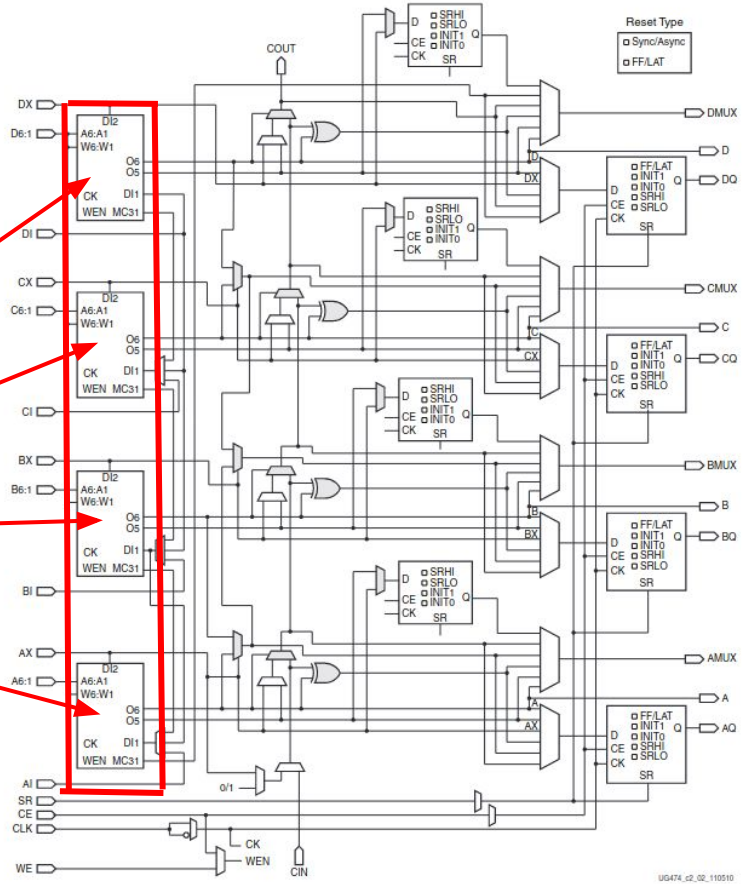


[Xilinx. 7 Series FPGAs CLB]

FPGA Architecture

- **CLB:**
  - SliceM

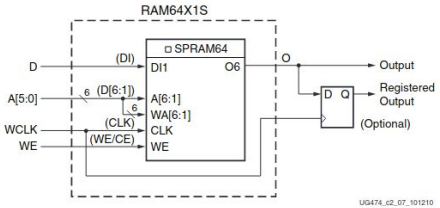


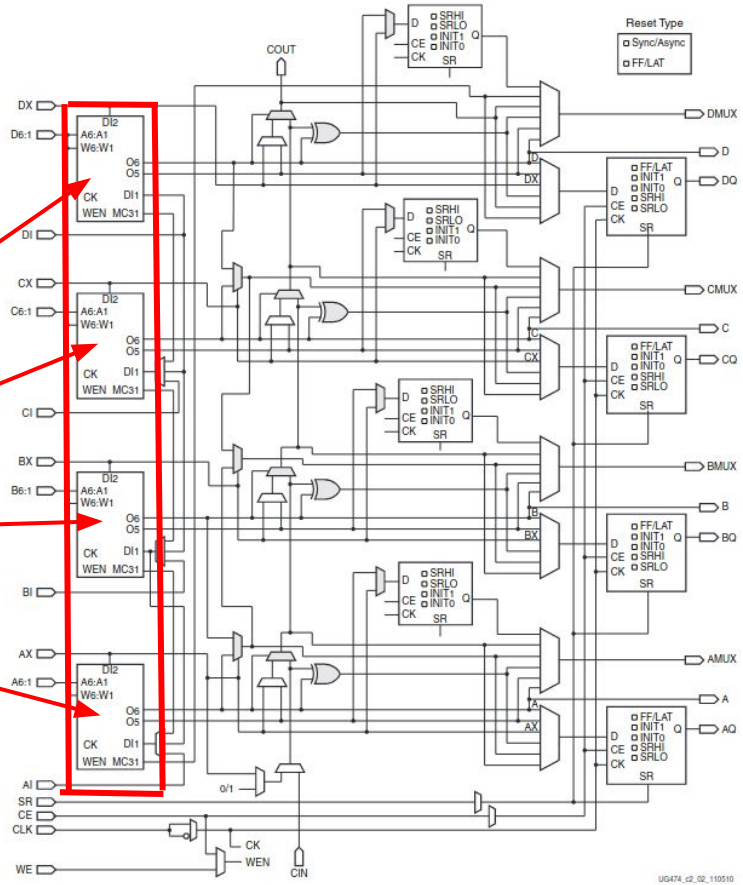


[Xilinx. 7 Series FPGAs CLB]

FPGA Architecture

- **CLB:**
  - SliceM



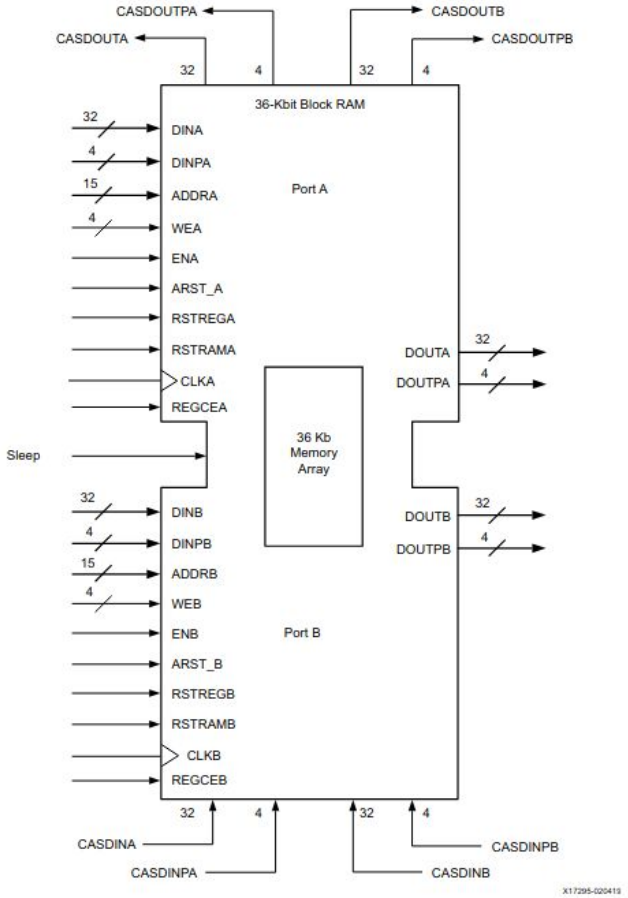


Michael Krekker
20. Oktober 2021

Xilinx. 7 Series FPGAs CLB

FPGA Architecture

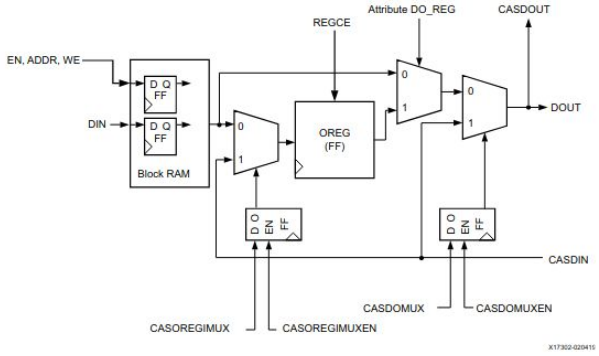
- **BRAM(Block RAM)**

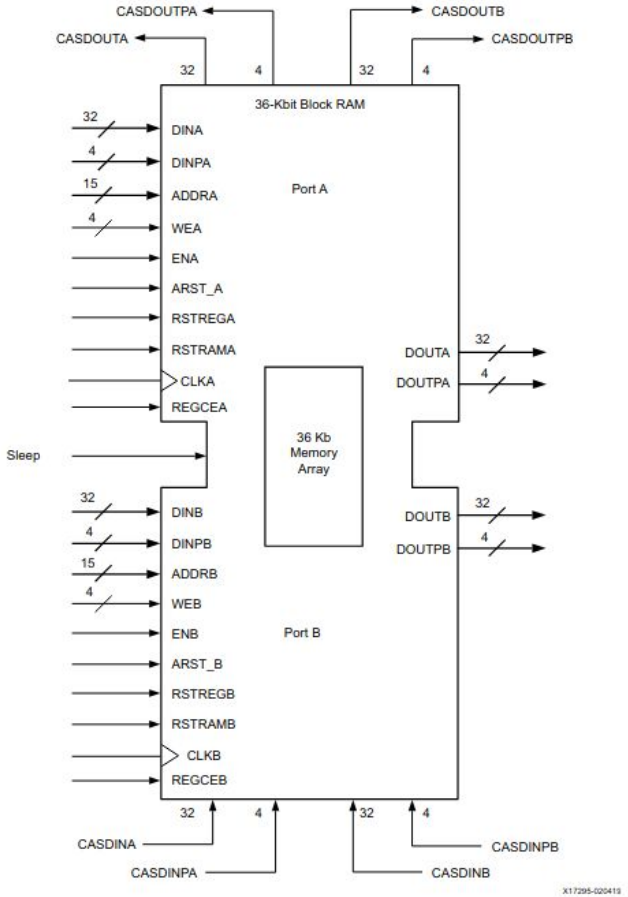


[Xilinx. BRAM UltraScale]

FPGA Architecture

- **BRAM(Block RAM)**

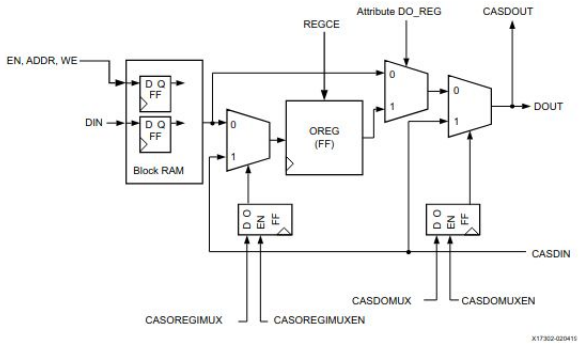


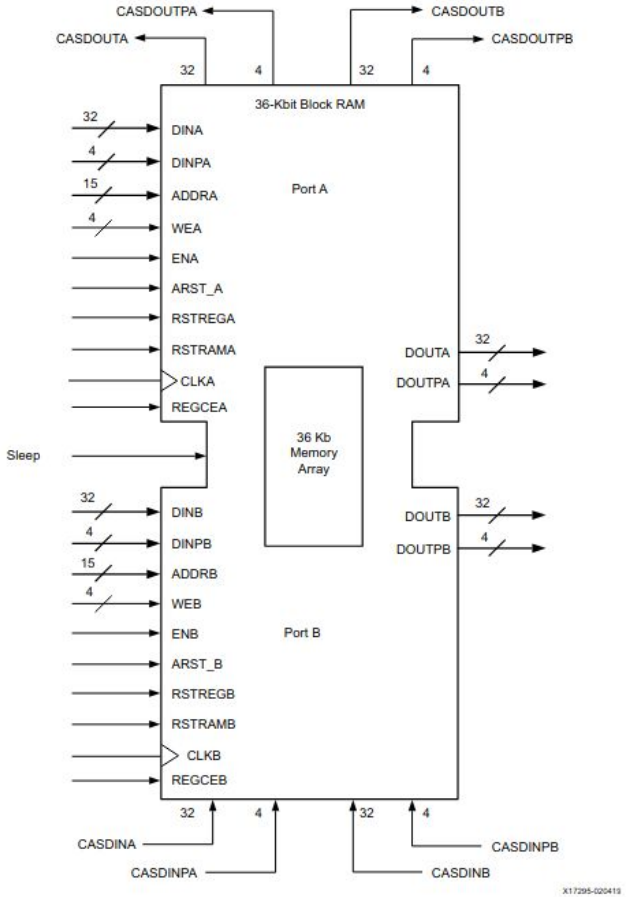


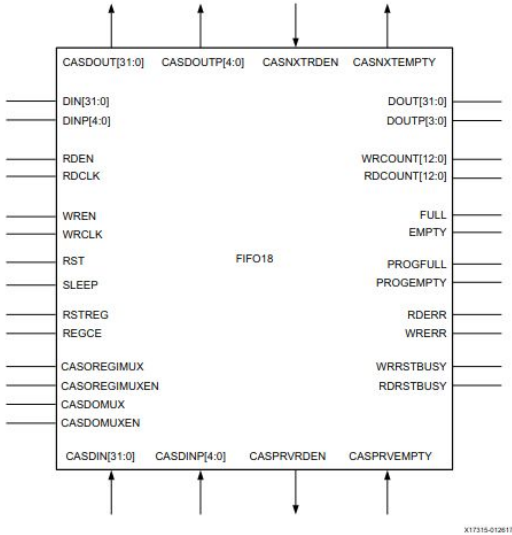
Xilinx. BRAM UltraScale

FPGA Architecture

- **BRAM(Block RAM)**



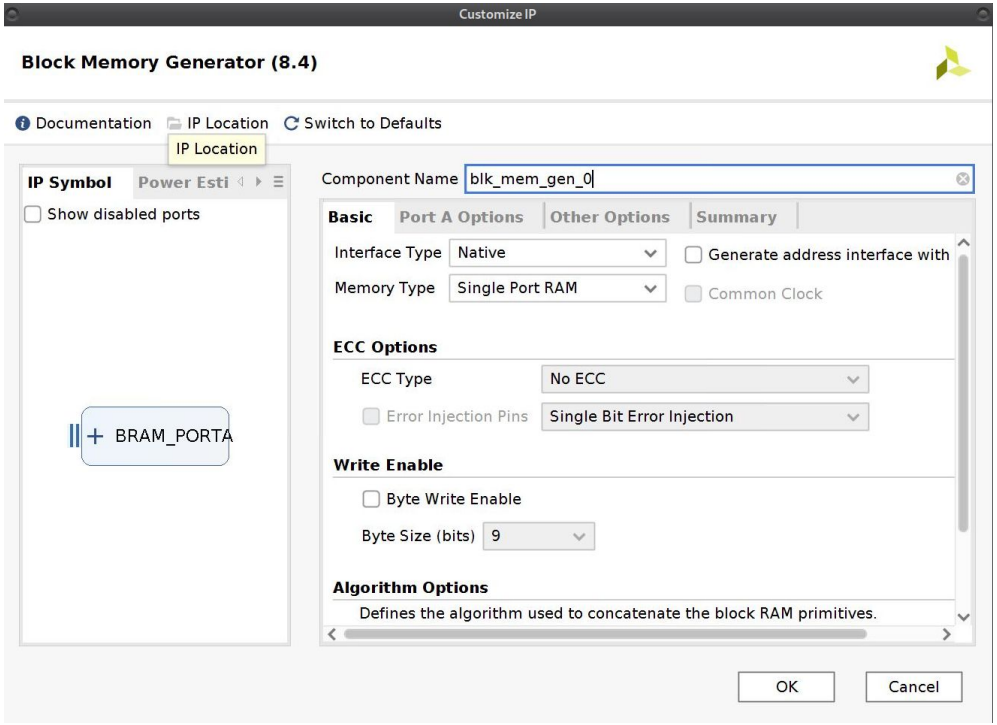




[Xilinx. BRAM UltraScale]

FPGA Architecture

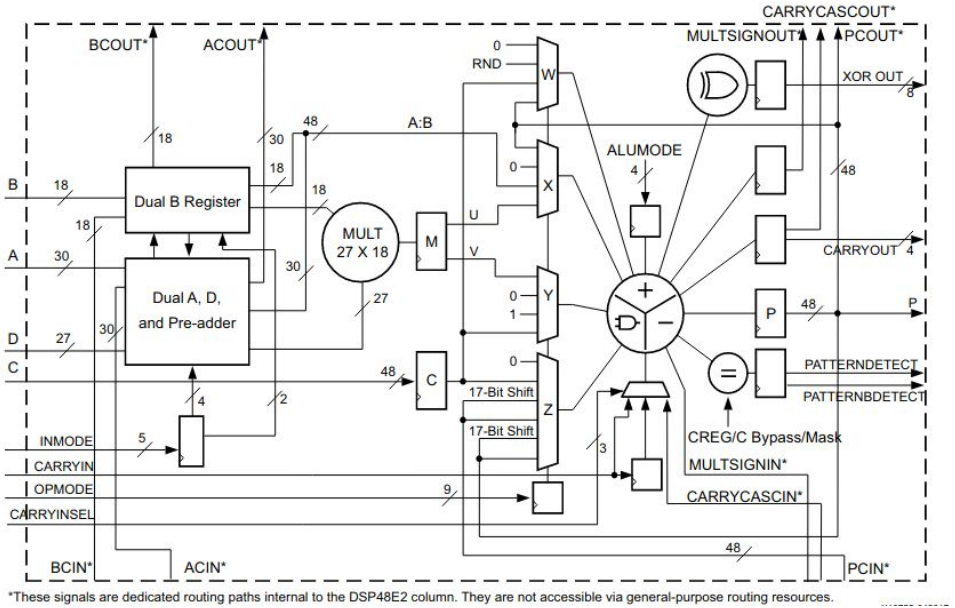
- **BRAM(Block RAM)**



Xilinx.Vivado. Block Memory Generator

FPGA Architecture

- **DSP48E2(Digital Signal Processing)**

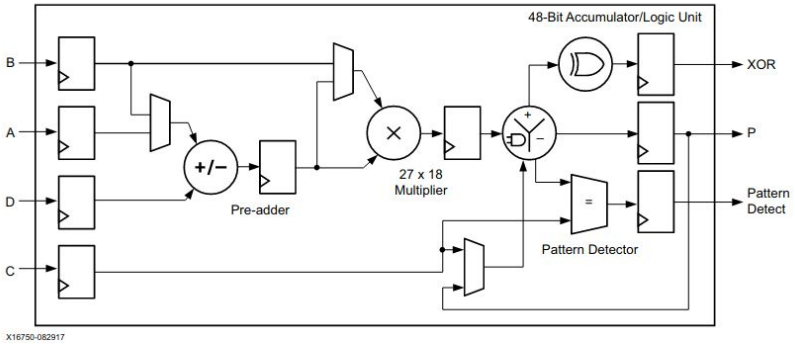


*These signals are dedicated routing paths internal to the DSP48E2 column. They are not accessible via general-purpose routing resources.

Xilinx. DSP UltraScale

FPGA Architecture

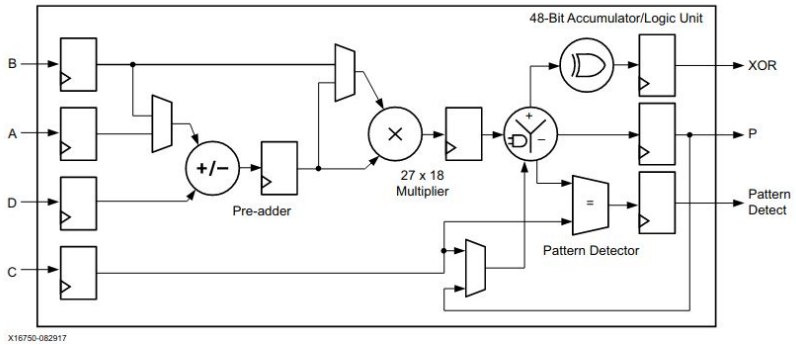
- **DSP48E2(Digital Signal Processing)**



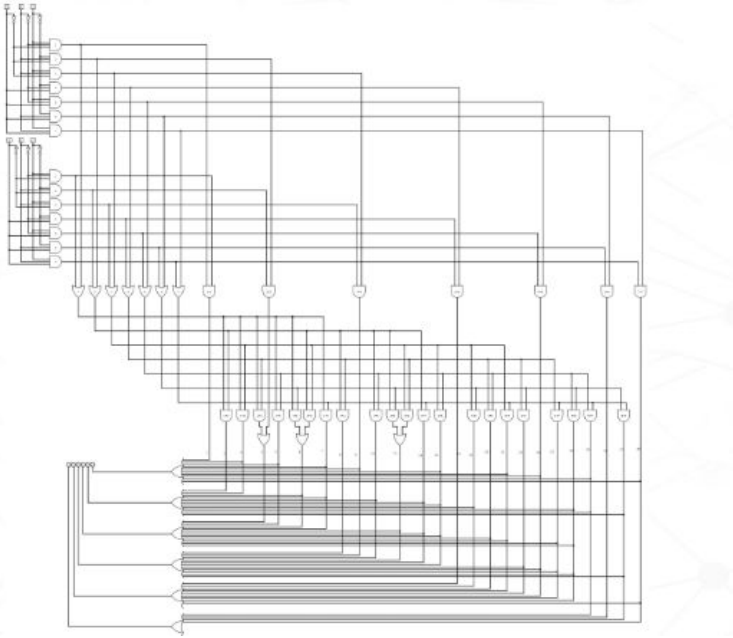
Xilinx. DSP UltraScale

FPGA Architecture

- **DSP48E2(Digital Signal Processing)**
  - Multiplier 27 x 18



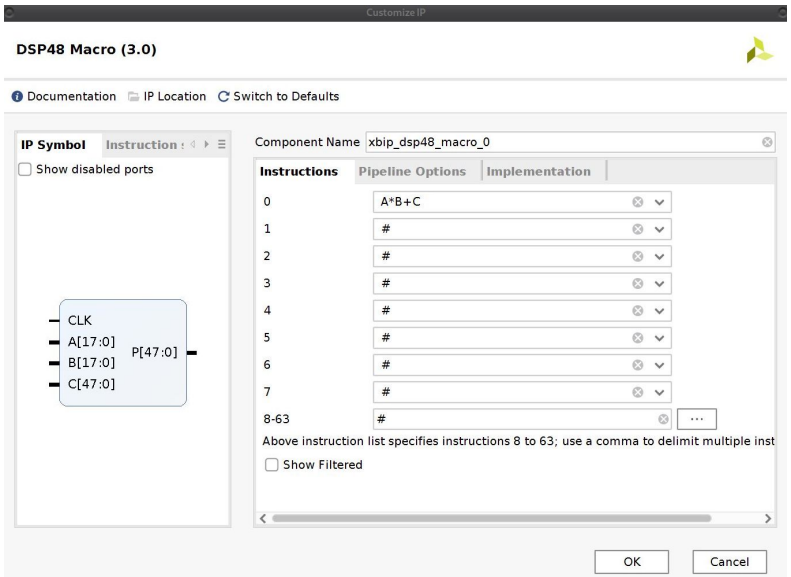
  - Multiplier 3 x 3

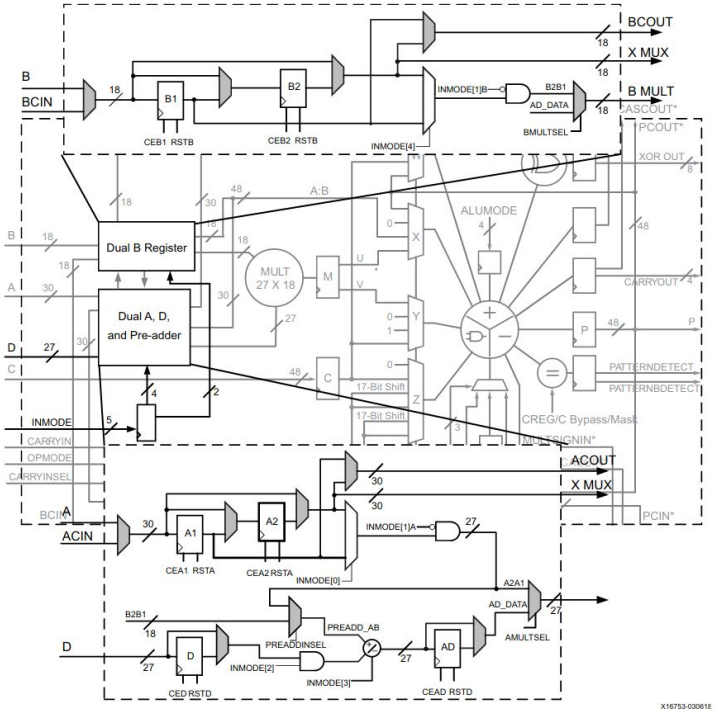


Xilinx. DSP UltraScale

FPGA Architecture

- **DSP48E2(Digital Signal Processing)**





Michael Krekker
20. Oktober 2021

Xilinx. Vivado. DSP48 Macro

FPGA Architecture

- **Clock**
  - *PLL/DLL(Phase/Delay Locked Loop)*
  - *MMCM(Mixed-Mode Clock* Manager)

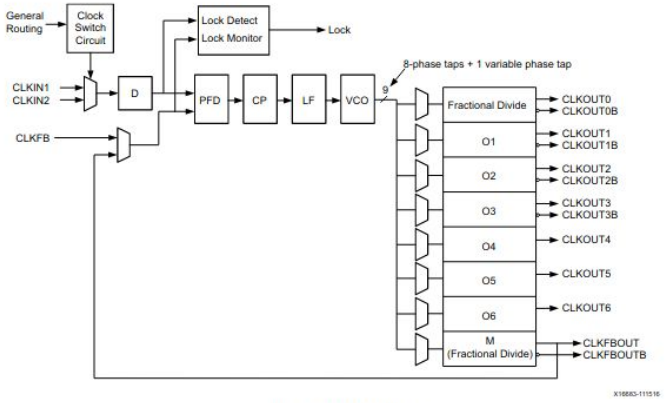
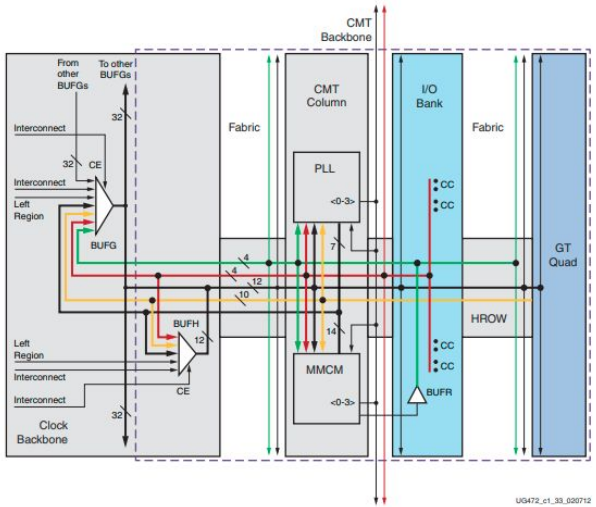


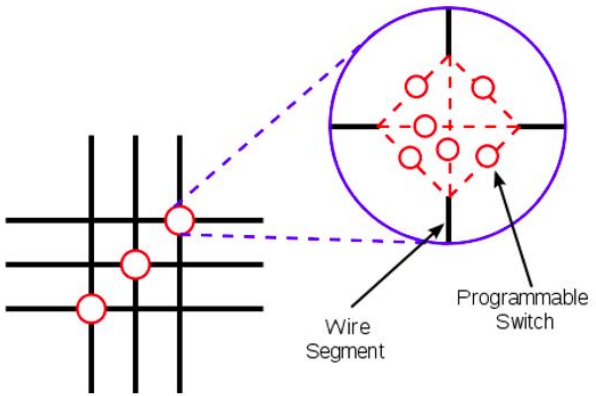
Figure 3-1: **Detailed MMCM Block Diagram**

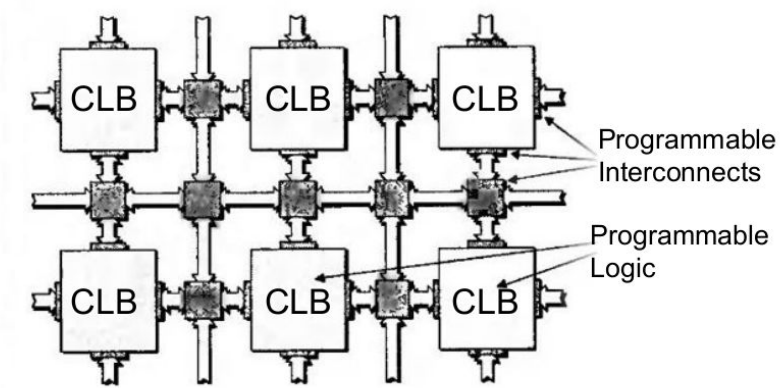


Xilinx. UltraScale Clocking Resources

FPGA Architecture

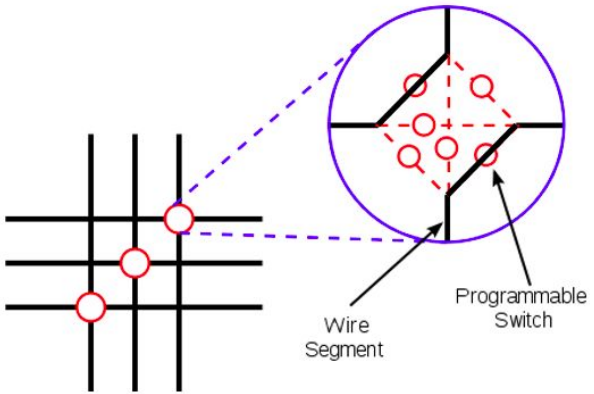
- **Interconnects**

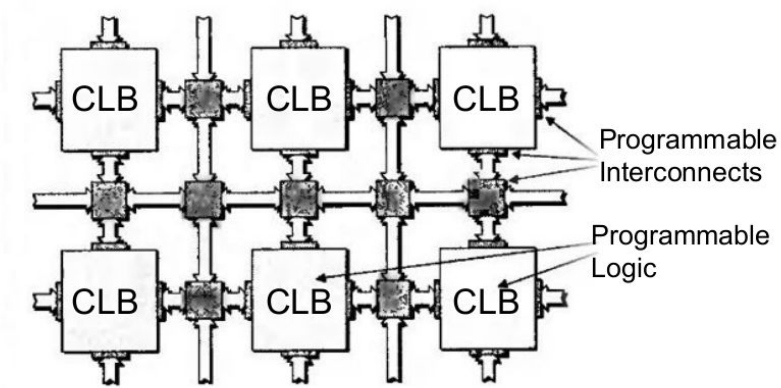




FPGA Architecture

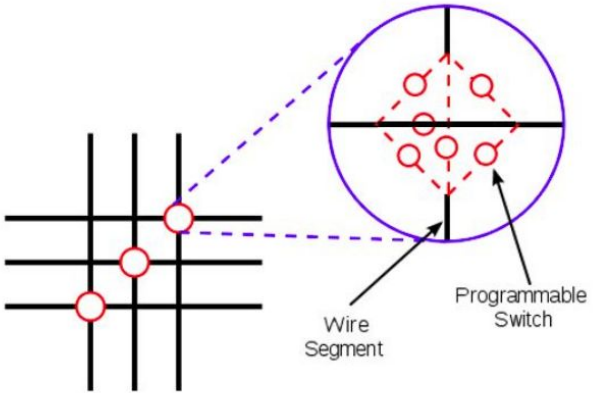
- **Interconnects**

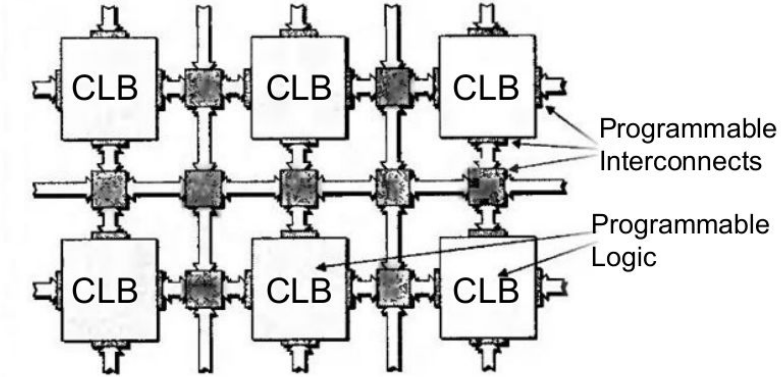




FPGA Architecture

- **Interconnects**

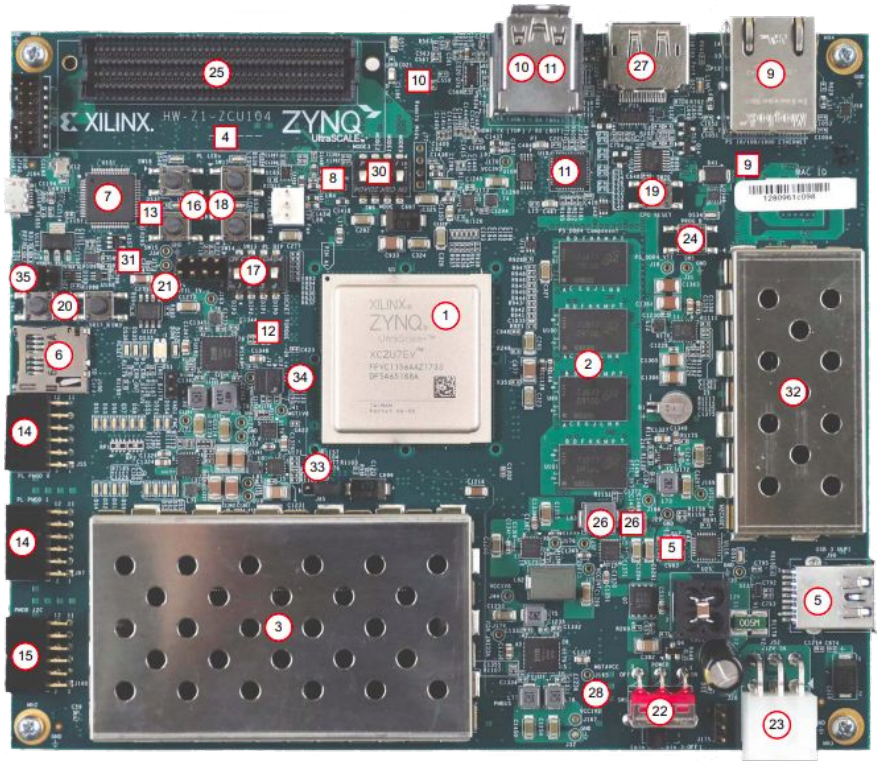




FPGA Architecture

- **Other Blocks**
  - PCI Express
  - high-speed transceiver
  - controller external memory
  - ADC
  - Processors

Zynq UltraScale+ MPSoC ZCU104



- CLB - 504k
- BRAM - 38 Mb
- DSP - 1728
- I/O Pins - 464
- Arm Cortex-A53

Michael Krekker
20. Oktober 2021

UG1267 - ZCU104 Board User Guide (v1.1)

Zynq UltraScale+ MPSoC ZCU104

The 6 steps to implement designs on FPGA's remotely

1. Establishing a VPN connection with the university network
2. Establishing a remote connection using X2GO client
3. Establishing a remote connection using SSH
4. Start the hw_server application
5. Implementation of VHDL program on Vivado Design Suite
6. Setup and Program FPGA

Michael Krekker
20. Oktober 2021

Books and papers

11 Reasons You Should NOT use an FPGA for a Design,
and Four Reasons You Should

David Harris, Sarah Harris. «Digital Design and Computer Architecture» - must read, for every Digital Designer

Pong Chu.«FPGA prototyping by VHDL examples»

Peter J. Ashenden. «The Designer's Guide to VHDL»

100 Power Tips for FPGA Designers

Steve Kilts. «Advanced FPGA Design»

Digital Arithmetic - many realisation of multiplier, adder and etc.

Altera. «Understanding Metastability»

Asynchronous & Synchronous Reset

Tutorials, blogs

https://www.fpga4fun.com/ - different projects on FPGA

projectf.io - grafics on FPGA

beyond-circuits.com - blog about FPGA

https://vhdlwhiz.com - development blog about VHDL and courses

adiuvoengineering - Adam Taylor's personal blog (Microzed Chronicles)

https://www.fpga4student.com - portal with FPGA projects

FPGA designs with VHDL

https://verificationacademy.com - Portal and competence center for verification of FPGA projects

UVM Tutorial for Candy Lovers - Source Code (GitHub)

UVM Tutorial for Candy Lovers - Official site

ZCU104 Manuals

Zynq UltraScale+ MPSoC ZCU104

Configurable Logic Block

Memory Resources

DSP Slice

Clocking Resources

SelectIO Resources

Vivado Design Suite
Synthesis

Zynq UltraScale+ Device

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Youtube tutorials and more

David L. Jones (EEVblog). «What Is An FPGA?»

Mohammad S. Sadri - lessons about Zynq

Vipin Kizheppatt - mini lessons about FPGA and work with it

NANDLAND

How To Create Difficult FPGA Designs with CPU, MCU, PCIE, ... (with Adam Taylor)

Xilinx. «Getting Started with the Vivado IDE»

High-Speed Serial I/O Made Simple

Automotive: example1 and example2

SDR.How does it work?

Data Center Acceleration

High Performance Computing

Computer Vision Project with zynq board

FPGA based Astronomy

Thanks to Mikail Yayla, Sanad Marji and Maksim Tolkachev
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Thank you
for your attention

Michael Krekker
20. Oktober 2021