中山大学本科生期末考试

考试科目：《数 字 电 路 》（A 卷）答案

学年学期：2017 学年第二学期　　姓　　名：_____

学 院/系：电子与信息工程学院　　学　　号：_____

考试方式：闭卷　　年级专业：_____

考试时长：120 分钟　　班　　别：_____

警示 《中山大学授予学士学位工作细则》第八条：“考试作弊者，不授予学士学位。”

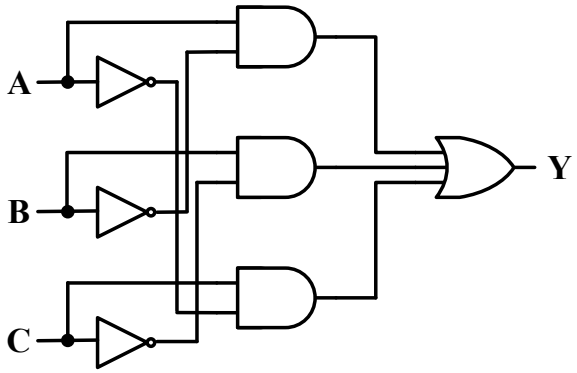
----------以下为试题，共 **2** 道大题，总分 **100** 分,考生请在答题纸上作答----------

一、填空题（共 25 小题，每个答案 2 分，共 50 分）

1. 10101010
2. 0.0101000
3. 011011
4. 11011
5. 1
6. $X = \overline{A}B + A\overline{B}$
7. $X = \left(\overline{A}+B+C\right)\left(\overline{A}+B+\overline{C}\right)\left(A+B+C\right)$
8. AND
9. NAND
10. COMP A
11. Propagation delay 传输延迟时间
12. 不可重复触发
13. Astable multivibrator 振荡器
14. 2Hz
15. 8
16. 1000
17. Faster speed 速度快
18. EEPROM
19. word length 字长
20. 255
21. Dual slope ADC
22. R-2R Ladder DAC
23. NOT
24. ON OFF

二、分析设计题（共 4 小题，共 50 分）

1. Write the output expression for the circuit shown below, obtain the truth table according to the expression, and determine the logic function. (写出所示逻辑电路的输出表达式, 列出真值表,并确定其逻辑功能) (8 points)



(Question. 1)

答案:

$Y = A\overline{B} + B\overline{C} + \overline{A}C$ (**2 points**)

Input			
A	**B**	**C**	**Y**
0	**0**	**0**	**0**
0	**0**	**1**	**1**
0	**1**	**0**	**1**
0	**1**	**1**	**1**
1	**0**	**0**	**1**
1	**0**	**1**	**1**
1	**1**	**0**	**1**
1	**1**	**1**	**0**

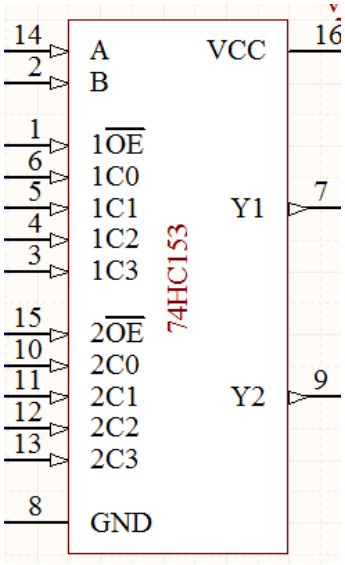
(**4 points**)

Logic function：The output is high when the inputs are different. (**2 points**)

2. Design a 1 bit full subtractor (设计一个一位全减器来计算 A-B-C), which computes A-B-C, where C is the borrow from the next less significant digit (其中 C 是来自低位的借位). It produce a difference D and a borrow from the next more significant bit P. (它将得到差 D 和对高位的借位)

(a) Implement the full subtractor by gates(write down the logic functions for the D and P, don't draw the circuit diagram) (采用逻辑门实现这个全减器，只需写出 D 和 P 的逻辑表达式，不需要画出电路图) (8 points)

(b) Implement the full subtractor by 74LS153 multiplexer and some gates (draw the circuit diagram). 74HC153 has two identical 4-input multiplexers which select two bits of data from up to four sources according to common data select inputs. (采用 74LS153 和逻辑门来实现这个全减器，需画出具体电路图，其中 74HC153 包含两个四输入多路复用器) (4 points)



(Question. 2)

答案:

The truth table for the full subtractor is as follows:

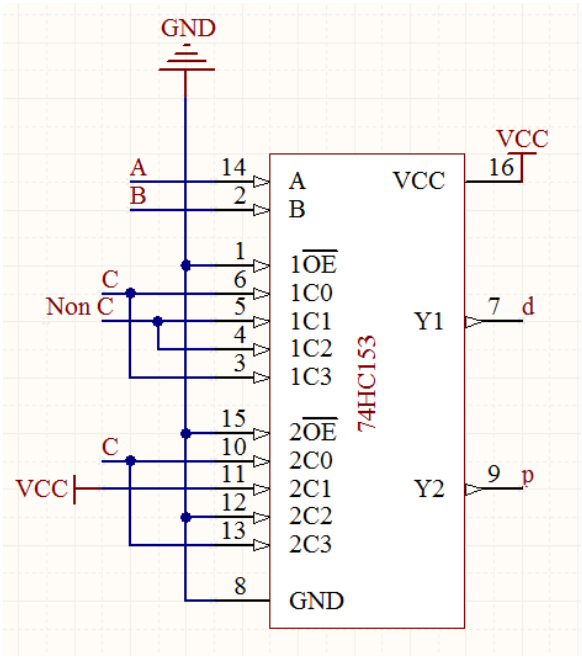
a	b	c	p	d
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(4 points)

$$d = \bar{a}\bar{b}\,c + \bar{a}\,b\,\bar{c} + a\,\bar{b}\,\bar{c} + a\,b\,c$$

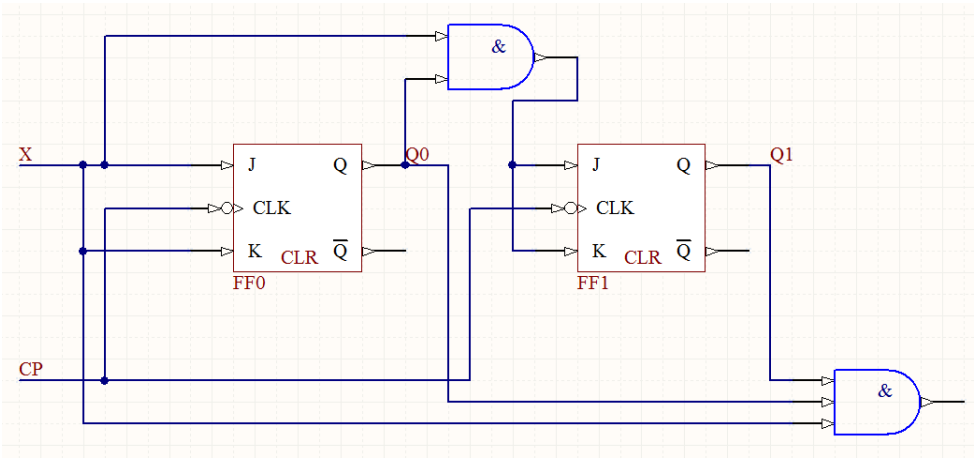
$$p = \bar{a}\bar{b}c + \bar{a}b\bar{c} + \bar{a}bc + abc = b\,c + \bar{a}\,c + \bar{a}\,b$$

(4 points)



(4 points)

3. Determine the logic function of the circuit sketched below. (确定下图所示电路的逻辑功能) The detailed procedure is required. (需给出具体过程) (14 points)



(Question. 3)

答案:

Excitation expression:

$$\begin{cases} J_0 = K_0 = X \\ J_1 = K_1 = XQ_0^n \end{cases}$$

State expression:

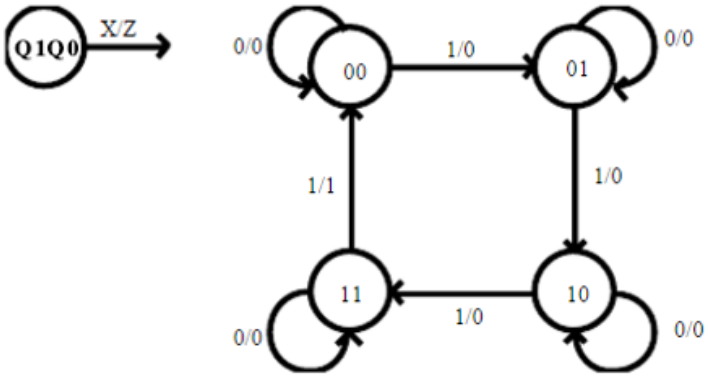
$$\begin{cases} Q_0^{n+1} = X \cdot \overline{Q_0^n} + \overline{X} \cdot Q_0^n \\ Q_1^{n+1} = X \cdot Q_0^n \cdot \overline{Q_1^n} + \overline{X \cdot Q_0^n} \cdot Q_1^n \end{cases}$$

Output expression:

$$Z = X \cdot Q_0^n \cdot Q_1^n$$ **(6 points)**

	X=0	X=1
00	00 / 0	01 / 0
01	01 / 0	10 / 0
10	10 / 0	11 / 0
11	11 / 0	00 / 1

(4 points)



Logic function:

When X=0, the circuit remains unchanged.

When X=1, the circuit is a four bits synchronous binary counter. **(4 points)**

4. Design a synchronous modulus-5 counter using D flip-flops and necessary gates(用 D 触发器和必要逻辑门设计一个同步模-5 计数器). The counter is required to go through the following sequence: 0->2->4->1->3->0->…. (要求计数器产生以下时序: 0, 2, 4, 1, 3, 0,…) The detailed procedure is required. (需给出具体过程). (16 points)

答案:

$Q_2^nQ_1^nQ_0^n$	$Q_2^{n+1}Q_1^{n+1}Q_0^{n+1}$	Z
000	010	0
010	100	0
100	001	0
001	011	0
011	000	1

(6 points)

$Q_2^{n+1} = D_2, Q_1^{n+1} = D_1, Q_0^{n+1} = D_0$

The K-map

Q2 \ Q1Q0	00	01	11	10
0	0	0	0	1
1	0	X	X	X

$D_2 = Q_1\overline{Q_0}$

Q2 \ Q1Q0	00	01	11	10
0	1	1	0	0
1	0	X	X	X

$D_1 = \overline{Q_1} \bullet \overline{Q_2}$

Q2 \ Q1Q0	00	01	11	10
0	0	1	0	0
1	1	X	X	X

$D_0 = Q_2 + \overline{Q_1}Q_0$

Q2 \ Q1Q0	00	01	11	10
0	0	0	1	0
1	0	X	X	X

$Z = Q_1Q_0$

(4 points)

Excitation expression.

$D_2 = Q_1 \cdot \overline{Q_0}$, $D_1 = \overline{Q_2} \cdot \overline{Q_1}$, $D_0 = Q_2 + \overline{Q_1} \cdot Q_0$, $Z = Q_1Q_0$ **(4 points)**

Check self boot

$Q_2^nQ_1^nQ_0^n$	$Q_2^{n+1}Q_1^{n+1}Q_0^{n+1}$	Z

000	010	0
010	100	0
100	001	0
001	011	0
011	000	1
101	001	0
110	101	0
111	001	1

The circuit can self boot. **(2 points)**