محمدمهدی مطری - ۹۹۲۱۰۹۱ - پیش گزارش آزمایش ۹

بخش verilog

```
`timescale 1 ns/1 ns
module DFF (Q, QP, D, clk, res);

input D, clk, res;

output reg Q;

output QP;   assign QP = ~Q;
always @(negedge clk or negedge res)

begin
  if( res == 1'b0 )
    Q <= 1'b0;
  else
  #5 Q <= D;
end

endmodule


module circuit (Y, Z, A, B, clk, res);

  output Y, Z;

  input A, B, clk, res;

  wire S, w1, w2, w3, R, w4, w5;

  and #(10) F1 (S, B, w4);

  or #(10) F2 (w1, S, A);
```

```
DFF #(5) F3 (Y, w2, w1, clk, res);

nor #(10) F4 (w3, w1, w2);

DFF #(5) F5 (w5, w4, w3, clk, res);

and #(10) F6 (R, w4, B);

or #(10) F7 (z, w2, R);

endmodule

module tb_circuit();

reg A, B, clk, res;

wire Y, Z;

circuit G1 (Y, z, A, B, clk, res);

initial begin

clk = 1'b0;

forever #40 clk = ~clk;

end
```

repeat (18)

```
#40 clk = ~clk;
```

```
initial begin
    res = 1'b1;
    A = 1'b0;
    B = 1'b0;
    #80;
    res = 1'b1;
    A = 1'b0;
    B = 1'b1;
    #40;
    res = 1'b1;
    A = 1'b1;
    B = 1'b1;
    #80;
    res = 1'b1;
    A = 1'b0;
    B = 1'b1;
    #80;
    res = 1'b1;
    A = 1'b0;
    B = 1'b0;
    #40;
    res = 1'b1;
    A = 1'b1;
    B = 1'b0;
    #120;
    res = 1'b1;
    A = 1'b1;
    B = 1'b1;
    #40;
    res = 1'b1;
    A = 1'b0;
    B = 1'b0;
    #120;
    res = 1'b1;
    A = 1'b0;
    B = 1'b1;
    #40;
    res = 1'b1;
    A = 1'b1;
    B = 1'b1;
    #80;
end
endmodule
```