```
`timescale 1 ns/1 ns

module adder_1bit (s, co, ci, a, b);

  input a, b, ci;

  output s, co;

  wire w1, w2, w3, w4;

  xor #(10) F1 (w1, b, ci);

  xor #(10) F2 (w3, a, w1);

  xor #(10) F3 (s, w2, ci);

  and #(5) F4 (w2, w1, a);

  and #(5) F5 (w4, w2, ci);

  or #(5) F6 (co, w4, w2);

endmodule
```

```
`timescale 1 ns / 1 ns

module adder_4bit(s, Co, Ci, a, b);

  input [3:0] a;

  input [3:0] b;

  input Ci;

  output [3:0] s;

  output Co;

  wire [6:0] w;


xor #(1.) G1(w[0], Ci, b[0]);
xor #(1.) G2(w[1], Ci, b[1]);
xor #(1.) G3(w[2], Ci, b[2]);
xor #(1.) G4(w[3], Ci, b[3]);
adder_1bit G0(s[0], w[4], Ci, a[0], b[0]);
adder_1bit G1(s[1], w[5], w[4], a[1], b[1]);
adder_1bit G2(s[2], w[6], w[5], a[2], b[2]);
adder_1bit G3(s[3], Co, w[6], a[3], b[3]);

endmodule
```

testbench

```
`timescale 1 ns/1 ns

module tb_adder_4bit();

reg [3:0] a, b;

reg Ci;

wire [3:0] S;

wire Co;

adder_4bit T1 (S, Co, Ci, a, b);

initial
  begin
    a = 4'b0001;
    b = 4'b0001;
    Ci = 1'b0;
    #10;
    a = 4'b0100;
    b = 4'b0001;
    ci = 1'b0;
    #10;
```

سلف حالی جمع

```
    a = 4'b1110;
    b = 4'b0011;
    Ci = 1'b0;
    #20;
```

حالت های تمرین

```
a = 4'b0001;
b = 4'b0001;
ci = 1'b1;
#10;

a = 4'b1010;
b = 4'b0011;
ci = 1'b1;
#10;

a = 4'b0010;
b = 4'b1000;
ci = 1'b1;
#10;

end

endmodule
```