time scale 1 no/1 ns Verilog Jus module OFF (Q,QR,O,clk, res ); input D, clk, res; output reg Q : CP: always @ (negedge clk or negedge res) (0) H(20) F6 (B, wt. 6) if ( res == 1'60 ) (a, su, s) == (a) == vo Q <= 1'60; +5 < Q3=0: en d · Otasis de station end module. C'est adis O.A Gar module circuit (Y, Z, A, B, Clk, ves); 1 5 . Y 500 output Y, Z; 62 (Y, E) A.B. Olle, mills f ways input A, B, clk, res; road ladin 1 Od'I + 2/2 wire 5, w2, w2, w3, R, w4, w5; for the ? and # (10) F1 (s. B. W.4).); Kan or #(10) F2 (w1, s, A);

DFF#(5)F3(Y, w2, w2, clk, ra);

withit will !

nor # (10) F4. (w3, w1, w2);

DFF #(5) F5 (W5, W4, W3, clk, va);

and #(10) F6 (R, , w4, B);

or #(10) F7 (Z, w2, R);

end module

module tb\_circuit();

reg A, B, clk, res;

wire Y, Z;

circuit 61 (Y, Z, A, B, clk, ros);

initial begin

clk = 1'b0;

(18) . Trepent (18) # 40 clk = ~clk; clk = wclk; b forever #40 end

· (av. 140.8, A. S. 7) Francisco

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Coreling & tog.

initial begin		ves = 1'61;
Yes = Z'b1;		A, 1'61;
A = 1'60;		B = 1'61',
B = 1'60;		# 40;
#80;		re, z 1'61;
yes = 2'63;	٠	A = 1'60;
A = 1'50;		B = 1'60;
8 : 1/61:		
# 40 ;		# 120;
res = 1'61;	*	res = 1'61;
		A = 1'b0:
A. 1'61;	٠	B. 1'61;
3 = 1'b1;		# 40;
# 80;		
res = 1'61;		res z 1/b1:
A , 1'60;	,	A, 1'61;
B = 1'b1;		B, 1'b1;
# 80;		# 80:
res = 1'61;		4 00 ,
A = 1'b0;	e	en d
B 2 1'60;		endmodule
# 40;		
res z 1'b1;		•
A = 1/61;		
B = 1'60; # 120;		

