v 06, 1 0/10 jum - aa en . 41 محسمس تعلن -1 ns/1 ns" time scale adder_1bit (s, co, ci, a, b); a, b ; ci; S. Co; 10 1. 1. gm w, w, we, we; wile 10.83 Tagh 10 #(1.) FI(w1,b,ci); i od togtom # (1.) Fr (wr, a, w1); [6.0] # (1.) FT(S, we, Ci); #(1) G! (w[0] . ici(& E634)) 37 (6) # #(0) FD(WE; WE, C:); YO X # (1) Gr(w[2] , ci. b. 1) P7 (b) # (1) Gr(w[3] yw, 3 W, 0) P7 (b) # YOX illosa, fose (10, lt)w, 2032) 60 + de_wibo end module odder Ib. F Gr (Still, web) with, alliness)

1 ms / 1 ms time scale no dule adder - 4 bit (s, co, ci, a, b): [3:0] [3.0] 6; input input ontput \$3:0] 5; (10, d, 12) 17 (1) # YOX : (IN CO : 7W) 77 (1) # YOX (1) FT(S, we, C)) #(1.) GI (WEOZ, Ci, BEOJ); ") 17 (6) # 6 ~0 XOY # (1.) Gr (w[1], ci, b[]]) () () () () () # (1.) Gr (w[2], ci, b[2]); # (1) GE (WE3]; Ci, b[3]); odder_ 1bit Gd (SEO3, WC43, Ci, a EO], b EO]); 69 (SE13, WE 53, WE43, all, blis); adder - 1bit GV (5[2], W[6], W[5], a[]], b[2]); adder _ 16it GN(5[3], Co, WE 6], a[3], b[3]): adder-16it

end module

'time scale I ns/1 ns nodule 16 - adder - 4bit (); reg [3:0] a,b; reg C:; wire [3:0] 8; Chilif & A ... 1 1 - a 1 1 2 4 wire Co; . 18 2 . 13 T1 (S, Co, Ci, a, b); adder - 4 bit 1 知神 : 01000 de com initial b. 4 6 1000: begin az 4'b 1110 ; d 1 . 0 a=4'60001; b = 4'b 0011; OI # b = 4 b 0001; c: 21'60; C: 2 1 60; # 20; #10; 51 26 -n 8 00 az 4'60100; b= 4'b 0001; c; 2 1 b0; #10;

6 no

testberch

a=460001:

b= 4'6000 Z:

C: 161;

#10;

az 4' b 1010 :

bz 4 b 0011;

c:=1'b1;

#10;

az 4 / 60010;

b. 4'b 1000;

C:= 1 61 : 12111 4 + = 10

20; 1100 17 . 8

c. a 1 'bo :

· 4 20;

en d

end module

oz 4 '6 0 100:

12000 a Red

12001, -..

5 \$ 0000 £ A 5 a

: 06 2 - 0

10 ·

100-1 - 10