Design and Analysis of 6T SRAM: Read/Write Operations and SNM Stability

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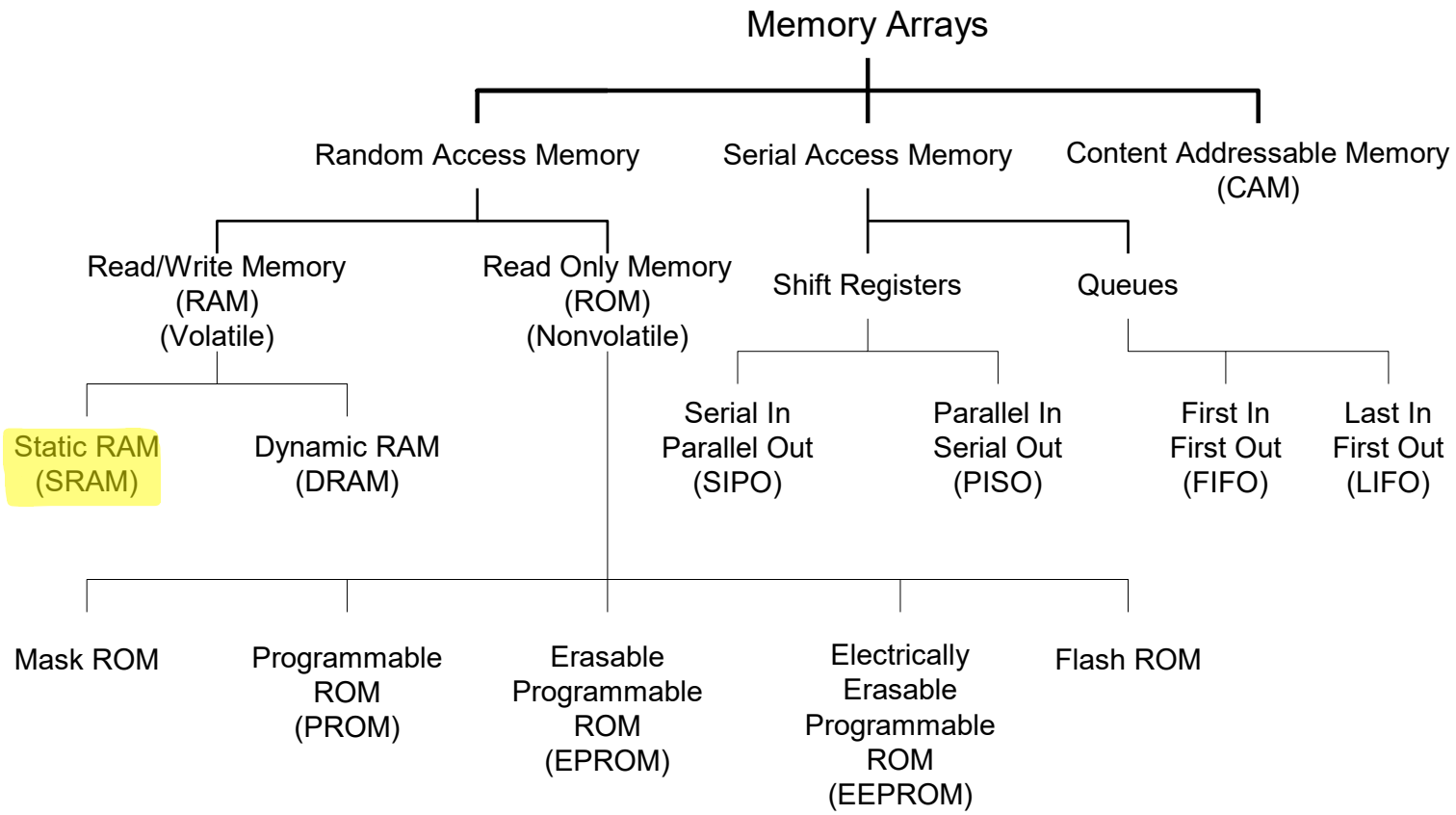
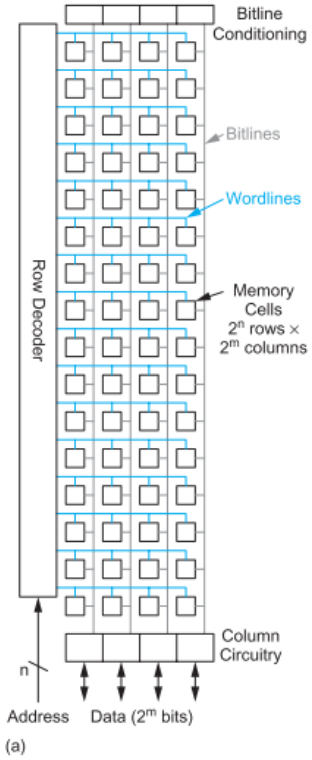
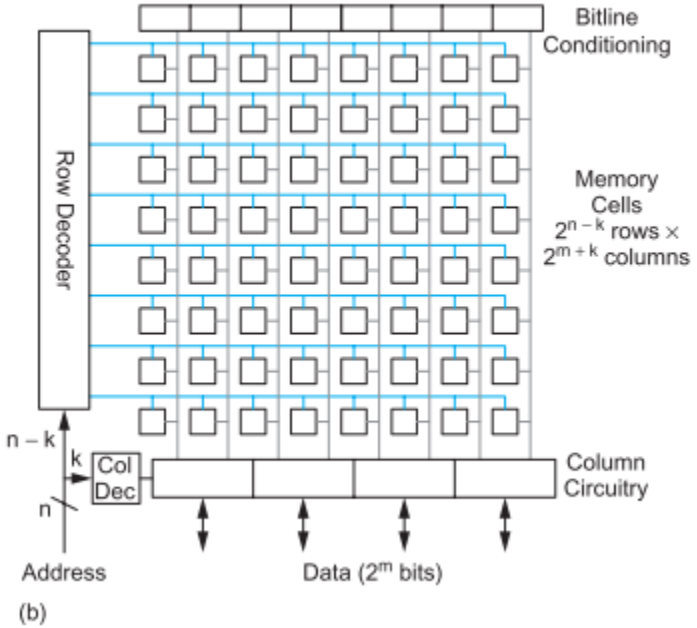
Memory Arrays



Array Architecture

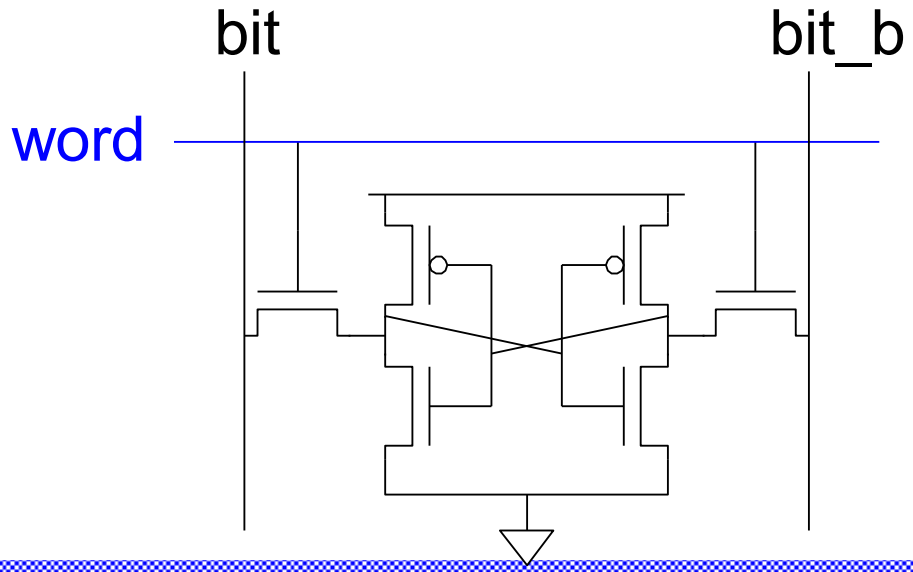
- The row decoder uses the address to activate one of the rows by asserting the wordline
- In a long structure, the address is directly decoded into one row, and that row contains exactly one data word.
- But longer bitlines in a tall structure create high capacitance and resistance, which slows down data transfer and take more power
- This is why array is folded into fewer rows of more columns for a better PPA





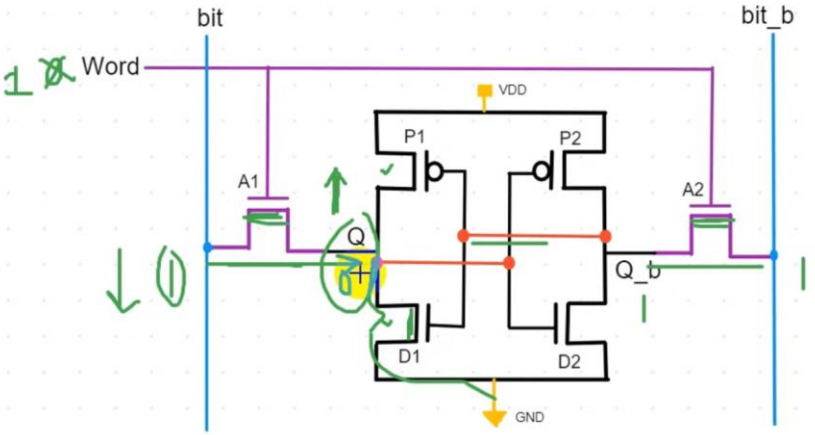
6T SRAM Cell

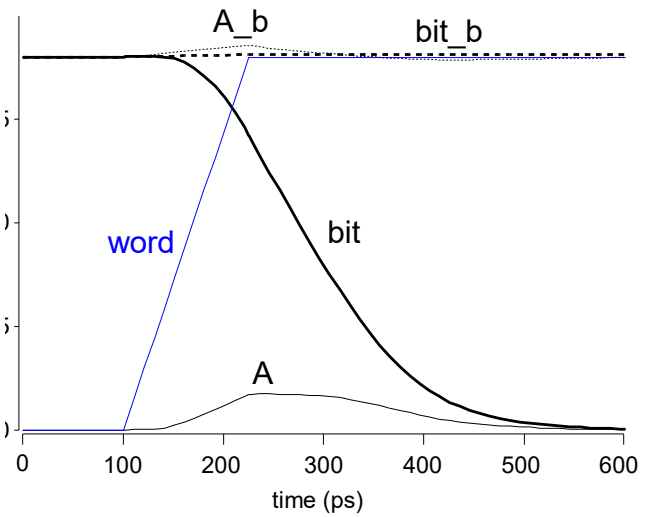
- Cell size accounts for most of array size
  - Reduce cell size at expense of complexity
- 6T SRAM Cell
  - Used in most commercial chips
  - Data stored in cross-coupled inverters
- Able to read/write and hold data as long as power is applied
- Flip-flop might work, but the size is too big for it to be on a chip



SRAM Read 0

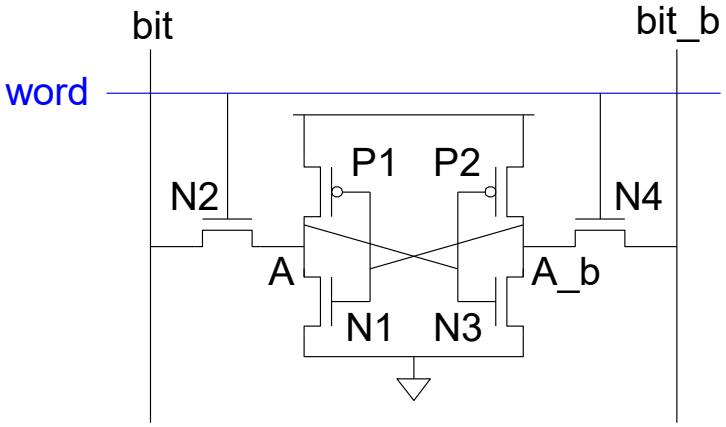
- **Initial Conditions:** The Bit Lines (BL and BL_bar) are pre-charged to **1**. The word line (WL) is activated (**1**), turning on access transistors (A1 and A2).
- **The Data State:** The internal node Q is storing a **0**, while Q_bar is storing a **1**.
- **The Voltage "Fight":** Since BL=1 and Q=0, current flows from the Bit Line toward the node Q.
  - This causes the voltage at node Q to rise slightly.
  - Simultaneously, the driver transistor (D1) is **ON** and fights to pull Q back down to **0**.
- **Stability:** To prevent a "Read Upset" (accidentally changing the memory), the driver transistor D1 must be stronger than the access transistor A1.
- **Outcome:** The small voltage drop on BL is sensed by a sense amplifier, successfully reading the **0** without changing the stored data.

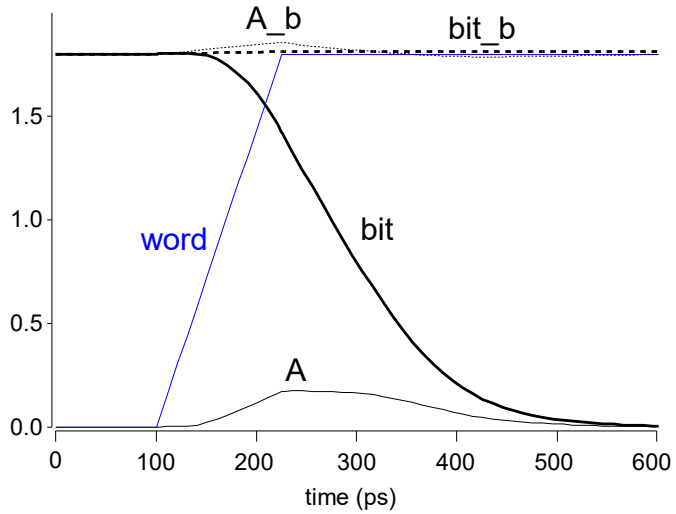




SRAM Read 1

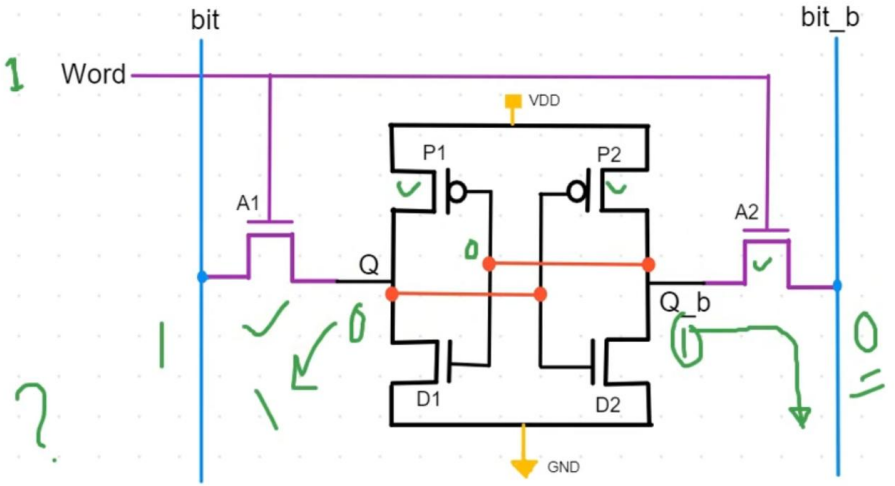
- **Initial Conditions:** The Bit Lines (**BL** and **BL_bar**) are pre-charged to **1**. The word line (**WL**) is activated (**1**), turning on access transistors (**A1** and **A2**).
- **The Data State:** The internal node **Q** is storing a **1**, while **Q_bar** is storing a **0**.
- **The Voltage "Fight":** Since **BL_bar=1** and **Q_bar=0**, current flows from the Bit Line Bar toward the node **Q_bar**.
- This causes the voltage at node **Q_bar** to rise slightly.
- Simultaneously, the driver transistor (**D2**) is **ON** and fights to pull **Q_bar** back down to **0**.
- **Stability:** To prevent a "Read Upset" (accidentally changing the memory), the driver transistor **D2** must be stronger than the access transistor **A2**.
- **Outcome:** The small voltage drop on **BL_bar** is sensed by a sense amplifier, successfully reading the **1** without changing the stored data.

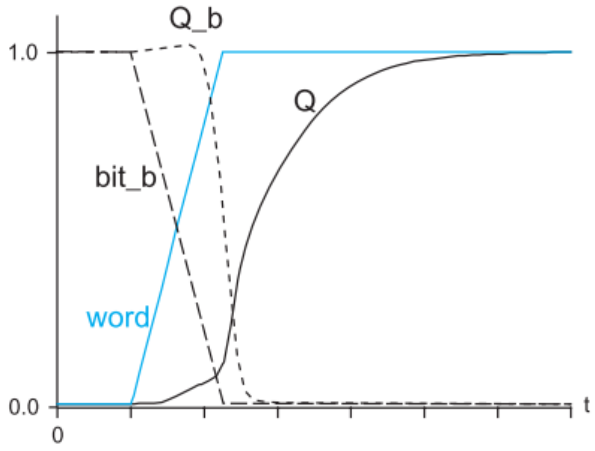




SRAM Write 1

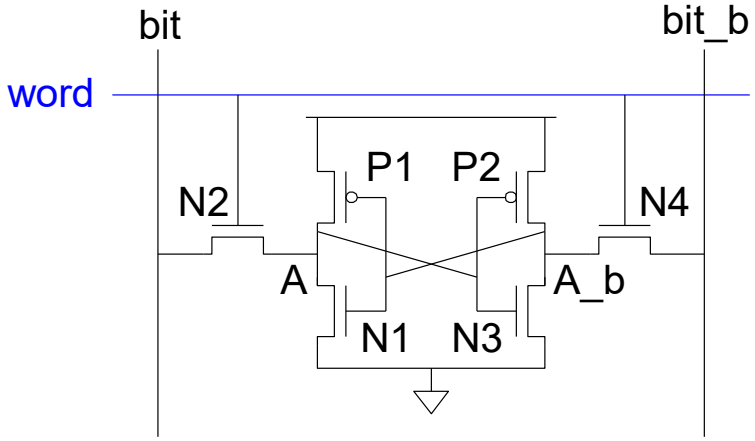
•**Setup:** Bit Line (BL) is driven to **1** and BL-bar is driven to **0**; the Word Line (WL) is then activated.
•**The Overpowering:** The powerful write buffer pulls node **Q-bar** down to **0** through the access transistor.
•**The Feedback Flip:** As Q-bar drops to **0**, the internal feedback loop pulls node **Q** up to **1**, successfully writing the new state.
•**Stability:** To allow the flip, the access transistors must be designed to be stronger than the internal PMOS pull-up transistors.

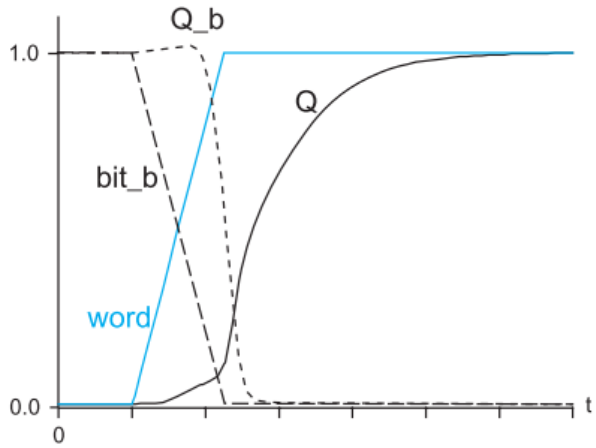




SRAM Write 0

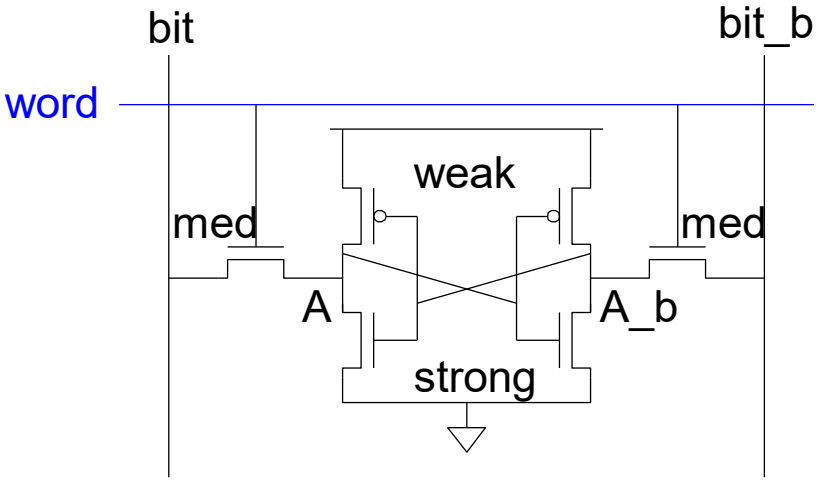
•**Setup:** Bit Line (BL) is driven to **0** and BL-bar is driven to **1**; the Word Line (WL) is then activated.
•**The Overpowering:** The powerful write buffer pulls node Q down to **0** through the access transistor.
•**The Feedback Flip:** As Q drops to **0**, it triggers the internal feedback loop to pull Q-bar up to **1**, permanently flipping the state.
•**Stability:** For a successful write, the access transistors must be stronger than the internal PMOS pull-up transistors.





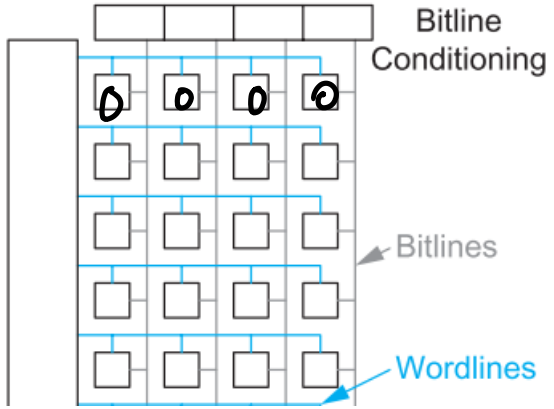
SRAM Sizing

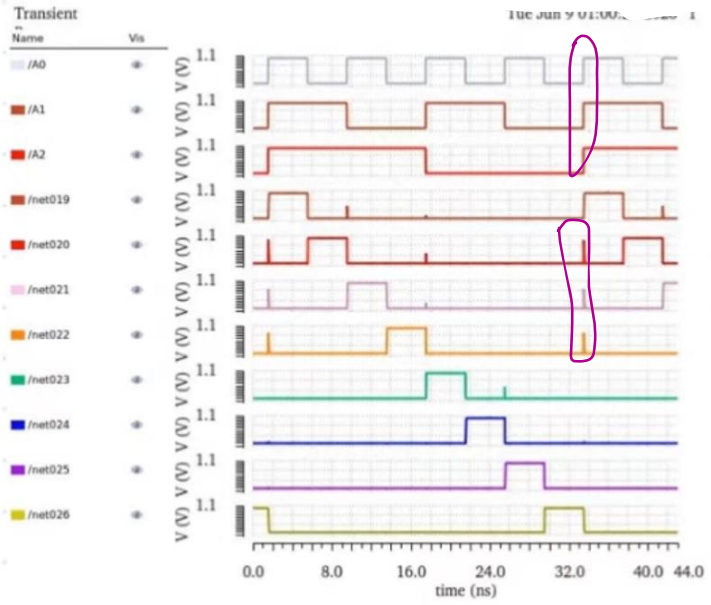
- High bitlines must not overpower inverters during reads
- But low bitlines must write new value into cell



Stability of SRAM

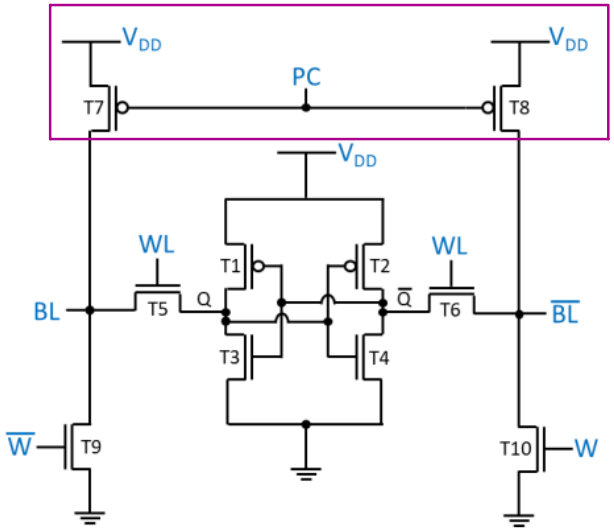
- **Array Logic**: In a memory grid, multiple cells share the same Wordlines and Bitlines.
- **Integrity**: Data stored in a row (e.g., 0000) must remain unchanged during operations on other rows.
- **Stability Violation**: A failure occurs if reading one row accidentally corrupts or overwrites the value in another row.
- **Requirement**: Proper "Ratioing" of all transistors in the array is required to prevent these unintended state changes.

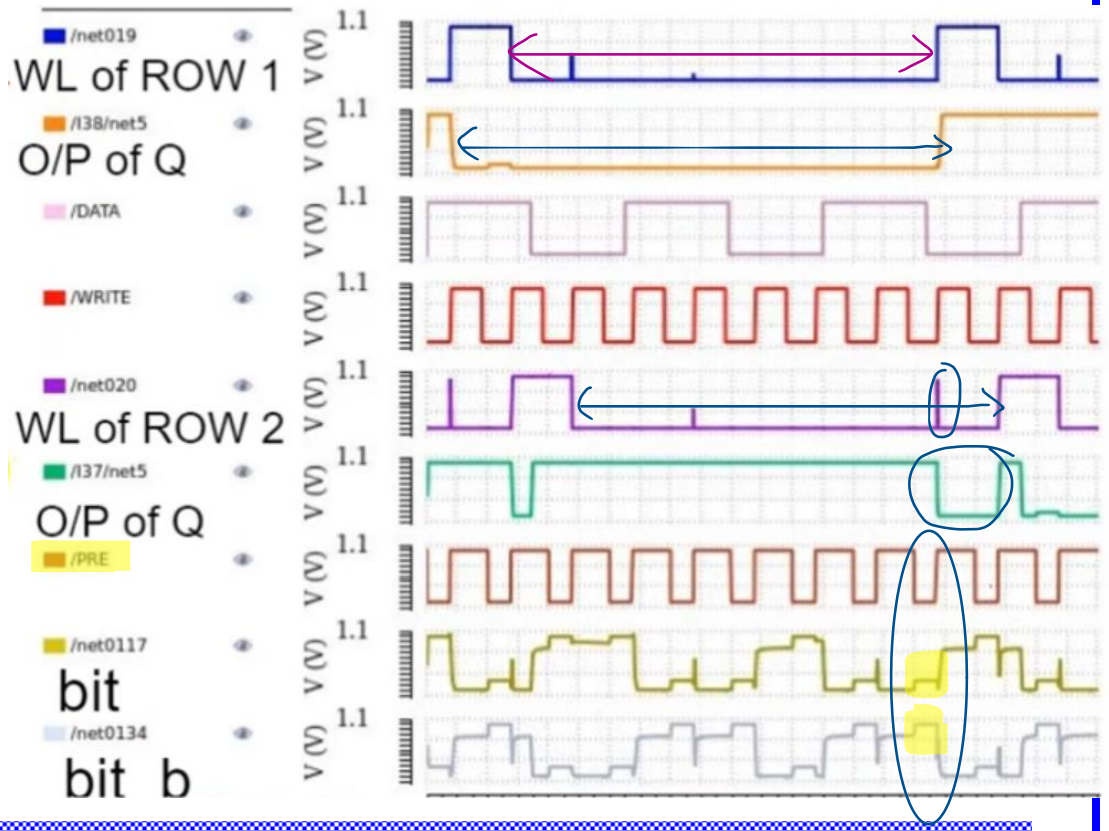




Stability of SRAM

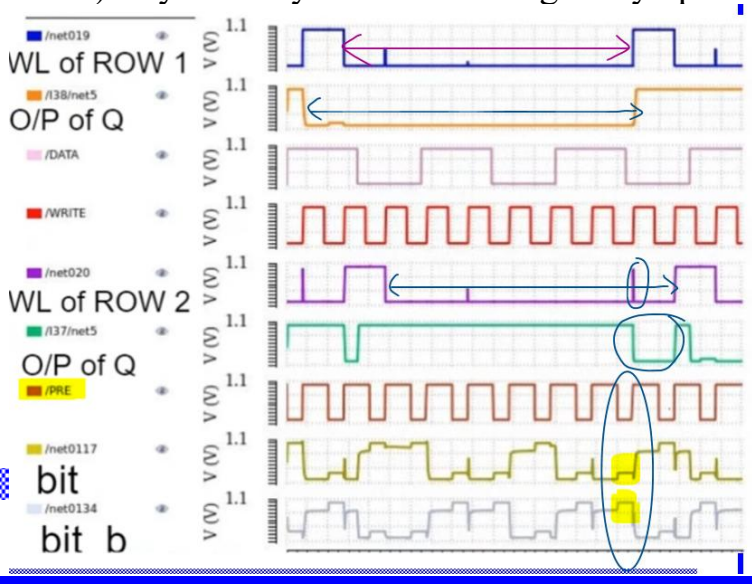
- Use of precharge circuit: the precharge circuit sets both Bit Lines (BL and BL_bar) to a high voltage (usually VDD) before a read or write operation begins.





Stability of SRAM

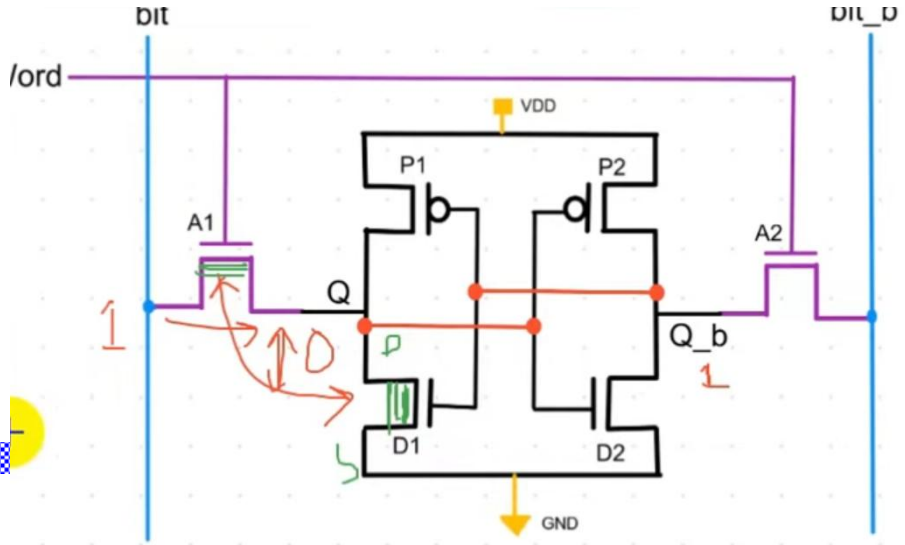
•**Stable Operation (Row 1):** In Row 1, the Word Line (WL) is completely stable and high. Because the internal node Q remains at its correct value throughout the operation, the data is safe and no "Read Upset" occurs.
•**Instability Issue (Row 2):** In Row 2, the Word Line is not stable. This instability causes the internal state (O/P of Q) to suddenly drop or change when it shouldn't, leading to corrupted data.
•**Pre-charge Failure:** Ideally, when the Pre-charge (/PRE) signal is low, both Bit and Bit-bar should be at the same level. However, the diagram shows Bit is High while Bit-bar is Low, proving the internal instability is fighting the pre-charge circuit.
•**The Need for Stability:** This "Violation of Stability" shows that without proper transistor sizing, reading or writing one part of the array can accidentally flip the bits in another row. Stability is required to ensure
•that stored data (like a 0000 row) stays exactly the same during every operation.



Read and Write Stability

- Read Stability (Cell Ratio): To prevent data flip during a read, the Driver (D1) must be stronger than the Access (A1) transistor.
  - Rule $\left(\frac{w}{L}\right)_{D_1} > \left(\frac{w}{L}\right)_{A_1}$
- Write Stability (Pull-up Ratio): To successfully flip the bit, the Access (A1) must be stronger than the internal PMOS (P1).
  - Rule: $\left(\frac{w}{L}\right)_{A_1} > \left(\frac{w}{L}\right)_{P_1}$
- Stability Metric: Hold, Read, and Write margins are defined by the Static Noise Margin (SNM).

$$I_{D,lin} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2]$$



Static Noise Margin (SNM)

•**Definition of SNM:** SNM is the maximum amount of noise voltage that the SRAM cell can tolerate without flipping its stored state.

•**Measurement:** It is graphically represented by the "Butterfly Curve," which is the intersection of the Voltage Transfer Curves (VTC) of the two cross-coupled inverters.

The stability is calculated using the following expression, effectively rotating the coordinate system by 45◦ to find the perpendicular distance between curves:

$$SNM = \frac{1}{\sqrt{2}} \times |V_{\text{out}} - V_{\text{inverted}}|$$

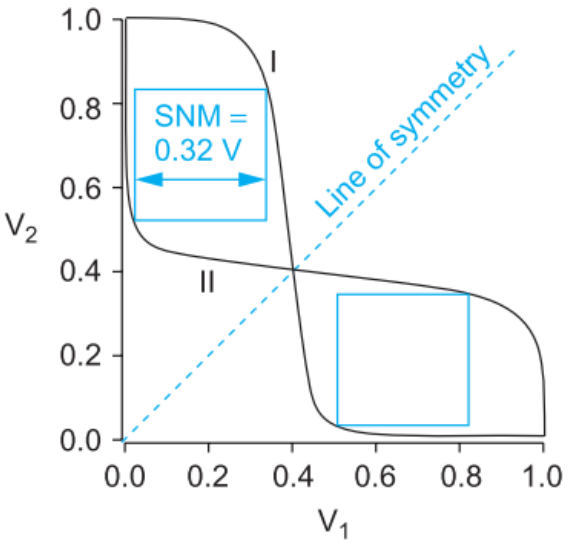


FIGURE 12.9 Butterfly diagram indicating hold margin

- **Stability Visualization:** The two "wings" or loops created show the range of voltages where the cell can safely hold its data. **The SNM Value:** is represented by the side of the **largest square** that can fit inside these loops. In this diagram, the SNM is **0.32 V**, meaning the cell can handle up to that much noise before it accidentally flips its data.
- **Operating Margins:** This specific diagram shows the **Hold Margin**, which measures stability when the cell is at rest. The larger the loops (and the square), the more reliable the memory is during operations like reading or holding data.

Thank You