Do you pashanate know about upcomming Technology?

Now is your hour

RISC V

Lets start now

WHAT IS ISA

Instruction set architecture

An Instruction Set Architecture (ISA) is part of the abstract model of a computer that defines how the CPU is controlled by the software. The ISA acts as an interface between the hardware and the software, specifying both what the processor is capable of doing as well as how it gets done.

The ISA provides the only way through which a user is able to interact with the hardware. It can be viewed as a programmer’s manual because it’s the portion of the machine that’s visible to the assembly language programmer, the compiler writer, and the application programmer.

The ISA defines the supported data types, the registers, how the hardware manages main memory, key features (such as virtual memory), which instructions a microprocessor can execute, and the input/output model of multiple ISA implementations. The ISA can be extended by adding instructions or other capabilities, or by adding support for larger addresses and data values.

Complex Instruction Set Architecture (CISC)

The main idea is that a single instruction will do all loading, evaluating, and storing operations just like a multiplication command will do stuff like loading data, evaluating, and storing it, hence it’s complex.

Characteristics of CISC

Complex instruction, hence complex instruction decoding.

Instructions are larger than one-word size.

Instruction may take more than a single clock cycle to get executed.

Less number of general-purpose registers as operations get performed in memory itself.

Complex Addressing Modes.

More Data types.

Reduced Instruction Set Architecture (RISC)
The main idea behind this is to simplify hardware by using an instruction set composed of a few basic steps for loading, evaluating, and storing operations just like a load command will load data, a store command will store the data.

Characteristics of RISC
Simpler instruction, hence simple instruction decoding.
Instruction comes undersize of one word.
Instruction takes a single clock cycle to get executed.
More general-purpose registers.
Simple Addressing Modes.
Fewer Data types.
A pipeline can be achieved.
Advantages of RISC
Simpler instructions: RISC processors use a smaller set of simple instructions, which makes them easier to decode and execute quickly. This results in faster processing times.
Faster execution: Because RISC processors have a simpler instruction set, they can execute instructions faster than CISC processors.
Lower power consumption: RISC processors consume less power than CISC processors, making them ideal for portable devices.

Digital equipment corporation

Intel ISA : The First ISA develop by the intel corpration

SPARC

MIPS

IBM POWER

ARM

RISC-V Overview

RISC-V is an open standard instruction set architecture (ISA) based on established reduced instruction set computing (RISC) principles. The key features of RISC-V include

Open Standard
Modularity
Scalability
Community-Driven Development

SiFive Overview

SiFive is a company that was founded by the creators of RISC-V to commercialize the ISA. Key points about SiFive include

- IP Cores: SiFive offers IP cores that can be licensed by companies to incorporate RISC-V processors into their own chips.
- RISC-V Processors: SiFive develops and sells a range of processors based on the RISC-V ISA, targeting various applications from embedded systems to high-performance computing.
- Customization: SiFive provides tools and services for customizing RISC-V cores to meet specific requirements, making it easier for companies to develop tailored solutions.
- Ecosystem Development: SiFive actively contributes to the growth of the RISC-V ecosystem, including software development tools, libraries, and hardware platforms.

open-source & proprietary implementations

Field	*Open Standard*	*Free, Open Implement.*	*Proprietary Implement.*
Networking	Ethernet, TCP/IP	*Many*	*Many*
OS	Posix	Linux, FreeBSD	Windows
Compilers	C	gcc, LLVM	Intel icc, ARMcc, Xcode
Databases	SQL	MySQL, PostgresSQL	Oracle 12C, DB2
Graphics	OpenGL	Mesa3D	DirectX
ISA	??????	----------	x86, ARM, IBM360

Why not successful open standards and multiple open-source & proprietary implementations, like other fields?

Generations

In 2010, after many years and many research projects using MIPS, SPARC, and x86, time for architecture group at UC Berkeley to choose ISA for next set of projects

Obvious choices: x86 and ARM

x86 impossible too complex, IP issues

ARM mostly impossible complex, no 64-bit in 2010, IP issues

So we started "3-month project" during summer 2010 to develop clean-slate ISA

Four years later, May 2014, released frozen base user spec

many tapeouts and several research publications along the way

Name RISC-V (pronounced "risk-five") represents fifth major Berkeley RISC ISA

How is RISC-V Avoiding Fragmentation?

RISC-V

Two powerful forces keep fragmentation at bay:

- Users: No one wants a repeat of vendor lock-in.
- Software: No one, not even nation state, can afford their own software stack.

Upstream open-source projects only accept frozen/ratified Foundation standards.

RISC-V Completeness

RISC-V

• Large number of extensions ratified in 2021

Vectors

Full application vectors ("V") + subsets for embedded ("Zve*")

• Hypervisor

supports Type-1 and Type-2

Scalar Crypto

NIST and Shang-Mi cipher suites

Cache Management Operations

Block prefetch, zero, clean/flush/discard

Virtual Memory Enhancements

Larger pages (64KiB), PTE-based memory attributes, faster invalidate

More extensions in flight for 2022 and beyond

IOMMU, Advanced scalable interrupts, vector crypto, FP16, BF16, pointer masking,

Comparing ISA Business Models

ISA	Chips?	Architecture License?	Commercial Core IP?	Add Own Instructions?	Open-Source Core IP?
x86	Yes, ***three*** vendors	***No***	***No***	***No***	***No***
ARM	Yes, ***many*** vendors	Yes, ***expensive***	Yes, ***one*** vendor	***No*** *(Mostly)*	***No***
RISC-V	Yes, ***many*** vendors	Yes, ***free***	Yes, ***many*** vendors	***Yes***	***Yes, many available***

RISC-V: The ISA that likes to say "Yes"

Why is RISC-V so popular?

RISC-V

- Engineers sometimes "don't see forest for the trees"
- The movement is not happening because some benchmark ran

10% faster, or some implementation was 30% lower power (though that might be true)

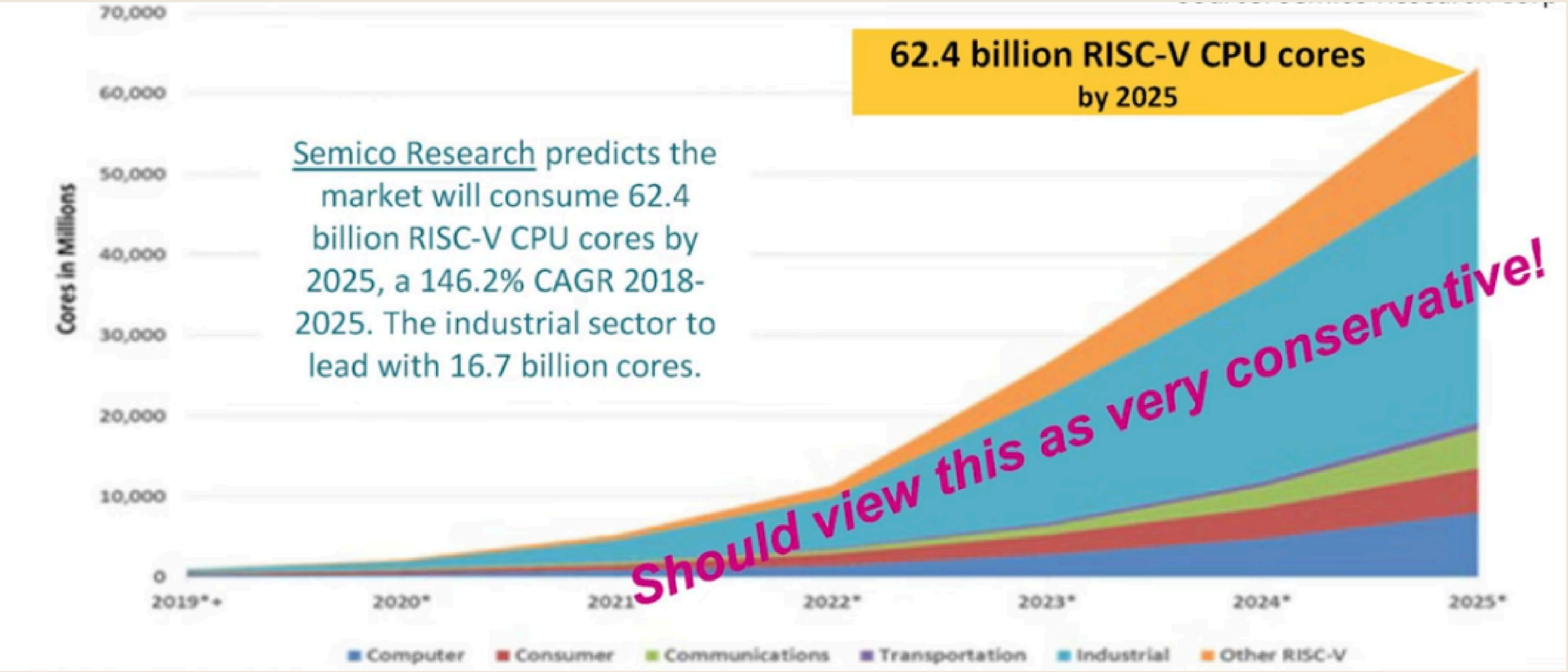
- The movement is happening because new business model changes everything

Pick ISA first, then pick vendor or build own core

Add your own extension without getting permission Commercial, academic, and open-source ecosystems can

coalesce around a single open standard

Rapid RISC-V growth over next five years led by industrial



RISC-V ISA Development Boards and Processors

The RISC-V (Reduced Instruction Set Computing V) ISA (Instruction Set Architecture) has gained significant traction in recent years, with various development boards and processors available for enthusiasts, researchers, and professionals. Here's a look at some of the popular development boards and processors using the RISC-V ISA

RISC-V Ecosystem

Software

Open-source software:
Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, …

Commercial software:
Lauterbach, Segger, IAR, Greenhills WindRiver, Micrium, ExpressLogic, Ashling, Imperas, AntMicro, …

RISC-V International

ISA specification | Golden Model | Compatibilty

Hardware

Open-source cores:
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Swerv, Hummingbird, WARP-V, XiangShan, BlackParrot, …

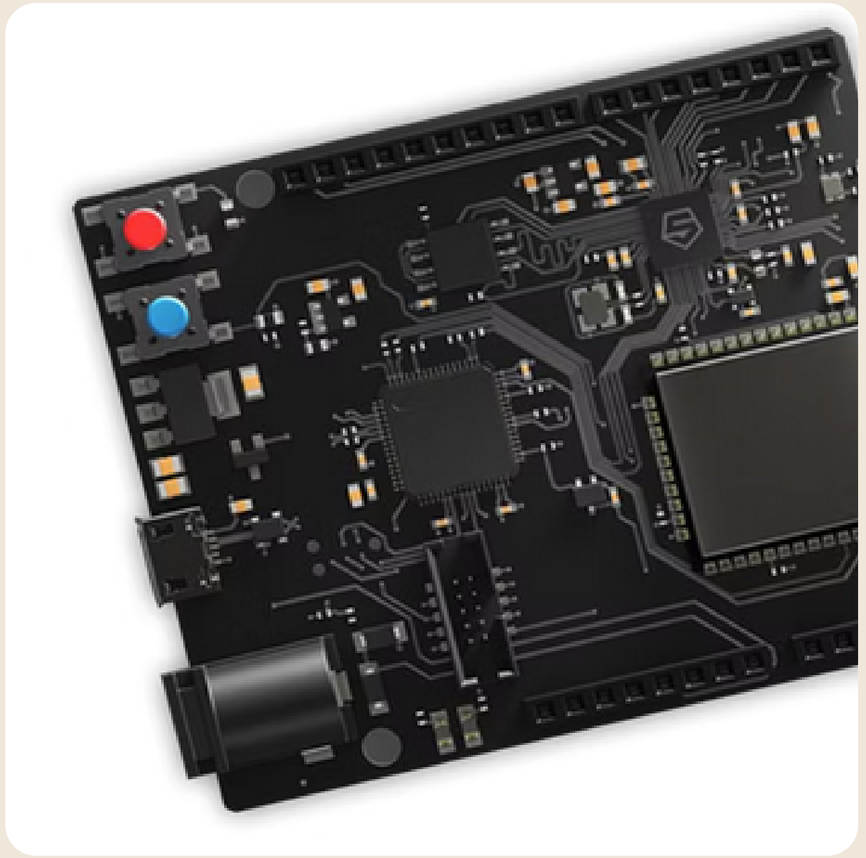
Commercial core providers:
Alibaba, Andes, Bluespec, Cloudbear, Cobham, Codasip, Cortus, Imagination, InCore, MIPS, Nuclei, Semidynamics, **SiFive**, StarFive, Syntacore,

Inhouse cores:
Nvidia, WDC, Seagate Alibaba, +others

Development Boards

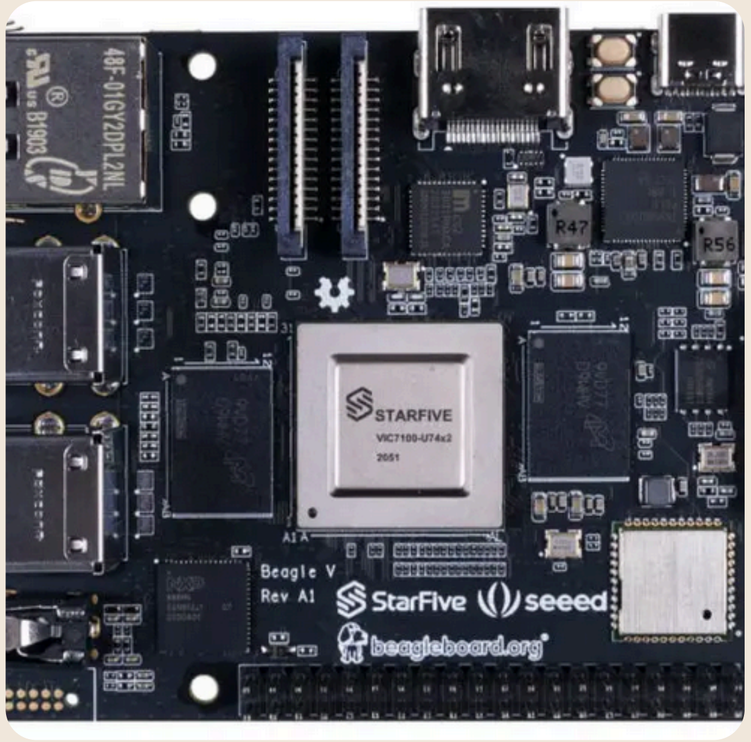
SiFive HiFive Boards

- HiFive1 Rev B: A low-cost development board featuring the SiFive FE310 RISC-V microcontroller, suitable for learning and prototyping.
- HiFive Unleashed: A more advanced board featuring the SiFive Freedom U540 SoC, designed for more complex applications and capable of running a full Linux operating system.



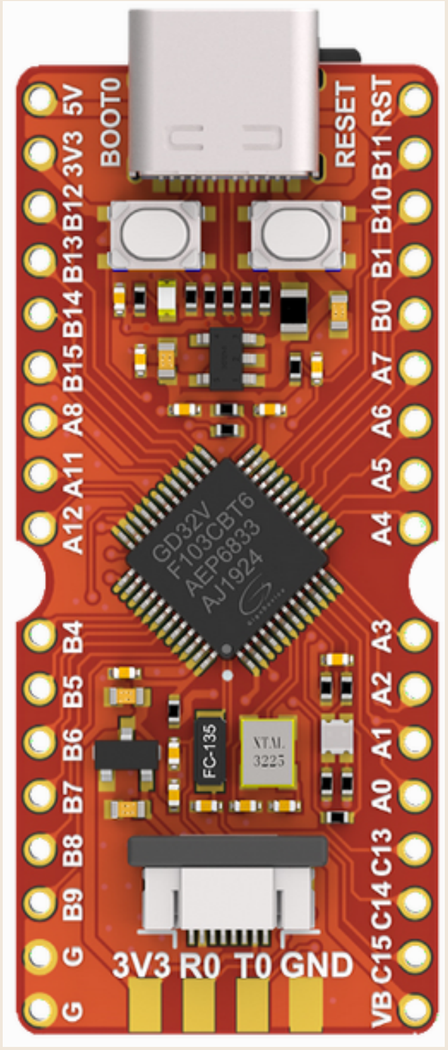
BeagleV

A single-board computer developed by BeagleBoard.org in collaboration with Seeed Studio and SiFive. It features a StarFive JH7100 SoC and is capable of running Linux distributions, providing a platform for both hobbyist projects and serious development.



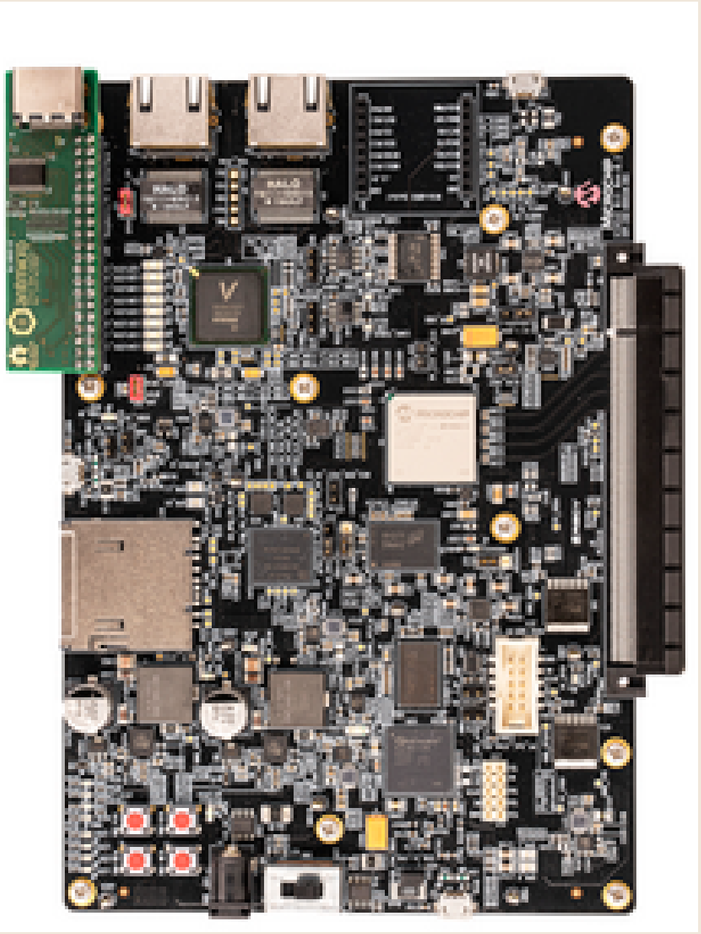
Sipeed Longan Nano

- Longan Nano: A compact and affordable development board featuring the GD32VF103 RISC-V microcontroller. It is well-suited for entry-level embedded systems development.



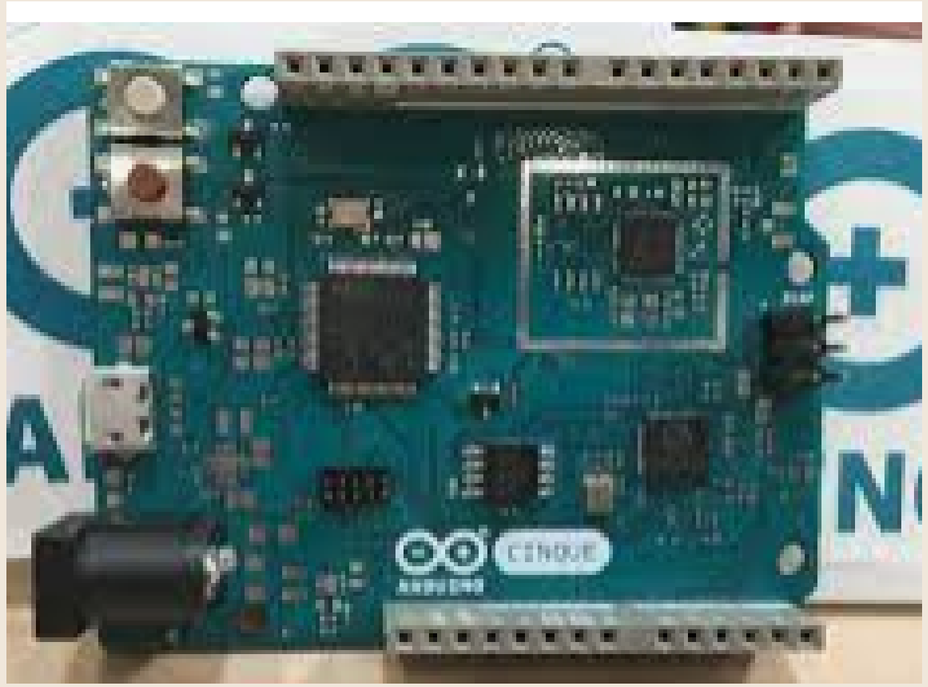
Microchip PolarFire SoC Icicle Kit

- PolarFire SoC Icicle Kit: A versatile development kit featuring the Microchip PolarFire SoC, which combines a RISC-V CPU with FPGA fabric. This board is ideal for exploring heterogeneous computing and custom hardware accelerations.



Arduino Cinque

- A collaboration between Arduino and SiFive, featuring the SiFive FE310 RISC-V microcontroller. It combines the familiar Arduino platform with the RISC-V architecture, making it accessible to a broad audience of makers and developers.



AI/ML Focused Development Boards and Processors RISC-V

SiFive HiFive Unmatched
Processor: SiFive Freedom U740 SoC
Features:

- **Quad-core U74 RISC-V CPUs**
- **Suitable for running full Linux distributions**
- **Expandable with PCIe slots and ample I/O options**

AI/ML Use: While not exclusively designed for AI, its expandability allows for adding GPUs or AI accelerators, making it suitable for AI development and experimentation.
BeagleV (Starlight Development Board)
Processor: StarFive JH7100 SoC
Features:

- **Dual-core SiFive U74 RISC-V CPUs**
- **Vision DSP (Digital Signal Processor) for AI tasks**
- **Capable of running Linux distributions like Fedora**

AI/ML Use: Specifically designed with AI applications in mind, including computer vision and neural network inferencing.
Microchip PolarFire SoC Icicle Kit

Processor: Microchip PolarFire SoC
Features:

- Multi-core RISC-V CPUs combined with FPGA fabric
- Rich set of peripherals and interfaces
- Capable of real-time processing and custom hardware accelerations

AI/ML Use: The FPGA can be programmed to accelerate AI workloads, making it versatile for custom AI solutions.

Sipeed MAIX Series
Processor: Kendryte K210 SoC
Features:
Dual-core 64-bit RISC-V CPUs
Integrated KPU (Kendryte Processing Unit) for neural network inferencing
Vision accelerators for AI tasks
AI/ML Use: Specifically designed for AI applications, including image recognition and audio processing, making it suitable for edge AI applications.

SiFive U74-MC Core Complex
Features:

- Designed for high-performance applications
- Multi-core configuration for parallel processing

AI/ML Use: Provides the processing power needed for AI workloads, and can be integrated with AI accelerators for enhanced performance

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Alibaba T-Head Xuantie C910
Features:

- High-performance RISC-V core
- Support for AI acceleration

AI/ML Use: Developed with AI applications in mind, suitable for data centers and edge computing with AI workloads.

GreenWaves GAP8

Processor: GAP8 IoT Application Processor

Features:

- RISC-V based multi-core processor
- Specialized for low-power AI and IoT applications

AI/ML Use: Optimized for energy-efficient AI processing, making it ideal for battery-operated devices and edge AI.


Thank
you!