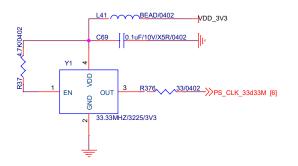
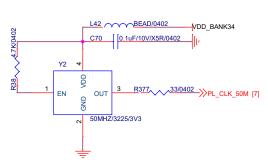
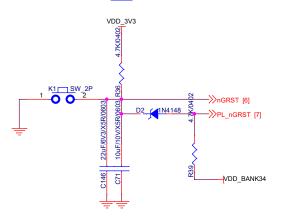


ZYNQ_CLK



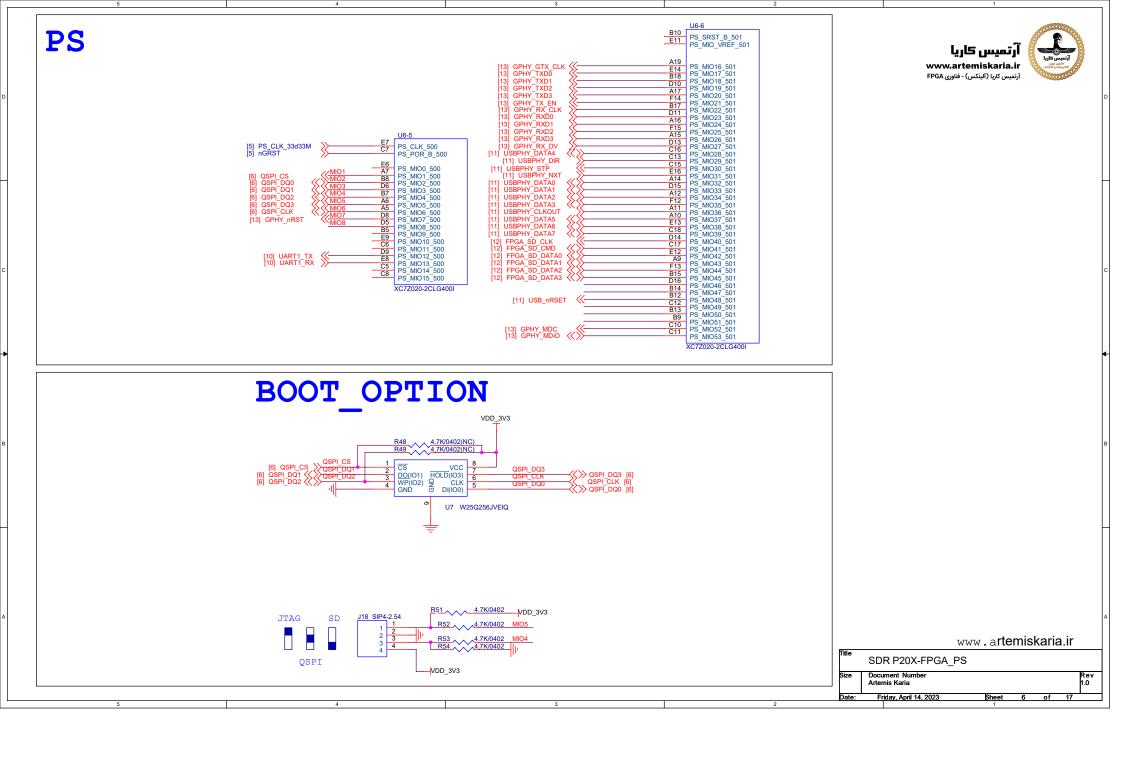


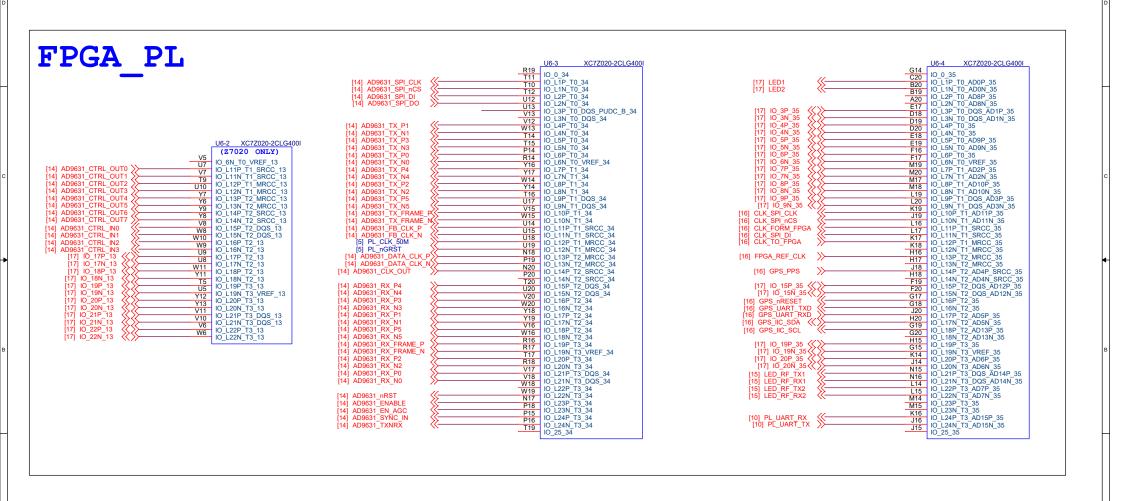
ZYNQ_RST





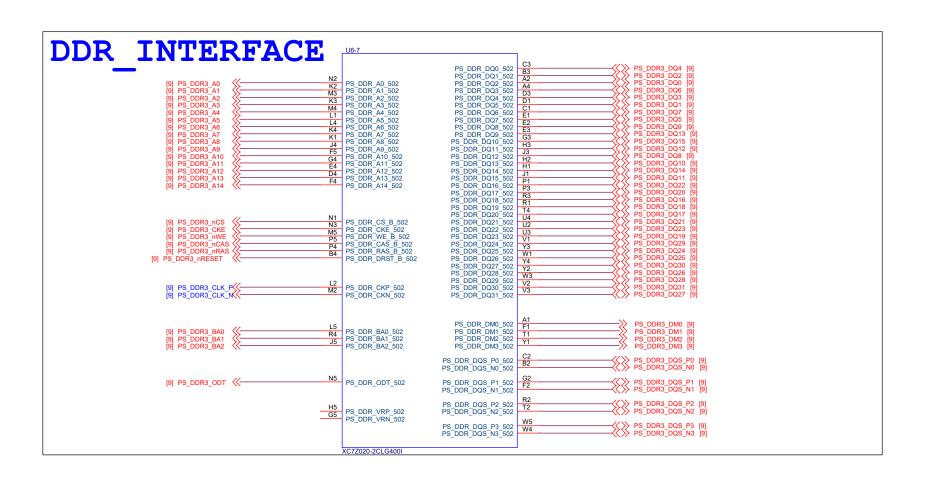
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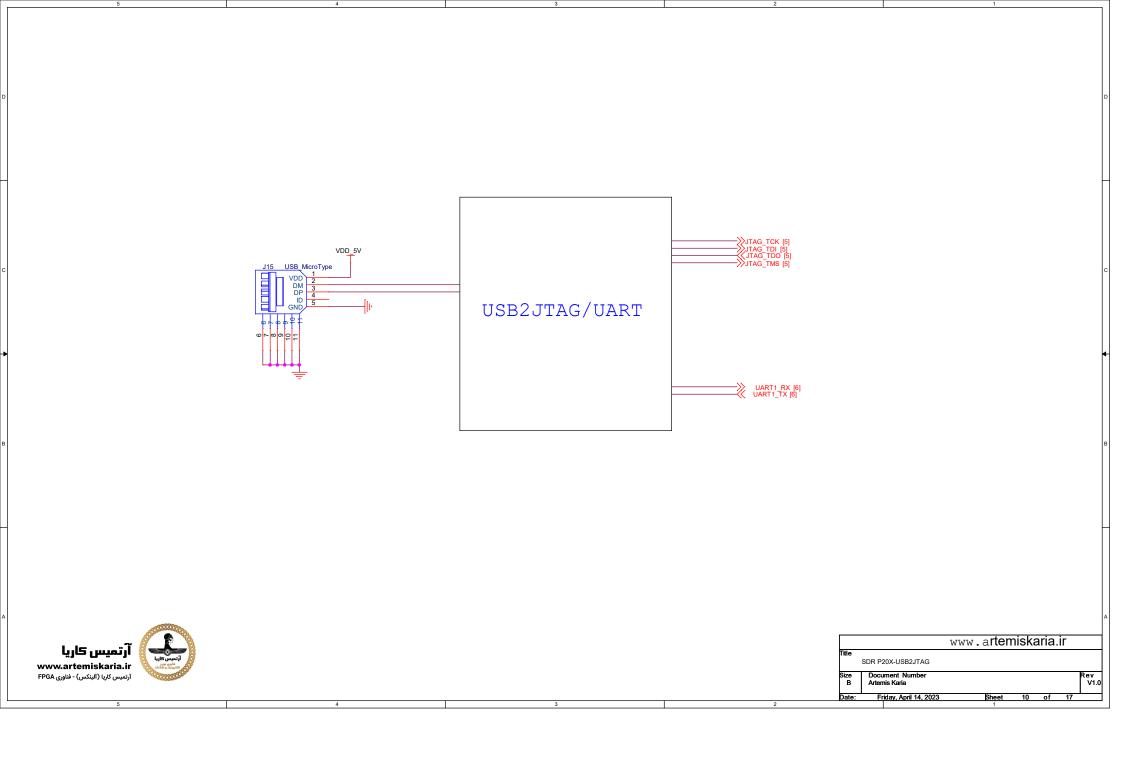


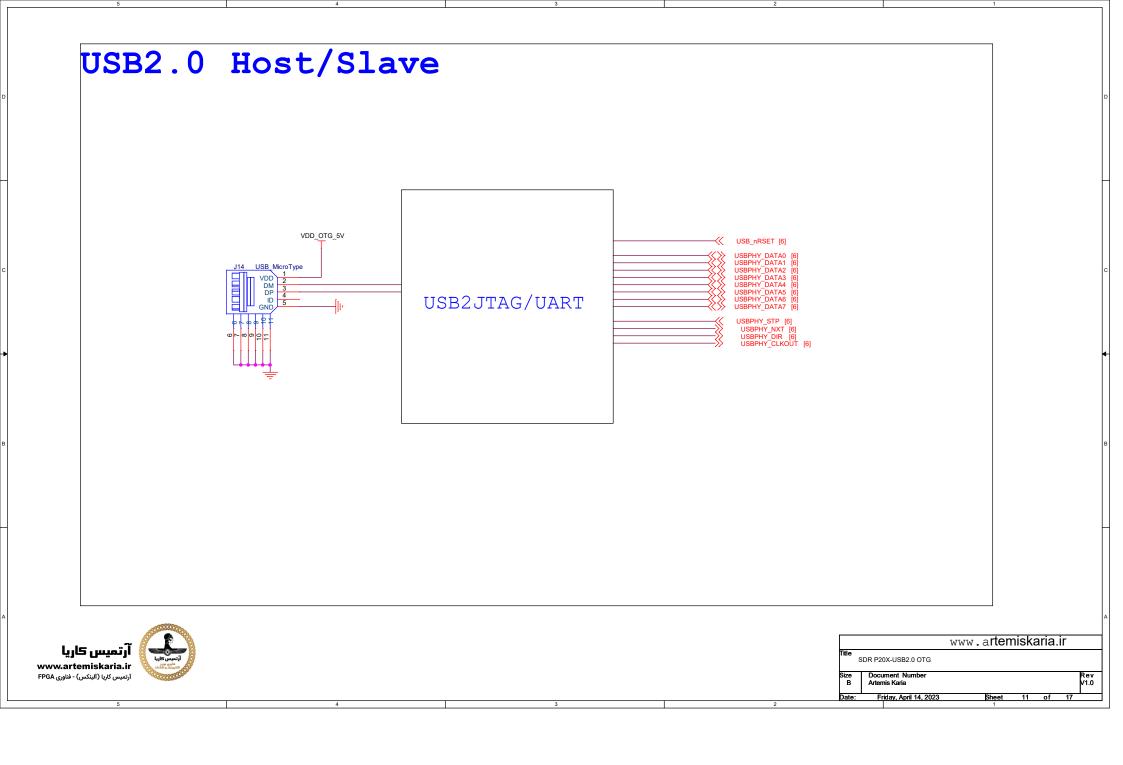
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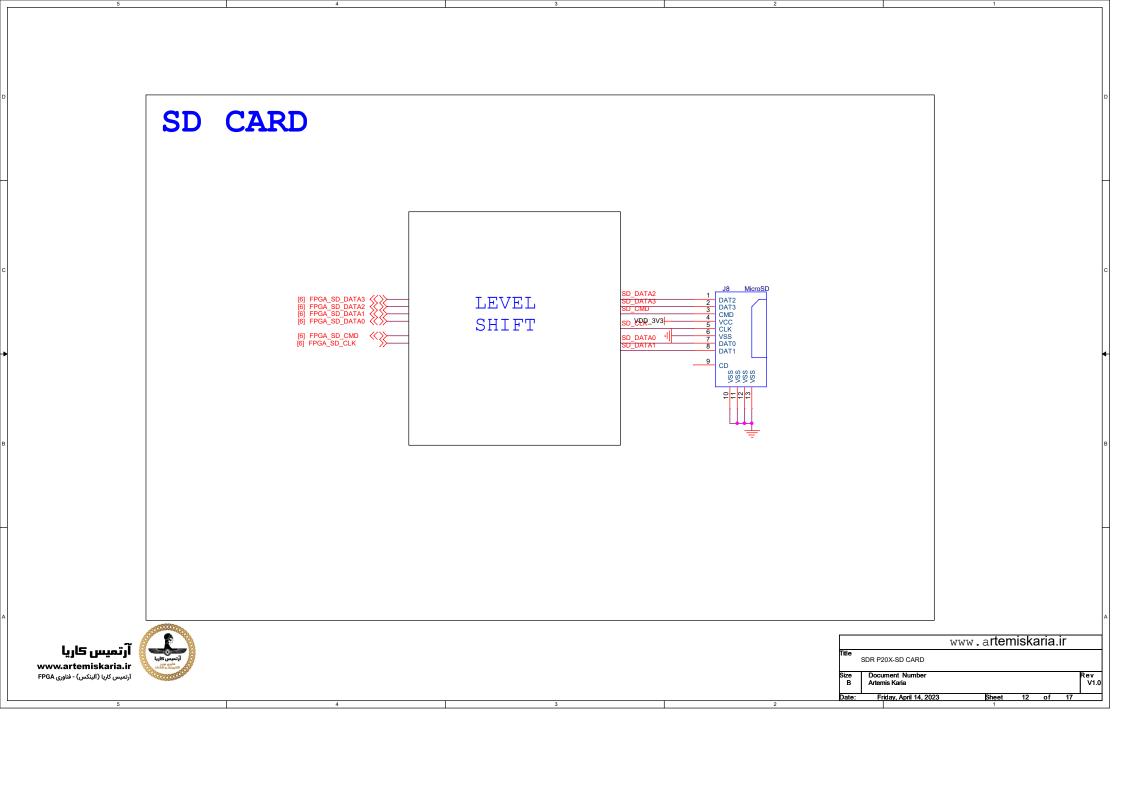
PS DDR3 VDD_1V5 VDD_1V5 U9 U10 B2 VSS J8 VSS A9 VSS M1 B2 VDD VDD D9 G7 K2 D9 G7 K2 K8 VSS A9 VSS M1 VDD VDD VDD VDD VDD VSS M9 VSS B3 VDD VSS M9 K8 N1 N9 R1 B3 P1 P9 E1 T1 N1 N9 R1 B3 P1 VSS VSS VSS VSS VSS VSS VSS VSS VDD VDD VDD VSS VDD VSS P9 VDD VDD R9 R9 VDD VDD VSS VSS VSS T9 G8 G8 VDDQ VDDQ A8 VDDQ C1 VDDQ A8 VDDQ C1 VDDQ C9 VDDQ VDDQ C9 D2 E9 F1 H2 VDDQ D2 E9 F1 VSSQ B9 VSSQ D1 VSSQ B9 VSSQ D1 VDDQ **VDDQ** VDDQ VDDQ VSSQ VSSQ VSSQ VDDQ VDDQ VSSQ D8 E2 E8 F9 H2 D8 VDDO VDDO VSSO E2 E8 F9 H9 H9 VDDQ VDDQ VSSQ VSSQ VSSQ VREFDQ VREFCA VREFDQ VSSQ VSSQ M8 M8 VREFCA VSSQ VSSQ PS_DDR3_A0 PS_DDR3_A1 PS_DDR3_A2 N3 P7 P3 A1 A2 N3 P7 P3 VSSQ VSSQ [8] PS_DDR3_A0 [8] PS_DDR3_A1 [8] PS_DDR3_A2 [8] PS_DDR3_A3 [8] PS_DDR3_A4 Α1 DQ0 F7 DQ1 F2 PS_DDR3_DQ0 [8]
PS_DDR3_DQ1 [8]
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PS_DDR3_DQ17 [8]
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PS_DDR3_A4
PS_DDR3_A5
PS_DDR3_A6 A2 A3 A2 A3 A4 A5 A6 A7 A8 DQ0 DQ1 N2 P8 N2 P8 DQ2 DQ2 F8 H3 P2 R8 PS DDR3 DQ18
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PS_DDR3_DQ8_[8]
PS_DDR3_DQ9_[8] DQ6 DQ6 PS DDR3 A9 DQ6 H7 DQ7 D7 DQ8 C3 DQ9 C8 DQ10 C2 DQ7 DQ8 DQ9 L7 A9 A10 PS DDR3 A10 D7 C3 C8 C2 A7 R7 A10/AP N7 A11 T3 A12/BC_n PS_DDR3_A12 PS_DDR3_A12 DQ10 PS_DDR3_DQ10 [8] PS_DDR3_A13 PS_DDR3_A14 PS_DDR3_DQ10 [6]
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PS_DDR3_DQ31 [8] PS_DDR3_A13 PS_DDR3_A14 A13 DQ11 DQ11 A7 DQ12 DQ13 DQ12 DQ13 A14 A14 A2 B8 J7 PS_DDR3_CLK_P J7 [8] PS_DDR3_CLK_P [8] PS_DDR3_CLK_N [8] PS_DDR3_CKE CLK DQ14 CLK DQ14 A3 A3 CLK_n PS_DDR3_DQ15 [8] CLK_n K9 K9 CKE CKE PS_DDR3_DQS_P0 [8]
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PS_DDR3_DQS_P3 [8]
PS_DDR3_DQS_N3 [8] LDQS PS_DDR3_nCS PS_DDR3_nRESE LDQS G3 G3 CS RESET WE RAS CAS CS RESET WE RAS CAS [8] PS_DDR3_nCS LDQSn LDQSn PS DDR3 nRESE T2 L3 T2 L3 [8] PS_DDR3_nRESET >> PS_DDR3_nWE UDQS UDQS [8] PS_DDR3_nWE [8] PS_DDR3_nRAS **UDQSn UDQSn** J3 K3 J3 K3 PS_DDR3_nRAS M2 PS DDR3 BA0 M2 NC1 J1 X NC2 L1 X NC3 L9 X NC4 M7 X [8] PS_DDR3_BA0 BA0 NC1 J9 X NC2 L1 X NC3 L9 X NC4 M7 X BA0 N8 M3 N8 M3 [8] PS_DDR3_BA1 [8] PS_DDR3_BA2 BA1 BA1 PS DDR3 BA2 BA2 BA2 PS DDR3 DM2 E7 E7 [8] PS_DDR3_DM0 [8] PS_DDR3_DM1 LDM I81 PS DDR3 DM2 LDM NC5 NC5 PS_DDR3_DM3 D3 D3 UDM [8] PS DDR3 DM3 UDM PS_DDR3_ODT K1 K1 L8 L8 [8] PS_DDR3_ODT ODT ZQ ODT ZQ MT41K256M16TW-107IT:P MT41K256M16TW-107IT:P www.artemiskaria.ir

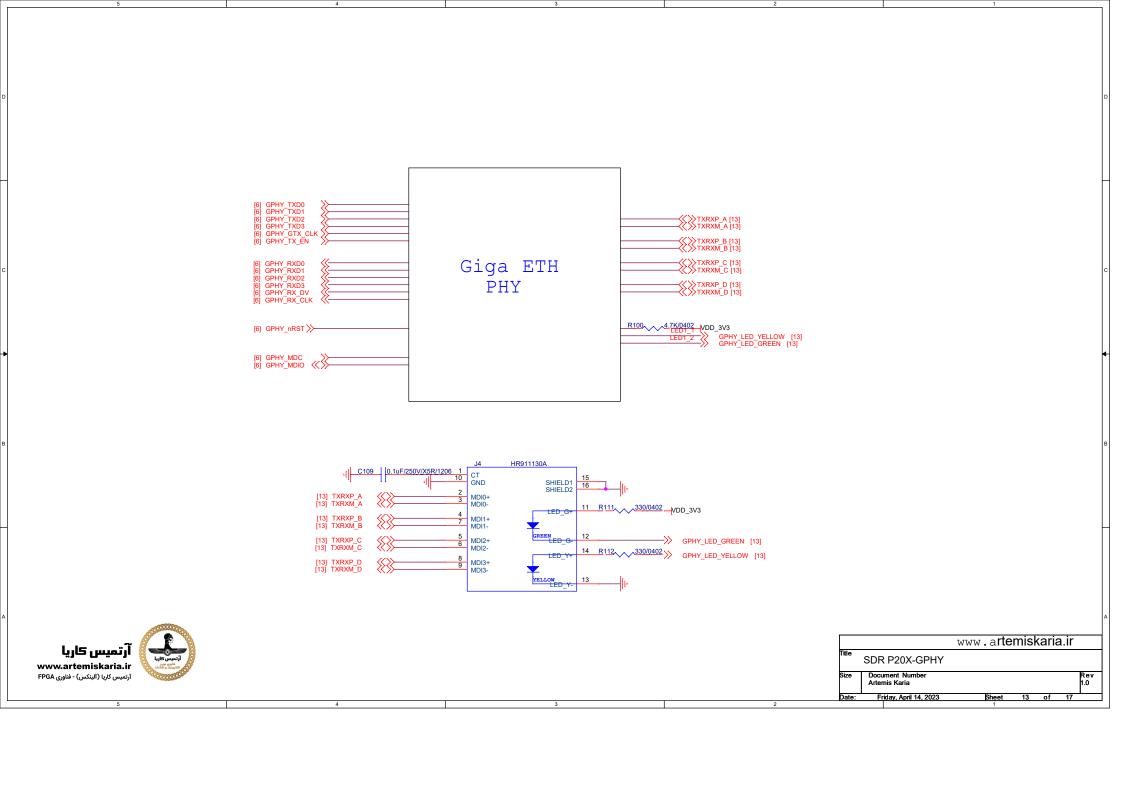


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TX_MON2 [7] AD9631_CLK_OUT CLK_OUT J5
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SPI_ENB
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SPI_DO [7] AD9631_SPI_CLK [7] AD9631_SPI_nCS [7] AD9631_SPI_DI AUXDAC1 B3 [7] AD9631 SPI DO [7] AD9631_nRST >> RESETR AUXDAC2 G6 ENABLE AUXADC L5 [7] AD9631_ENABLE >> C4 TEST/ENABLE TX_VCO_LDO_OUT B11 VDDA1P1_TX_VCO A11 G5 EN_AGC [7] AD9631_EN_AGC >>-H5 SYNC_IN RX_VCO_LDO_OUT G3
VDDA1P1_RX_VCO [7] AD9631_SYNC_IN >>-[7] AD9631_TXNRX >> TXNRX TX_EXT_LO_IN A12 L4 RBIAS RX_EXT_LO_IN G1 D4 | CTRL_OUT0 | CTRL_OUT1 | CTRL_OUT2 | CTRL_OUT3 | C [7] AD9631_CTRL_OUT0[7] AD9631_CTRL_OUT1[7] AD9631_CTRL_OUT2[7] AD9631_CTRL_OUT3 F6 CTRL_OUTS
F5 CTRL_OUT4
CTRL_OUT5
CTRL_OUT6
CTRL_OUT7 77 AD9631 CTRL OUT3 77 AD9631 CTRL OUT4 77 AD9631 CTRL OUT5 77 AD9631 CTRL OUT6 78 AD9631 CTRL OUT7 A3 NC1 C5 C6 CTRL_IN0 CTRL_IN1 CTRL_IN2 CTRL_IN3 М3 [7] AD9631_CTRL_IN0 [7] AD9631_CTRL_IN1 [7] AD9631_CTRL_IN2 [7] AD9631_CTRL_IN3 NC2 B7 B6 B5 B4 GPO_1 GPO_2 GPO_3 GPO_3 M11 XTALP M12 V SSD [16] AD9631_REF_CLK >> XTALN www.artemiskaria.ir SDR P20X-AD9361 Document Numbe Rev V1.0 Artemis Karia Friday, April 14, 202

