MCP4706/4716/4726

8-/10-/12-Bit Voltage Output Digital-to-Analog Converter with EEPROM and I²C™ Interface

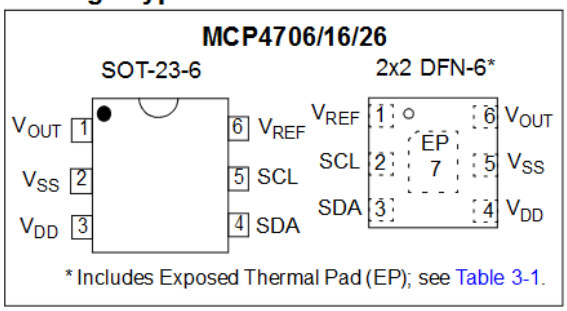
Features:

- Output Voltage Resolutions:
  - 12-bit: **MCP4726**
  - 10-bit: **MCP4716**
  - 8-bit: **MCP4706**
- Rail-to-Rail Output
- Fast Settling Time of 6 µs (typical)
- DAC Voltage Reference Options:
  - V_{DD}
  - V_{REF} Pin
- Output Gain Options:
  - Unity (1x)
  - 2x, only when V_{REF} pin is used as voltage source
- Nonvolatile Memory (EEPROM):
  - Auto Recall of Saved DAC register setting
  - Auto Recall of Saved Device Configuration (Voltage Reference, Gain, Power-Down)
- Power-Down modes:
  - Disconnects output buffer
  - Selection of V_{OUT} pull-down resistors (640 kΩ, 125 kΩ, or 1 kΩ)
- Low-Power Consumption:
  - Normal Operation: 210 µA typical
  - Power-Down Operation: 60 nA typical (PD1:PD0 = 11)
- Single-Supply Operation: 2.7V to 5.5V
- I²C™ Interface:
  - Eight Available Addresses
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (3.4 Mbps) modes
- Small 6-lead SOT-23 and DFN (2x2) Packages
- Extended Temperature Range: -40°C to +125°C

Applications:

- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems
- Motor Control

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Description:

The MCP4706/4716/4726 are single channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with nonvolatile memory and an I²C serial interface. This family will also be referred to as MCP47X6.

The V_{REF} pin or the device V_{DD} can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is connected internally to the DAC reference circuit. When the V_{REF} pin is used, the user can select the output buffer's gain to 1 or 2. When the gain is 2, the V_{REF} pin voltage should be limited to a maximum of $V_{DD}/2$.

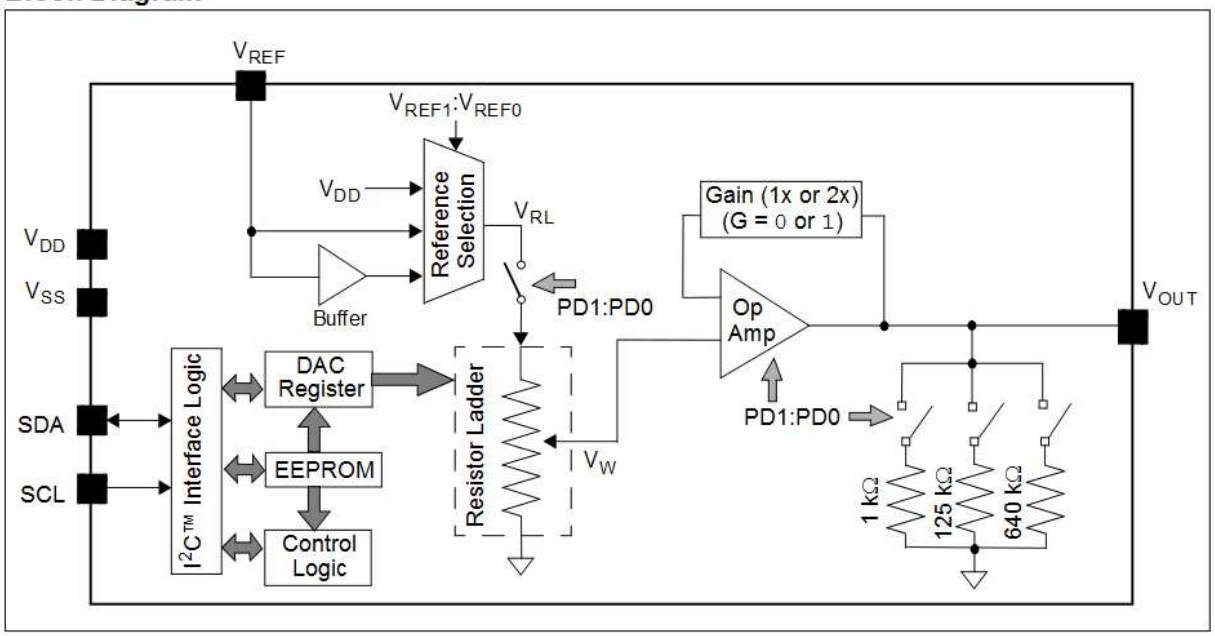
The DAC register value and Configuration bits can be programmed to nonvolatile memory (EEPROM). The nonvolatile memory holds the DAC register and Configuration bit values when the device is powered off. A device Reset (such as a Power-on Reset) latches these stored values into the volatile memory.

Power-Down modes enable system current reduction when the DAC output voltage is not required. The V_{OUT} pin can be configured to present a low, medium, or high resistance load.

These devices have a two-wire I²C™ compatible serial interface for standard (100 kHz), fast (400 kHz), or High-Speed (3.4 MHz) mode.

These devices are available in small 6-pin SOT-23 and DFN 2x2 mm packages.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +6.5V
Voltage on all pins with respect to V_{SS} .....-0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} (V_I < 0, V_I > V_{DD}) .....±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .....±20 mA
Maximum input current source/sunk by SDA, SCL pins .....2 mA
Maximum output current sunk by SDA Output pin .....25 mA
Maximum current out of V_{SS} pin .....50 mA
Maximum current into V_{DD} pin .....50 mA
Maximum current sourced by the V_{OUT} pin .....40 mA
Maximum current sunk by the V_{OUT} pin.....40 mA
Maximum current sunk by the V_{REF} pin .....40 µA
Package power dissipation (T_A = +50°C, T_J = +150°C)
SOT-23-6.....452 mW
DFN-6.....1098 mW
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied .....-55°C to +125°C
ESD protection on all pins.....≥ 6 kV (HBM)
.....≥ 400V (MM)
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF, T_A = -40°C to +125°C. Typical values at +25°C.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Power Requirements						
Input Voltage	V_{DD}	2.7	—	5.5	V	
Input Current	I_{DD}	—	210	400	µA	V_{REF1}:V_{REF0} = 00, SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 0x000
		—	210	400	µA	V_{REF1}:V_{REF0} = 11, V_{REF} = V_{DD}, SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 0x000
Power-Down Current	I_{DDP}	—	0.09	2	µA	PD1:PD0 = 01 (**Note 6**), V_{OUT} not connected
Power-On Reset Threshold	V_{POR}	—	2.2	—	V	RAM retention voltage, (V_{RAM}) < V_{POR}
Power-Up Ramp Rate	V_{RAMP}	1	—	—	V/S	**(Note 1, Note 4)**
DC Accuracy						
Offset Error	V_{OS}		±0.02	0.75	% of FSR	Code = 0x000h V_{REF1}:V_{REF0} = 00, G = 0
Offset Error Temperature Coefficient	V_{OS}/°C	—	±1	—	ppm/°C	-40°C to +25°C
		—	±2	—	ppm/°C	+25°C to +85°C
Zero-Scale Error	E_{ZS}	—	0.13	2.0	LSb	**MCP4706**, Code = 0x00h
		—	0.52	7.7	LSb	**MCP4716**, Code = 0x000h
		—	2.05	30.8	LSb	**MCP4726**, Code = 0x000h
Full-Scale Error	E_{FS}	—	0.3	5.2	LSb	**MCP4706**, Code = 0xFFh
		—	1.1	20.5	LSb	**MCP4716**, Code = 0x3FFh
		—	4.1	82.0	LSb	**MCP4726**, Code = 0xFFFh
Gain Error **(Note 2)**	g_E	-2	-0.10	2	% of FSR	**MCP4706**, Code = 0xFFh V_{REF1}:V_{REF0} = 00, G = 0
		-2	-0.10	2	% of FSR	**MCP4716**, Code = 0x3FFh V_{REF1}:V_{REF0} = 00, G = 0
		-2	-0.10	2	% of FSR	**MCP4726**, Code = 0xFFFh V_{REF1}:V_{REF0} = 00, G = 0
Gain Error Drift	ΔG/°C	—	-3	—	ppm/°C	
Resolution	n		8		bits	**MCP4706**
			10		bits	**MCP4716**
			12		bits	**MCP4726**
INL Error **(Note 7)**	INL	-0.907	±0.125	+0.907	LSb	**MCP4706** (codes: 6 to 250)
		-3.625	±0.5	+3.625	LSb	**MCP4716** (codes: 25 to 1000)
		-14.5	±2	+14.5	LSb	**MCP4726** (codes: 100 to 4000)
DNL Error **(Note 7)**	DNL	-0.05	±0.0125	+0.05	LSb	**MCP4706** (codes: 6 to 250)
		-0.188	±0.05	+0.188	LSb	**MCP4716** (codes: 25 to 1000)
		-0.75	±0.2	+0.75	LSb	**MCP4726** (codes: 100 to 4000)

Note 1: This parameter is ensured by design and is not 100% tested.
2: This Gain error does not include Offset error. See **Section 1.0 "Electrical Characteristics"** for more details in plots.
3: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
4: The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_{DD} over time.
5: This parameter is ensured by characterization, and not 100% tested.
6: The PD1:PD0 = 10, and '11' configurations should have the same current.
7: V_{DD} = V_{REF} = 5.5V.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, RL = 5 kΩ from V_{OUT} to GND, C_L = 100 pF, T_A = -40°C to +125°C. Typical values at +25°C.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	Output Amplifier's minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.04	—	V	Output Amplifier's maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	7	15	24	mA	
Settling Time	$t_{SETTLING}$	—	6	—	µs	Note 3
Power-Down Output Disable Time Delay	T_{PDD}	—	1	—	µs	PD1:PD0 = 00 -> 11, '10', or '01' started from falling edge SCL at end of ACK bit. V_{OUT} = V_{OUT} - 10 mV. V_{OUT} not connected.
Power-Down Output Enable Time Delay	T_{PDE}	—	10.5	—	µs	PD1:PD0 = 11, '10', or '01' -> "00" started from falling edge SCL at end of ACK bit. Volatile DAC Register = FFh, V_{OUT} = 10 mV. V_{OUT} not connected.
External Reference (V_{REF}) (Note 1)						
Input Range	V_{REF}	0.04	—	V_{DD} - 0.04	V	Buffered mode
		0	—	V_{DD}	V	Unbuffered mode
Input Impedance	R_{VREF}	—	210	—	kΩ	Unbuffered mode
Input Capacitance	C_REF	—	29	—	pF	Unbuffered mode
-3 dB Bandwidth		—	86.5	—	kHz	V_{REF} = 2.048V ± 0.1V, V_{REF1}:V_{REF0} = 10, G = 0
		—	67.7	—	kHz	V_{REF} = 2.048V ± 0.1V, V_{REF1}:V_{REF0} = 10, G = 1
Total Harmonic Distortion	THD	—	-73	—	dB	V_{REF} = 2.048V ± 0.1V, V_{REF1}:V_{REF0} = 10, G = 0, Frequency = 1 kHz
Dynamic Performance (Note 1)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (800h to 7FFh)
Digital Feedthrough		—	<10	—	nV-s	

Note 1: This parameter is ensured by design and is not 100% tested.
2: This Gain error does not include Offset error. See **Section 1.0 "Electrical Characteristics"** for more details in plots.
3: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
4: The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_{DD} over time.
5: This parameter is ensured by characterization, and not 100% tested.
6: The PD1:PD0 = 10, and '11' configurations should have the same current.
7: V_{DD} = V_{REF} = 5.5V.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF, T_A = -40°C to +125°C. Typical values at +25°C.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Digital Interface						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	$0.7V_{DD}$	—	—	V	
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	$0.3V_{DD}$	V	
Input Leakage	I_{LI}	—	—	±1	µA	SCL = SDA = V_{SS} or SCL = SDA = V_{DD}
Pin Capacitance	C_{PIN}	—	—	3	pF	**(Note 5)**
EEPROM						
EEPROM Write Time	T_{WRITE}	—	25	50	ms	
Data Retention		—	200	—	Years	At +25°C, **(Note 1)**
Endurance		1	—	—	Million Cycles	At +25°C, **(Note 1)**

Note 1: This parameter is ensured by design and is not 100% tested.
2: This Gain error does not include Offset error. See **Section 1.0 "Electrical Characteristics"** for more details in plots.
3: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
4: The power-up ramp rate affects on uploading the EEPROM contents to the DAC register. It measures the rise of V_{DD} over time.
5: This parameter is ensured by characterization, and not 100% tested.
6: The PD1:PD0 = `10`, and '`11`' configurations should have the same current.
7: V_{DD} = V_{REF} = 5.5V.

1.1 I²C Mode Timing Waveforms and Requirements

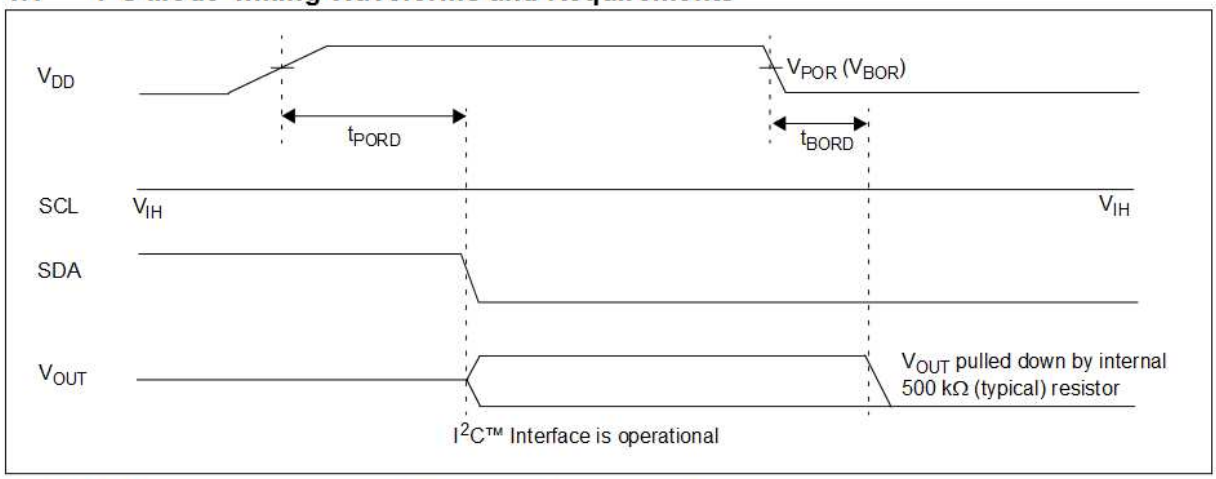


FIGURE 1-1: *Power-On and Brown-Out Reset Waveforms.*

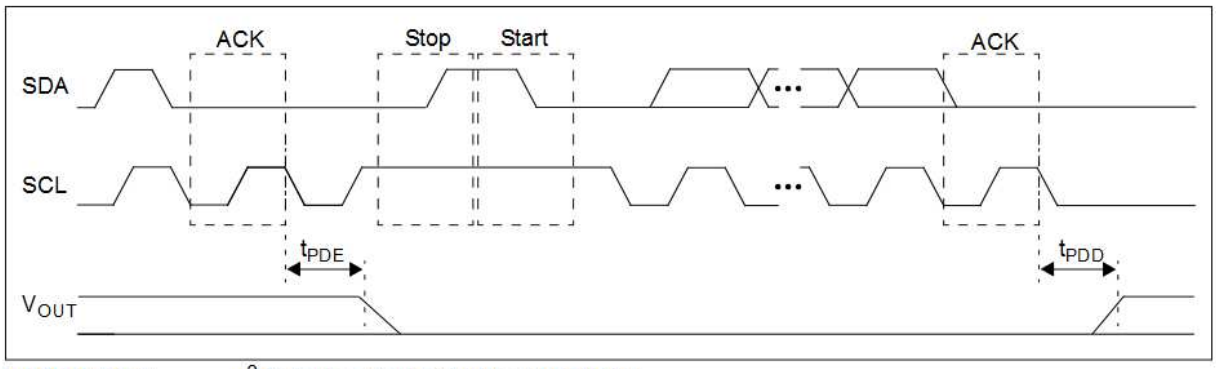


FIGURE 1-2: *I²C Power-Down Command Timing.*

TABLE 1-1: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Power-Up Reset Delay	t_{PORD}	—	60	—	µs	Monitor ACK bit response to ensure device responds to command.
Brown-Out Reset Delay	t_{BORD}	—	1	—	µs	V_{DD} transitions from $V_{DD(MIN)}$ → > V_{POR} V_{OUT} driven to V_{OUT} disabled
Power-Down Disable Time Delay	T_{PDD}	—	2.5	—	µs	V_{DD} = 5V PD1:PD0 → 00 (from '01', '10', or '11'), from falling edge SCL at end of ACK bit.
		—	5	—	µs	V_{DD} = 3V PD1:PD0 → 00 (from '01', '10', or '11'), from falling edge SCL at end of ACK bit.
Power-Down Enable Time Delay	T_{PDE}	—	10.5	—	µs	PD1:PD0 → 01, '10', or '11' (from '00'), from falling edge SCL at end of ACK bit.

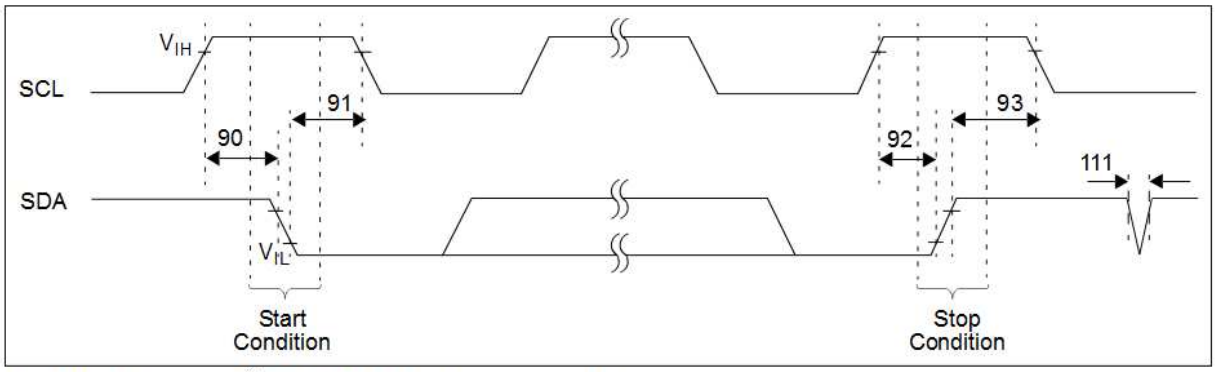


FIGURE 1-3: *I^2C Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-2: I^2C BUS START/STOP BITS REQUIREMENTS

I^2C™ AC Characteristics				**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ TA ≤ +125°C (Extended) Operating Voltage VDD range is described in **Electrical Characteristics**			
Param. No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
	F_{SCL}	SCL pin Frequency	Standard mode	0	100	kHz	C_b = 400 pF, 2.7V - 5.5V
			Fast mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
			High-Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V - 5.5V
			High-Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V - 5.5V
D102	C_b	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	$T_{SU:STA}$	Start condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated Start condition
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	$T_{HD:STA}$	Start condition Hold time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	$T_{SU:STO}$	Stop condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	$T_{HD:STO}$	Stop condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
94	T_{HVCSU}	HVC to SCL Setup time		25	—	uS	High Voltage Commands
95	T_{HVCHD}	SCL to HVC Hold time		25	—	uS	High Voltage Commands

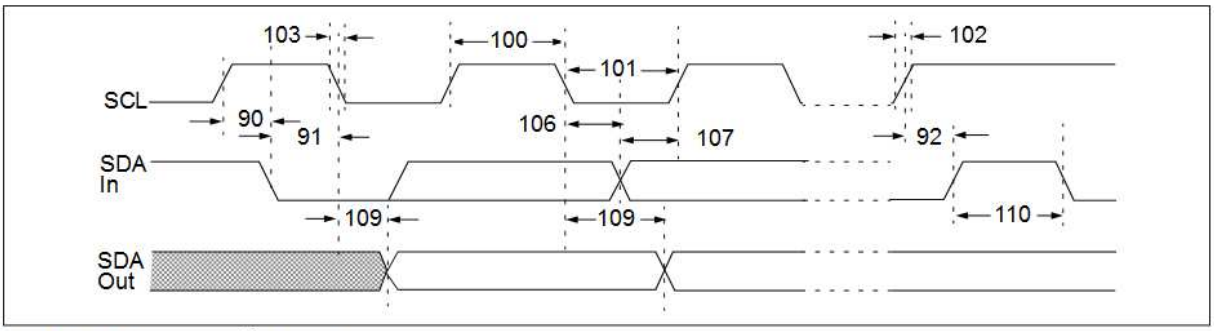


FIGURE 1-4: *I^2C Bus Data Timing.*

TABLE 1-3: I^2C BUS DATA REQUIREMENTS (SLAVE MODE)

I^2C™ AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Electrical Characteristics**				
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
100	THIGH	Clock high time	100 kHz mode	4000	—	ns	2.7V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120		ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	TLOW	Clock low time	100 kHz mode	4700	—	ns	2.7V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320		ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I^2C™ bus device can be used in a Standard mode (100 kHz) I^2C bus system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line.
T_R max.+$t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

3: The MCP47X6 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I^2C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested. This parameter ensured by characterization.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I^2C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.

Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

7: Ensured by the T_{AA} 3.4 MHz specification test.

8: The specification is not part of the I^2C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).

TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C™ AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Electrical Characteristics**				
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
102A(5)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a Repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a Repeated Start condition or an Acknowledge bit
102B(5)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
103A(5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B(5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb(4)	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C™ bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line.
T_R max.+$t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.

3: The MCP47X6 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested. This parameter ensured by characterization.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

7: Ensured by the T_{AA} 3.4 MHz specification test.

8: The specification is not part of the I²C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).

TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C™ AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Electrical Characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
106	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	2.7V-5.5V, **Note 6**
			400 kHz mode	0	—	ns	2.7V-5.5V, **Note 6**
			1.7 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**
			3.4 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**
107	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**Note 2**
			400 kHz mode	100	—	ns	
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3750	ns	**Note 1**, **Note 8**
			400 kHz mode	—	1200	ns	
			1.7 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**, **Note 7**, **Note 8**
				—	310	ns	Cb = 400 pF, **Note 1**, **Note 5**, **Note 8**
			3.4 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**, **Note 8**
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N/A	—	ns	
			3.4 MHz mode	N/A	—	ns	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C™ bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line.
T_R max.+$t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.

3: The MCP47X6 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not Tested. This parameter ensured by characterization.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.

Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

7: Ensured by the T_{AA} 3.4 MHz specification test.

8: The specification is not part of the I²C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or T_{RSDA}).