University of Tehran

School of Electrical and Computer Engineering

CA#3 VLSI

Due Date:

1398/2/1

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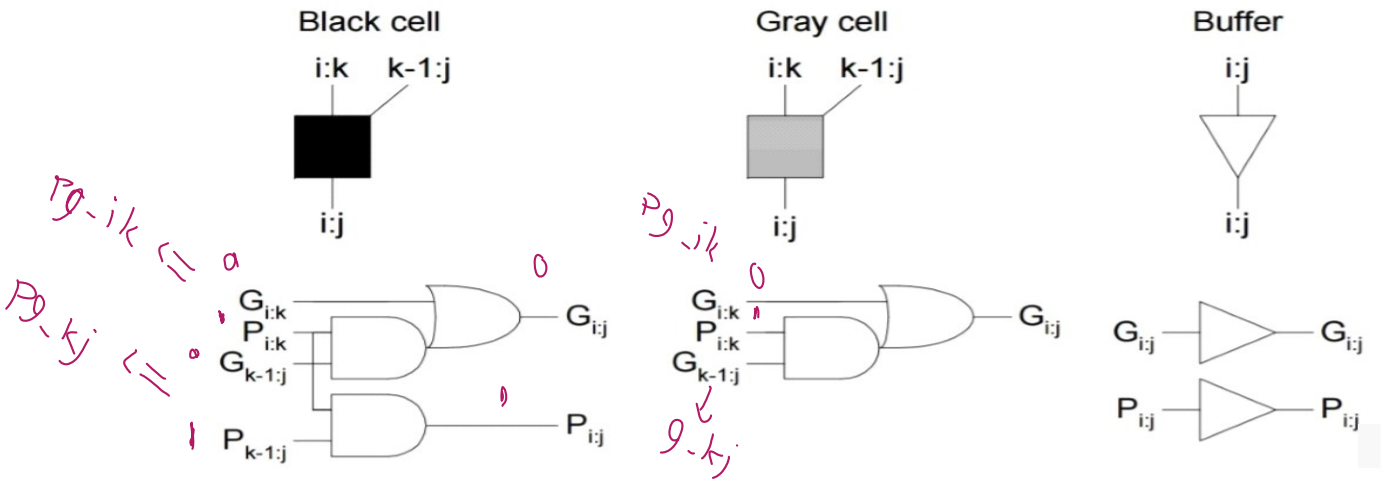
Good Luck.

In this Computer Assignment you are going to implement a 16-bit Kogge-Stone and a 16-bit Brent-Kung Adder in Modelsim.

You have to implement these two adders in gate level. Please note that this assignment DOES NOT require a report, thus your code should be MODULAR and clear to read.



After writing your code, compile and test your design using TCL and DO files in Modelsim. The next two references can help you through this step.

https://cseweb.ucsd.edu/classes/su12/cse141L-a/Media/modelsim_tut.pdf
(Chapter 8: Automating Simulation)

http://www.cems.uwe.ac.uk/~a2-lenz/n-gunton/worksheets/modelsim_tcl.pdf

Produce some test vectors (e.g. 10,000) and their corresponding results (Golden Results) and compare your Verilog code results with them in order to make sure your implementation is correct. For example you can use subtraction, or any other idea you may have.