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  - [time group](#)

# Complete Projects

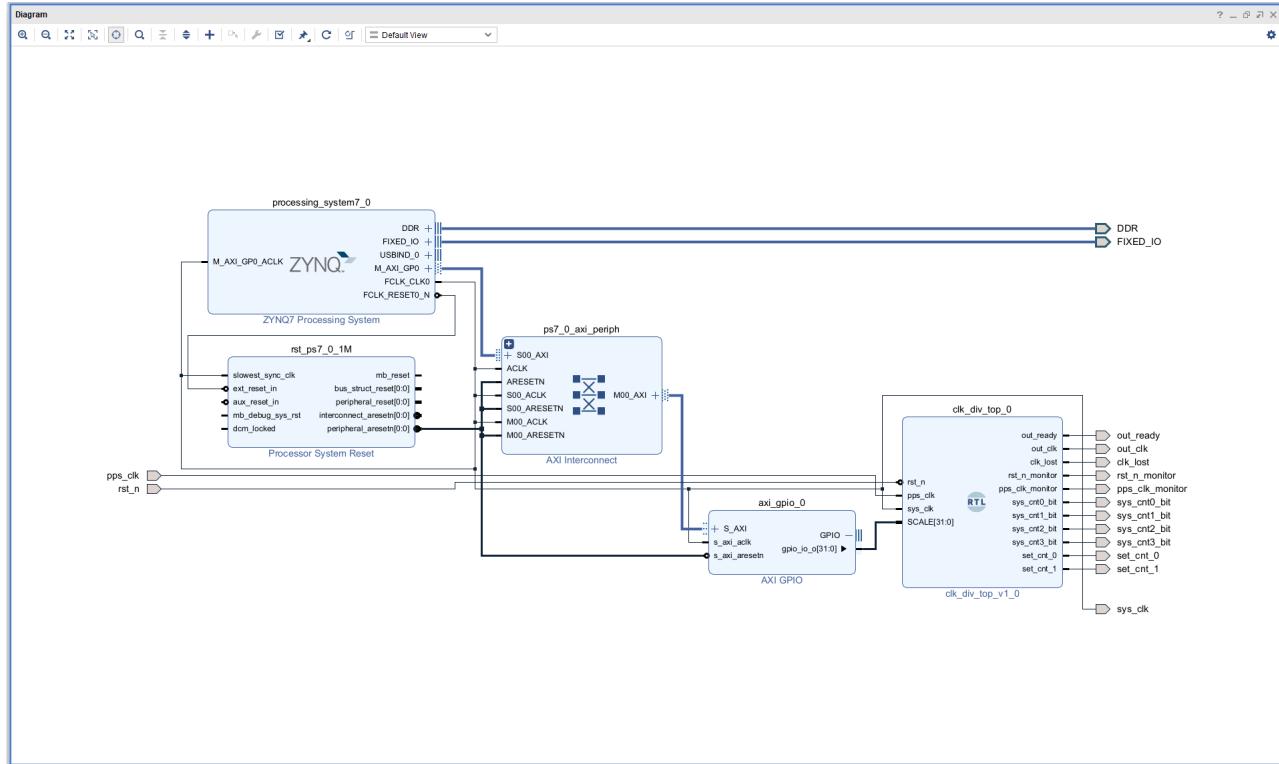
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The setup using AXI is working:

- [project\\_clk\\_div\\_scale\\_auto \(Vivado\)](#)
- [clk\\_div\\_scale\\_auto \(Vitis\)](#)
- [clk\\_div\\_scale\\_auto \(WaveForms\)](#)

The setup using PS is still problematic.

## Code



- module
- testbench
- constraint
- software

## Software setup

- I/O standard for pins:  $V_{CCO\_34} = 3.3 \text{ V}$
- Pin Mapping (Bank 34):

<b>package_pin</b>	<b>pin_name</b>	<b>JX1_pin_#</b>	<b>CON1_pin_#</b>	<b>block_pin_name</b>	<b>DIO #</b>
N/A	GND	N/A	1, 2	N/A	GND, GND
T11	JX1_LVDS_0_P	11	5	sys_clk	0
T12	JX1_LVDS_1_P	12	6	out_ready	1
T10	JX1_LVDS_0_N	13	7	out_clk	2
U12	JX1_LVDS_1_N	14	8	clk_lost	3
U13	JX1_LVDS_2_P	17	9	rst_n	W1
V12	JX1_LVDS_3_P	18	10	pps_clk	W2
V13	JX1_LVDS_2_N	19	11	rst_n_monitor	4

package_pin	pin_name	JX1_pin_#	CON1_pin_#	block_pin_name	DIO_#
W13	JX1_LVDS_3_N	20	12	pps_clk_monitor	13
T14	JX1_LVDS_4_P	23	13	sys_cnt0_bit	6
P14	JX1_LVDS_5_P	24	14	sys_cnt1_bit	7
T15	JX1_LVDS_4_N	25	15	sys_cnt2_bit	8
R14	JX1_LVDS_5_N	26	16	sys_cnt3_bit	9
Y16	JX1_LVDS_6_P	29	19	set_cnt_0	10
W14	JX1_LVDS_7_P	30	20	set_cnt_1	11

- To program via JTAG with Independent JTAG chain: JP3: 1-2 (0), JP2: 1-2 (0), JP1: 2-3 (1)

The 1x3 jumper options with default positions highlighted are shown below. The default position is Cascaded JTAG Chain, QSPI Boot. Defaults highlighted in yellow below.

**Table 17 – MicroZed Configuration Modes**

Xilinx TRM MIO →	JP3	JP2	JP1
	Boot_Mode[0]	Boot_Mode[2]	Boot_Mode[3]
	MIO[5]	MIO[4]	MIO[2]
<b>JTAG Mode</b>			
Cascaded JTAG Chain			1-2 (0)
Independent JTAG Chain			2-3 (1)
<b>Boot Devices</b>			
JTAG		1-2 (0)	
Quad-SPI		2-3 (1)	1-2 (0)
SD Card		2-3 (1)	2-3 (1)

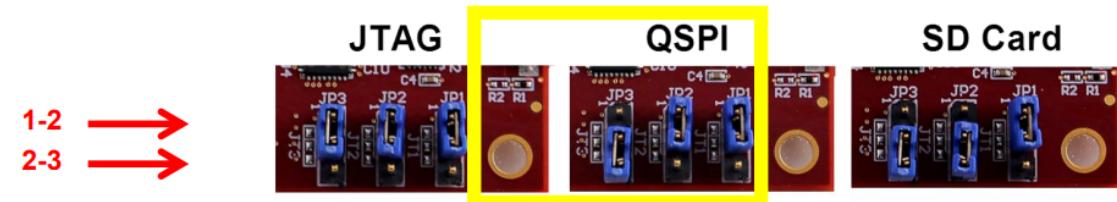
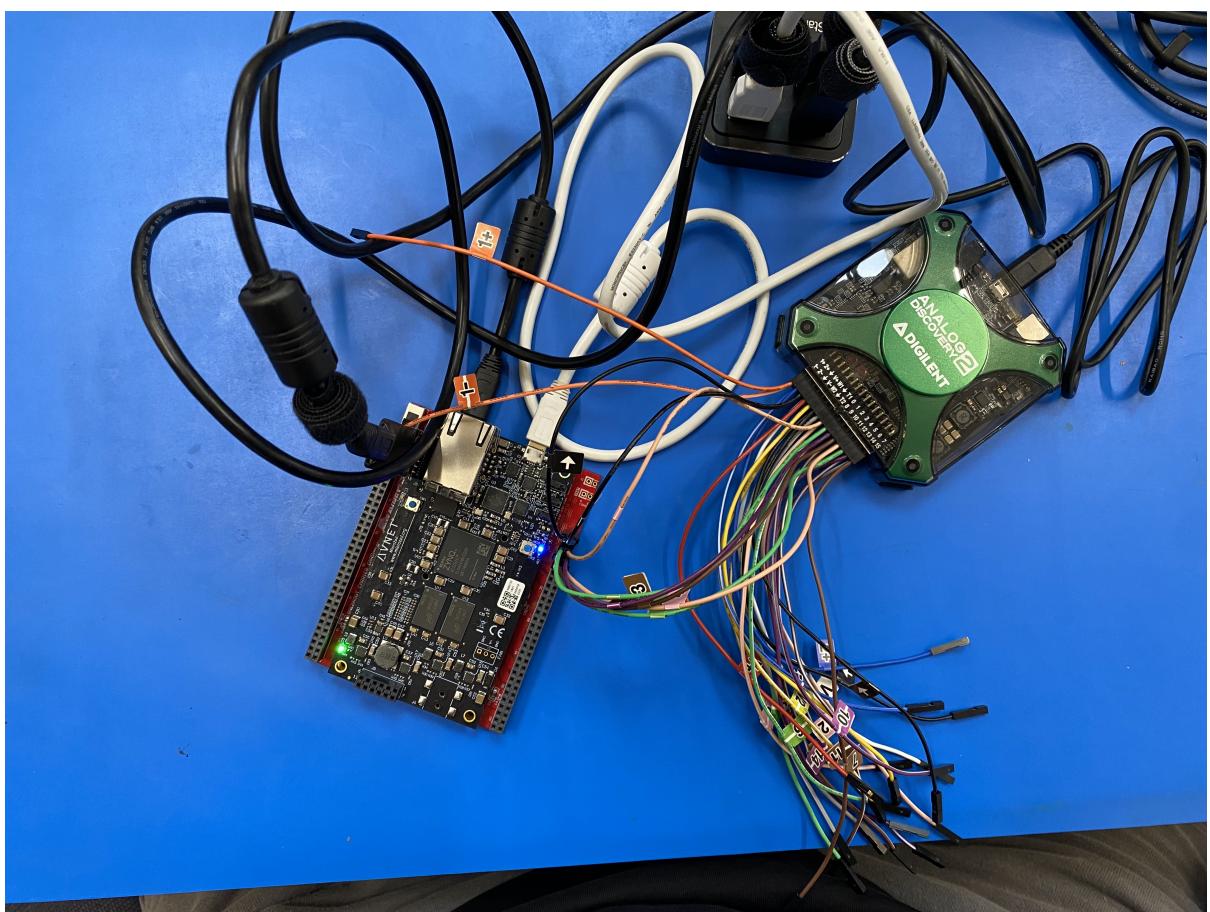


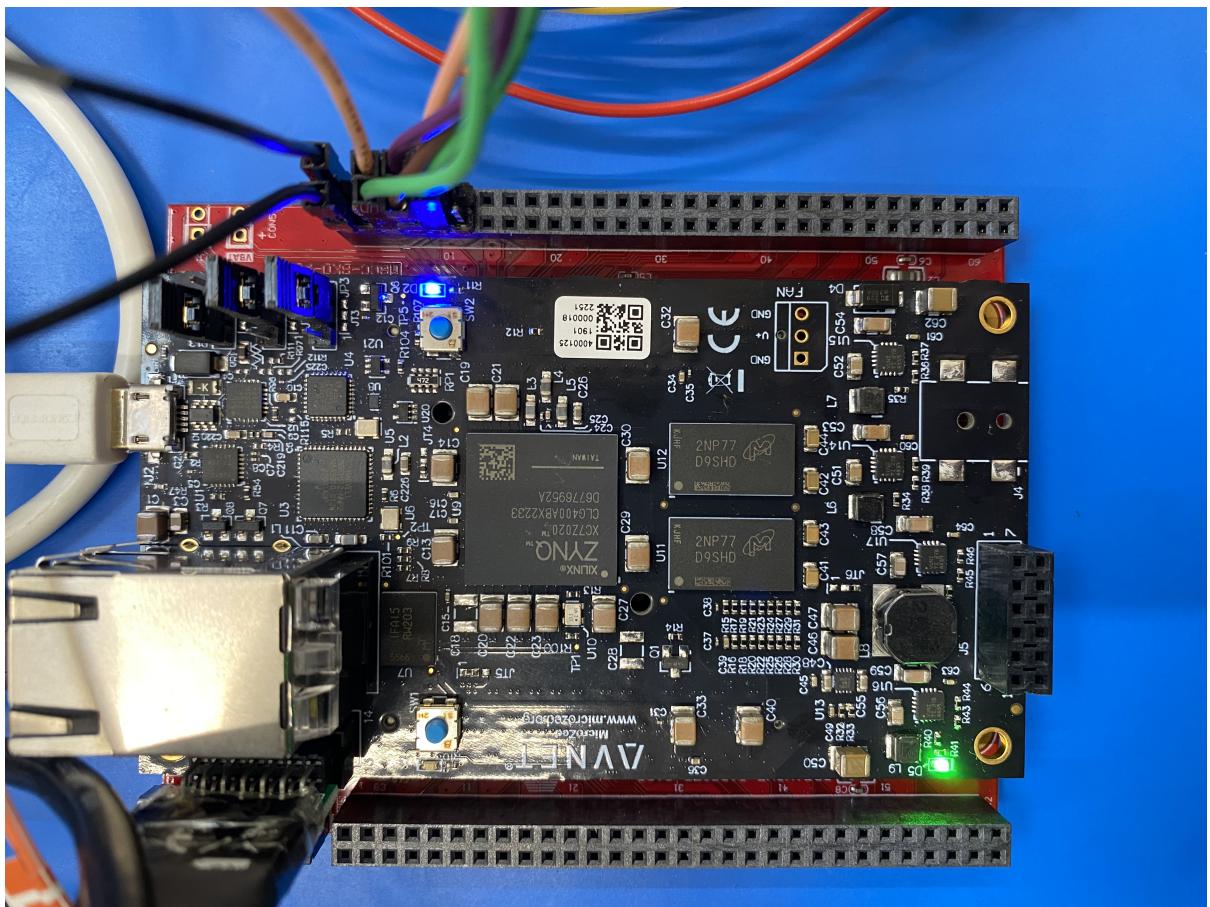
Figure 8 – Boot Mode Jumper Settings with Cascaded JTAG Chain

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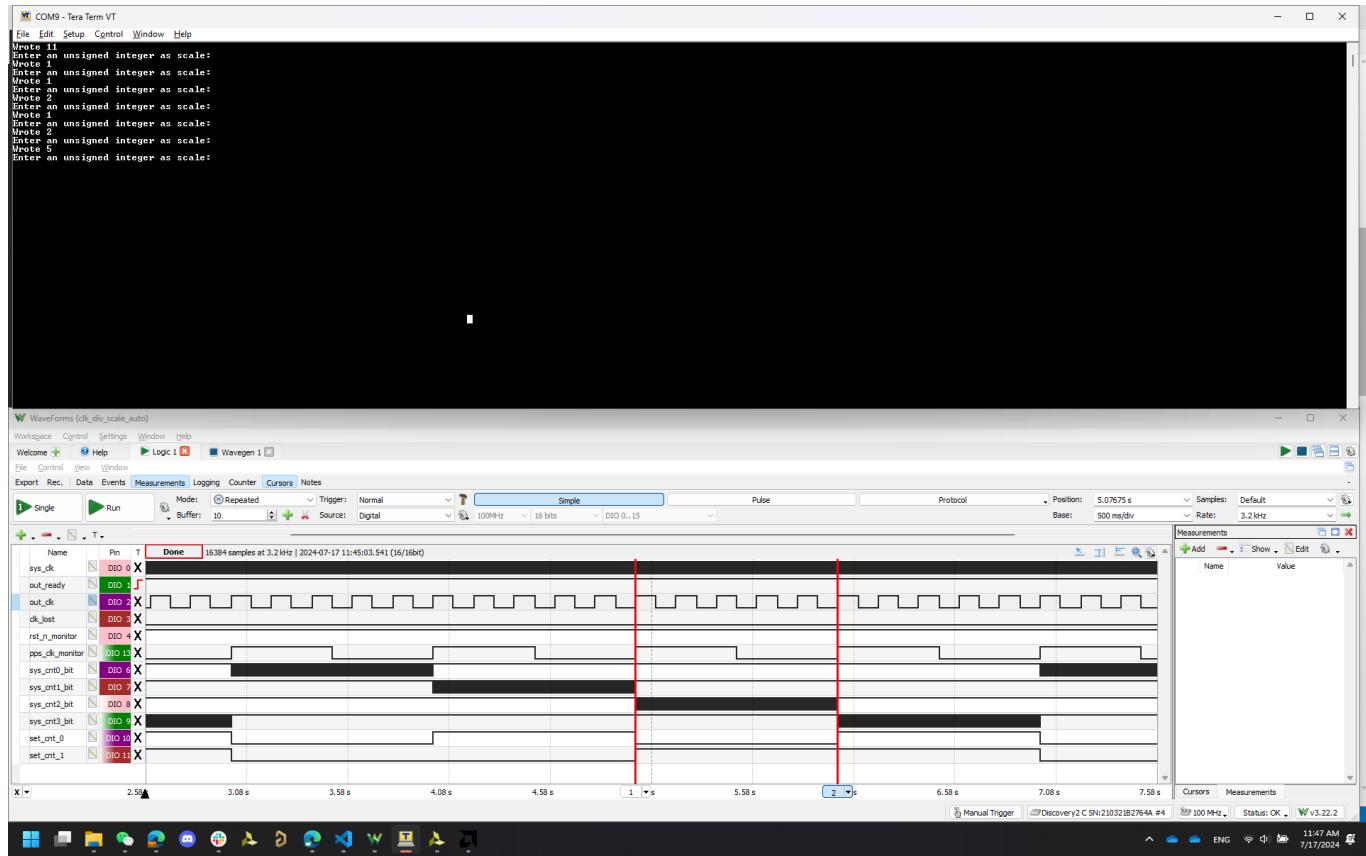
- o far view:



- o near view:



## Running Waveform



## Problem

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- If I change the scale after out\_clk is ready, out\_clk will be out of sync from pps\_clk. I'll change RTL so that reset can be triggered whenever scale is changed.
- Issue with the PS setup: The takeaway from [fpgawork video](#) is mainly that EMIO starts from BANK2. But when I use BANK2, only the LSB is recognized. **The main problem is still that I can't find the exact documentation of EMIO pin mapping.**