1) Simplify .

$Y = \overline{ACD} + \overline{\overline{B}(C + A(\overline{BD}))} + \overline{A}B\overline{C}\,\overline{D}$

$= \overline{ACD} + \overline{B} + (\overline{\overline{C} + A(\overline{BD})}) + \overline{A}B\overline{C}\,\overline{D}$

$= \overline{ACD} + \overline{B} + C + A(\overline{BC}) + \overline{A}B\overline{C}\,\overline{D}$

$= \overline{ACD} + \overline{B} + C + A\overline{B} + A\overline{C} + \overline{A}B\overline{C}\,\overline{D}$

$= \overline{ACD} + \overline{B}(A+1) + C + A\overline{C} + \overline{A}B\overline{C}\,\overline{D}$

$= \overline{ACD} + \overline{B} + C + A\overline{C} + \overline{A}B\overline{C}\,\overline{D}$

$= \overline{A} + \overline{C} + \overline{D} + \overline{B} + C + A\overline{C} + \overline{A}B\overline{C}\,\overline{D}$

$= \overline{A}[1 + B\overline{C}\,\overline{D}) + \overline{C} + C + A\overline{C} + \overline{D} + \overline{B}$

$= \overline{A} + \overline{C}(A+1) + C + \overline{D} + \overline{B}$

$= \overline{A} + \overline{C} + C + \overline{D} + \overline{B}$

$= 1 + \overline{A} + \overline{D} + \overline{B}$

$= 1$

$\therefore Y = 1$

2) $Z = A\overline{B} + \overline{A}CD + \overline{A}\overline{B}C + A\overline{B}C\overline{D}$

$= A\overline{B}(C + \overline{C}) + \overline{A}CD(B + \overline{B}) + \overline{A}\overline{B}C(D + \overline{D}) + A\overline{B}C\overline{D}$

$= (A\overline{B}C + A\overline{B}\overline{C})(D + \overline{D}) + \overline{A}CDB + \overline{A}CD\overline{B} + \overline{A}\overline{B}CD + \overline{A}\overline{B}C\overline{D} + A\overline{B}C\overline{D}$

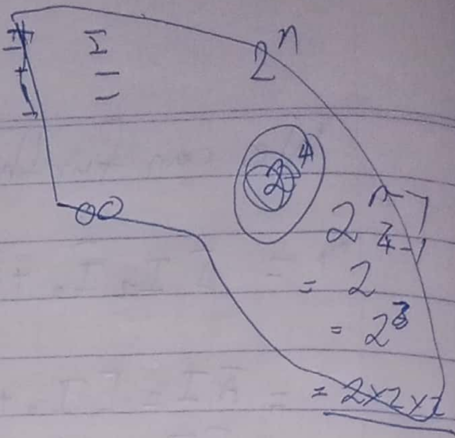
$= A\overline{B}CD + A\overline{B}C\overline{D} + A\overline{B}\overline{C}D + A\overline{B}\overline{C}\,\overline{D} + \overline{A}BCD + \overline{A}\overline{B}CD + \overline{A}\overline{B}CD + \overline{A}BC\overline{D} + \overline{A}\overline{B}C\overline{D}$

$\Sigma_m \{11, 10, 9, 8, 7, 5, 5, 6, 10\}$

$= \Sigma_m (11, 10, 9, 8, 7, 5, 6)$

$= \Sigma_m (5, 6, 7, 8, 9, 10, 11)$

4 5 — 0101   421 — 0111   1111 = 8+4+2+1



CD \ AB	00	01	11	10
00	0	4	12	1 (8)
01	1	1 (5)	13	1 (9)
11	3	1 (7)	15	1 (11)
10	2	1 (6)	14	1 (10)

$Y = A\bar{B} + \bar{A}BD + \bar{A}BC$

$Y = A\bar{B} + \bar{A}BD + \bar{A}BC$

(3) Multiplexer. → Multiplexer or Mux is a digital switch. This is also known as data selector. It is a combinational circuit with 2^n inputs where $n > 0$; n selector lines and one output. Selector lines are used to select or map one particular input to the output.

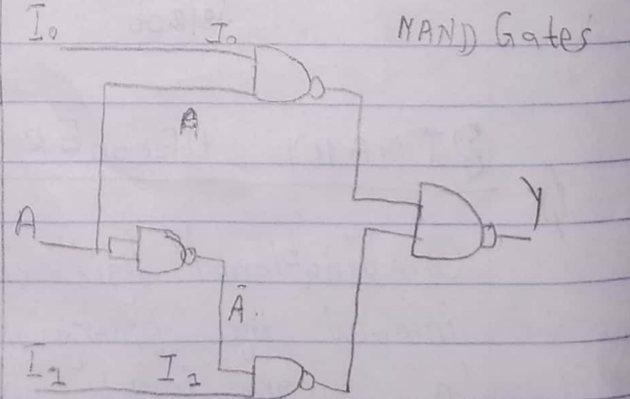
The 2×1 Multiplexer is an example.

$A \Rightarrow n$, $n = 1$

$2^n = 2^1 = 2$ Output = Y

$n = 2 = A$ Inputs : I_1, I_0

Selector A	Inputs I_1	I_0	Output Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



A acts as a selector between the two I_0 and I_1 inputs for output Y.

We can further prove this by boolean expression

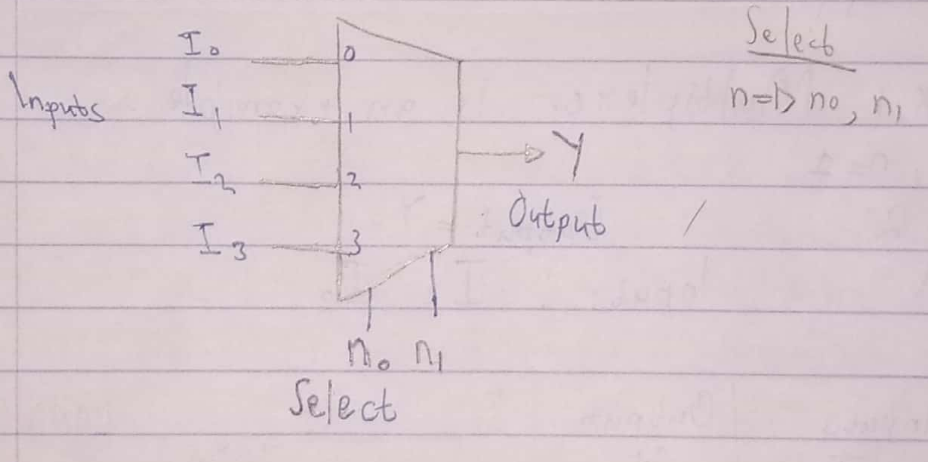
$Y = \bar{A} I_2 \bar{I}_0 + \bar{A} I_1 I_0 + A \bar{I}_0 \bar{I}_1 + A I_0 I_1$

$= \bar{A} I_2 [I_0 + \bar{I}_0] + A I_0 [\bar{I}_1 + I_1]$

$= \bar{A} I_2 + A I_0$

The procedure can be used for any 2^n inputs by 1 output multiplexer

Thus for $n = 2$,
Inputs $= 2^2 = 4$
Selector lines $= 2$
The multiplexer can be represented by a symbol.

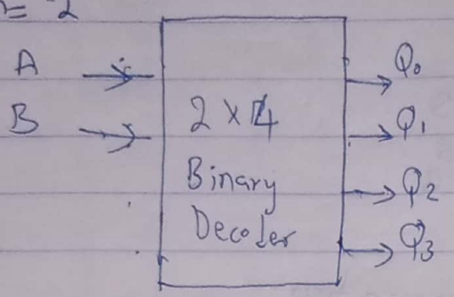


BINARY DECODER

Combinational logic circuit that decodes messages incoded by binary encoder. Binary decoder transforms 'n' binary inputs into 2^n outputs. n inputs activate one and only one of 2^n outputs to be

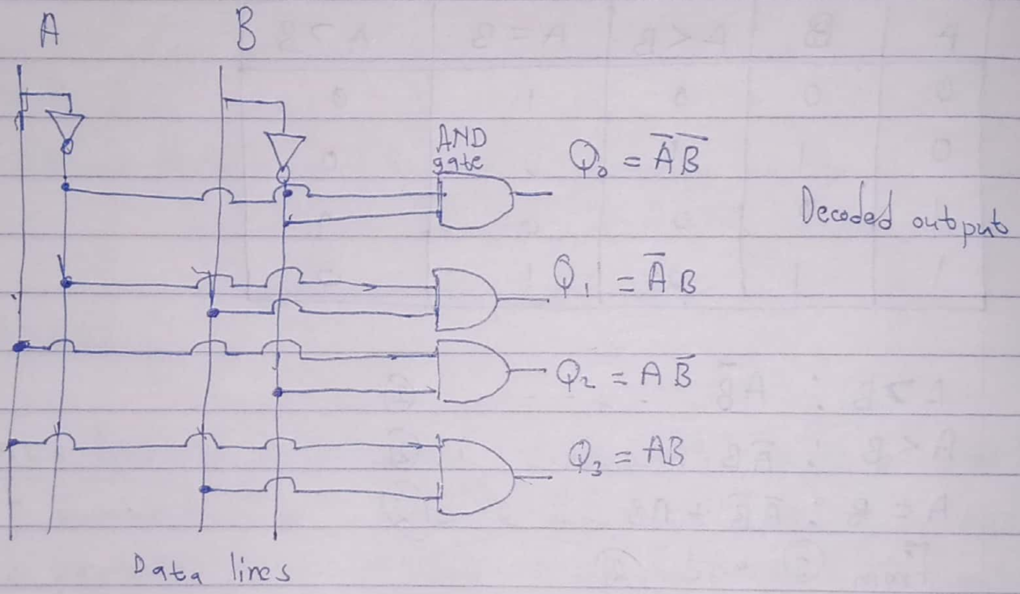
Example 2 x 4 Binary Decoder using AND gates

n = 2



A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

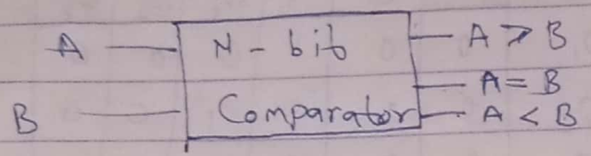
Each output represents one of the miniterms of the input variables A, B.



A NAND gate combinational circuit ~~acti~~ has only one output equal to logic '0' with all others '1' at any given time.

MAGNITUDE COMPARATOR → combinational circuit that compares two digital or binary numbers to find out if one is equal, greater or lesser than the other. For instance input A and B have three ouput terminals A > B, A = B and A < B functions.

This block diagram demonstrates the definition above.



1-Bit Magnitude comparator:

A comparator for comparing two bits is called a single-bit comparator.

1 bit comparator truth table.

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

$A>B : A\bar{B}$ - - - - - (1)

$A<B : \bar{A}B$ - - - - - (2)

$A=B : \bar{A}\bar{B}+AB$ - - - - (3)

From (1) and (2)

$(A<B)+(A>B) = A\bar{B}+\bar{A}B$

$((A<B)+(A>B))' = \overline{(A\bar{B}+\bar{A}B)}$

$= (\overline{A\bar{B}})(\overline{\bar{A}B})$

$= (\bar{A}+B)(A+\bar{B})$

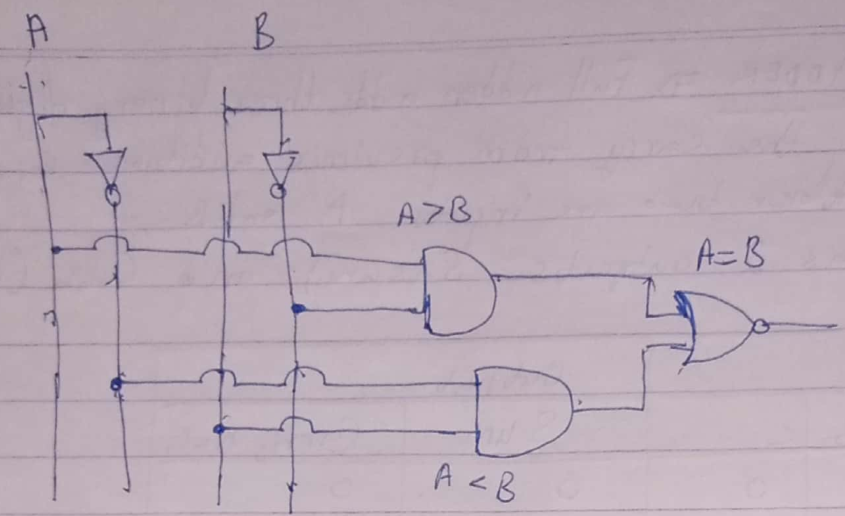
$= \bar{A}A+\bar{A}\bar{B}+AB+B\bar{B}$

$= \bar{A}\bar{B}+AB$

Thus

$((A<B)+(A>B))' = (A=B)$

Single-bit Comparator Combinational Circuit



For an n-bit comparator the number of combinations are

$A = B : 2^n$

$A > B$ or $A < B : \frac{(2^{2n} - 2^n)}{2}$

ADDERS

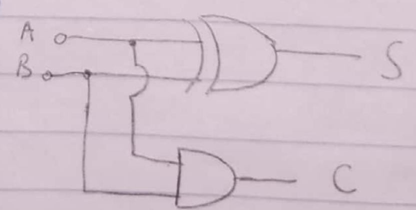
HALF ADDER - Electronic circuit that performs addition of numbers. It is able to add two single binary digits and provide the output plus a carry value. Two inputs A and B, and two outputs S and C
S (sum), C (carry)

Half adder Truth table.

Inputs		Outputs	
A	B	C	S
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

$S = A\bar{B} + \bar{A}B = A \oplus B$

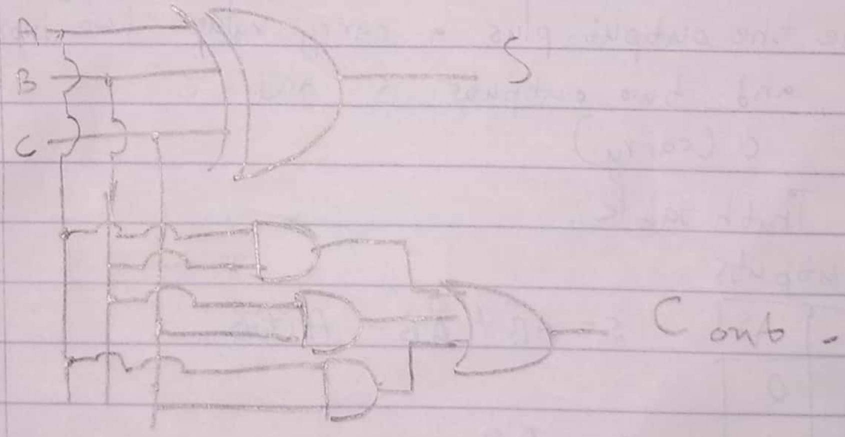
$C = AB$



FULL ADDER ⇒ Full adder adds three binary digits
One is the carry from previous addition C_{in}.
The other two are inputs A and B
It has 2 outputs S.(sum) and C_{out} (carry output)

Input			Output	
A	B	C	Sum	Carry Out
0	0	0	0	0
1	1	1	1	1
0	1	1	0	1
1	0	1	0	1
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

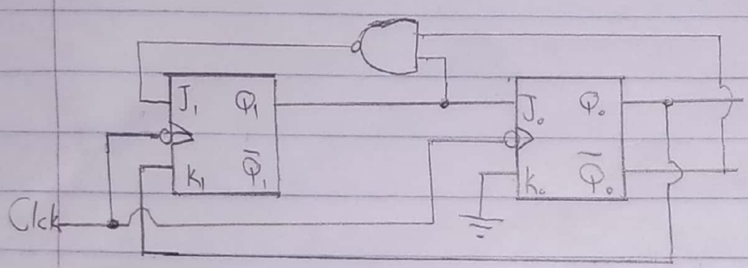
$$\text{Carry out} = AB + BC_{in} + AC_{in}$$
$$\text{Sum} = (A \oplus B) \oplus C_{in}$$

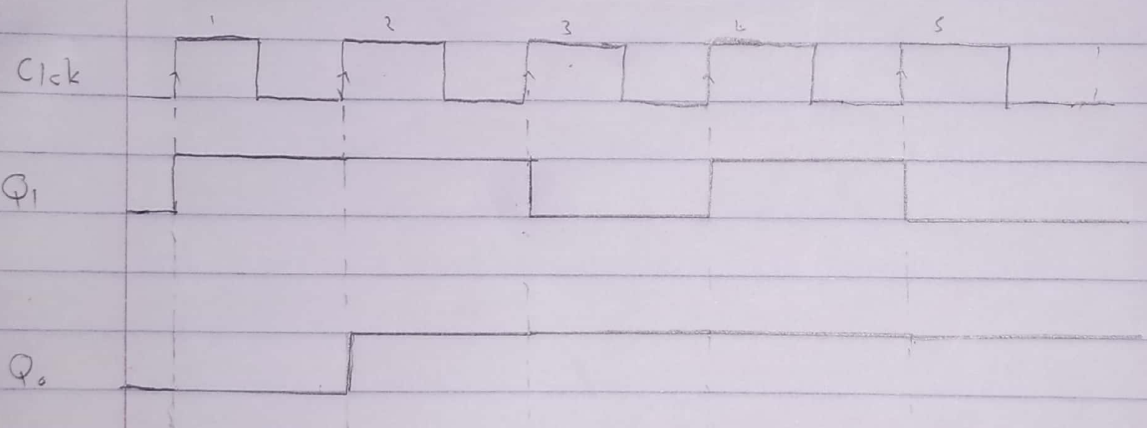


4) Sequential logic circuit of two JK FF's. Initially Cleared obtain the output Q_1 and Q_0 For 5 clock.

Truth table for JK flipflop

J	K	Q	Clck
0	0	Q [No change]	↑
0	1	0 [Reset]	↑
1	0	1 [Set]	↑
1	1	$\bar{Q}$ [Toggle]	↑





Clck	Q_1	Q_0
0	0	0
1	1	0
2	1	1
3	0	1
4	1	1
5	0	1