112 上學期 系統晶片設計 SOC Design Laboratory LAB1

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學系: 電控專

1. Tool Installation

The screenshot of Xilinx tools(Check your tool version)

> Vitis

```
ubuntugubuntu2004:-/Desktop5 vitis

****** Xllinx Vitis Development Environment
******* Vitis v2022.1 (64-bit)
****** Sw Build 3524922 on 2022-04-14-18:00:18
*** Copyright 1986-2022 Xllinx, Inc. All Rights Reserved.

***** Copyright 1986-2022 Xllinx, Inc. All Rights Reserved.

Launching Vitis with command /tools/Xllinx/Vitis/2022.1/eclipse/inx64.0/eclipse -vmargs -Xms64m -Xmx1024m -Dorg.eclipse.swt.internal.gtk.cairoGraphics=false -Dosgl.conffiguration.area=@user.home/.Xllinx/Vitis/2022.1 -add-nodules-All-SYSTEM --add-opens=java.base/java.nio=All-UNNAMED --add-opens=java.desktop/javax.swing=All-UNNAMED --add-opens=java.desktop/javax.swing=All-UNNAMED --add-opens=java.desktop/javax.swing=All-UNNAMED --add-opens=java.desktop/javax.swing=All-UNNAMED --add-opens=java.desktop/javax.swing=Infl.-UNNAMED --add-opens=javax.desktop/javax.swing=Infl.-UNNAMED --add-opens=javax.desktop/javax.swing=Infl.-UNNAMED --add-opens=javax.desktop/javax.swing=Infl.-UNNAMED --add-opens=javax.desktop/javax.swing=Infl.-UNNAMED --add-opens=javax.desktop/javax.swing=Infl.-UNNAMED --add-opens=javax.desktop/javax.swing=Infl.-UNNAMED --a
```

Vivado

```
ubuntu@ubuntu2004:~/Desktop$ vivado

***** Vivado v2022.1 (64-bit)
    **** SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
    **** IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
start_gui
```

Vitis_HLS

```
ubuntugubuntu2004:-/Desktop$ vitis_hls

****** Vitis HLS - High-Level Synthesis from C, C++ and OpenCL v2022.1 (64-bit)

****** SW Build 3526202 on Mon Apr 18 15:47:01 MDT 2022

**** IP Build 3526434 on Mon Apr 18 20:55:01 MDT 2022

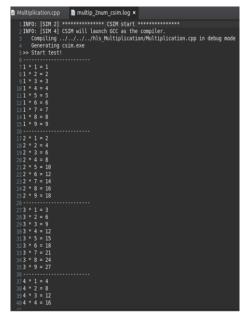
**** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.

source /tools/Xilinx/Vitis_HLS/2022.1/scripts/vitis_hls/hls.tcl -notrace
INFO: (HLS 200-10) Running '/tools/Xilinx/Vitis_HLS/2022.1/bin/unwrapped/inx64.0/vitis_hls'
INFO: (HLS 200-10) For user 'ubuntu' on host 'ubuntu2004.linuxvmimages.local' (Linux_x86_64 version 5.15.0-83-generic) on Sun Sep 17 04:52:09 EDT 2023
INFO: (HLS 200-10) In directory '/home/ubuntu/Desktop'
INFO: (HLS 200-10) Ringing up Vitis HLS GUI ...
```

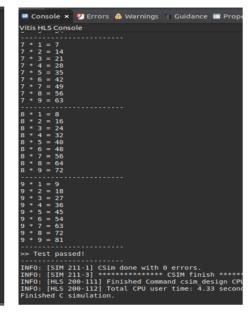
2. Co-Simulation Log

Co-simulation log(Usually located at VitisHLSProjectName/solution1/csim/report)

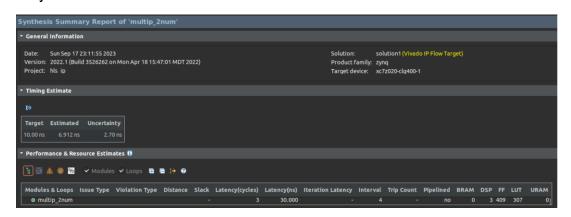
C simulation



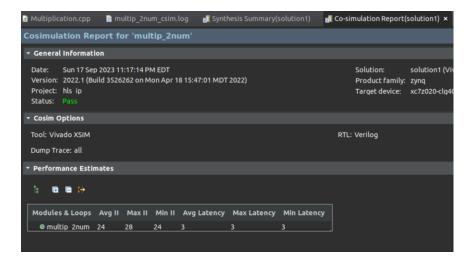
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62 6 * 6 = 36
63 6 * 7 = 42
64 6 * 8 = 48
65 6 * 9 = 54
667
67 * 1 = 7
68 7 * 2 = 14
69 7 * 3 = 21
70 7 * 4 = 28
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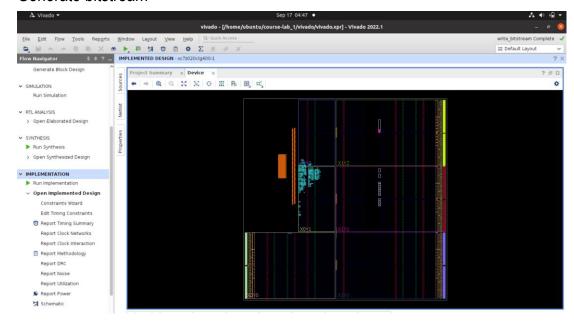
C synthesis



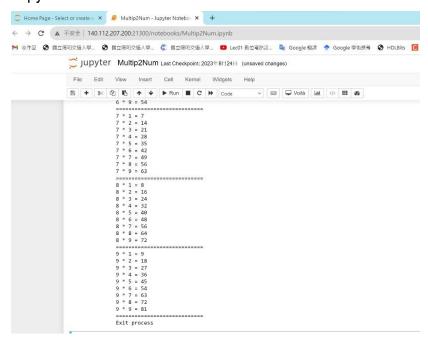
Cosimulation



Generate bitstream



> Jupyter notebook



3. Brief introduction about the overall system

用 HLS 的方式設計乘法器(Multip2Num),最後燒錄 FPGA 做驗證實驗步驟: (lab1 主要為讓學生了解如果操作,並無 coding)

- 1. vitis_hls 建置 Multip2Num IP (匯出 RTL)
- 2. vivado 使用 Multip2Num IP 並與其他電路連接,最後產生 BITSTREAM
- 3. 使用租借的 FPGA 燒錄
- 4. 用 PYTHON 對燒錄後的電路驗證

4. What is observed & learned

➤ Ubuntu 安裝困難

筆電容量如下圖剩下不多,因此需要外接硬碟(如 E 槽),剩餘的部分就按照說明做

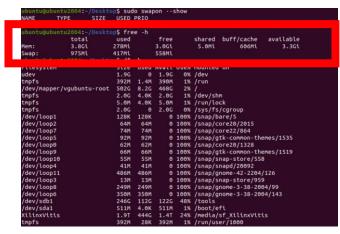
> 裝置和磁碟機

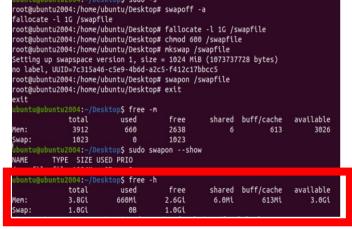


➤ Vivado 閃退問題

如下圖只要開始執行 BITSTREAM 這個步驟,就會發生閃退問題,畫面顯示 "RDI_PROG"

而後查證問題為內存不足(圖左),因此需要 SWAP 擴充,步驟如(圖右)





參考網址:

https://medium.com/@ihsanalhafiz28/how-to-solve-vivado-crash-on-ubuntu-while-running-4b445d609fa5

▶ 心得:

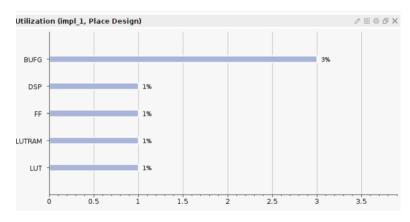
安裝與軟體熟悉比較麻煩,因為 LAB1 不需要 CODING 主要是解決硬體安裝上的問題~

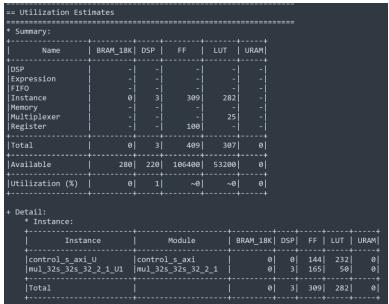
5. SCREEN DUMPS

PERFORMANCE

== Vitis HLS Report for 'multip_2num'						
* Date: Fri Sep 15 20:43:58 2023						
e. 111 3ep 13 20.43.36 2023						
rsion: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)						
<pre>* Project: hls_ip * Solution: solution1 (Vivado IP Flow Target)</pre>						
* Product family: zynq						
* Target device: xc7z020-clg400-1						
======================================						
== Performance Estimates						
+ Timing:						
* Summary: ++						
Clock Target Estimated Uncertainty						
++						
+ Latency:						
* Summary:						
Latency (cycles) Latency (absolute) Interval Pipeline						
						
3 3 30.000 ns 30.000 ns 4 4 no						

➤ UTILIZATION



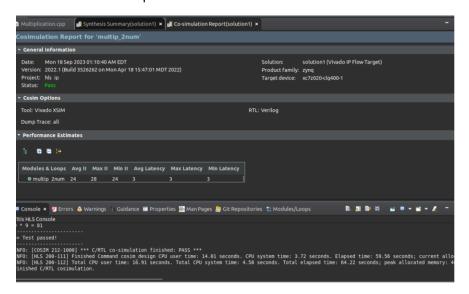


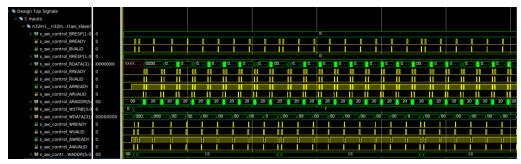
```
* DSP:
N/A
* Memory:
N/A
* FIFO:
N/A
* Expression:
N/A
* Multiplexer:
| Name | LUT| Input Size| Bits| Total Bits|
|ap_NS_fsm | 25| 5| 1| 5|
|Total | 25| 5| 1| 5|
* Register:
Name | FF | LUT| Bits| Const Bits|
--+----+
|Total | 100| 0| 100| 0|
```

Interface

== Interface						
* Summary:						
+	++	+	+	+		
RTL Ports	Dir	Bits	Protocol	Source Object	C Type	
s axi control AWVALID	++ in	 1	 s axi		pointer	
s axi control AWREADY	out	1	s axi	control	pointer	
s axi control AWADDR	out in	6	s axi	control	pointer	
s axi control WVALID	in	1	s axi	control	pointer	
s axi control WREADY	out	1	s axi	control	pointer	
s axi control WDATA	in	32	s axi	control	pointer	
s axi control WSTRB	in	4	s axi	control	pointer	
s axi control ARVALID	in	1	s axi	control	pointer	
s axi control ARREADY	out	1	s axi	control	pointer	
s axi control ARADDR	in	6	s axi	control	pointer	
s_axi_control_RVALID	out	1	s_axi	control	pointer	
s_axi_control_RREADY	in	1	s_axi	control	pointer	
s_axi_control_RDATA	out	32	s_axi	control	pointer	
s_axi_control_RRESP	out	2	s_axi	control	pointer	
s_axi_control_BVALID	out	1	s_axi	control	pointer	
s_axi_control_BREADY	in	1	s_axi	control	pointer	
s_axi_control_BRESP	out	2	s_axi	control	pointer	
ap_clk	in	1	ap_ctrl_none	multip_2num	return value	
ap_rst_n	in	1	ap_ctrl_none	multip_2num	return value	
+	++	+		+		

Co-simulation transcript/waveform





Jupyter Notebook execution results

