

112 上學期
系統晶片設計
SOC Design Laboratory LAB2

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1. Brief introduction about the overall system

兩種不同的通訊協議和其不同的用途與應用，實際操作 HLS 更了解 TOOL 的操作模式和資料傳輸方式及其設定等等問題

2. What is observed & learned

➤ Differences between MAXI and Stream interface

這是 2 種不同的兩種不同的通信協議，它們在硬件設計中通常用於不同的用途，並且可以相互配合以實現複雜的系統功能，以下分別分類兩者的不同

A. MAXI (AXI-Master):

I. Address-Based Protocol

它根據內存地址操作。它用於訪問內存映射的 IP 核和外設

II. Read and Write Operations

MAXI 支援讀取和寫入操作。它允許從特定內存地址讀取數據，並將數據寫入內存映射區域

III. Arbitration and Multiplexing

因為多個主機可能競爭訪問相同的內存或外設。它支援多通道數據傳輸

IV. Complex Control and Configuration

如突發傳輸、無序執行和高級保護機制，適用於高性能和複雜的內存訪問場景

V. Example Usage

通常用於與處理器（例如 CPU）、DMA 控制器、內存和其他內存映射外設在系統芯片（SoC）設計中進行接口

B. Stream Interface:

I. Data Streaming Protocol

一種數據流協議。它用於連續和順序數據傳輸，不涉及內存地址的概念

II. Point-to-Point Communication

數據直接從一個源傳輸到一個目的地，不涉及地址或內存映射

III. Low Overhead

非常適合連續數據流的應用，如音頻處理、圖像處理或任何需要連續數據流的操作

IV. No Addressing

與 MAXI 不同，Stream 界面不需要地址信息，使其對於數據流傳輸更加簡單和高效。

V. Example Usage

Stream 界面通常用於連接處理連續數據流的 IP 核，例如音頻處理或圖像處理塊，在 FPGA 或 ASIC 設計中

總之，MAXI 是一種有地址的、用於處理特定位置數據的方式，而 Stream 界面是一種連續的、不需要地址的方式，用於處理連續數據流。在硬件設計中，根據您的需求，您可以選擇使用這兩種不同的通信方式。

➤ Differences between csim and cosim

簡單來說 Simulation 是單獨測試元件，而 co-sim 就是將多個不同的元件放在一起互相模擬，確保整個系統的和諧運作

➤ Difficult and problem need to know

A. 必須限制 loop 次數才可以得到計算的時間: (如下圖 line 23)

```
FIR.cpp x FIR.h fir_n11_strm_csim.log Synthesis Summary(solution1)
1  #include "FIR.h"
2
3
4 void fir_n11_strm(stream_t* pstrmInput, stream_t* pstrmOutput, int32_t an32Coef[MAP
5 {
6     #pragma HLS INTERFACE s_axilite port=regXferLeng
7     #pragma HLS INTERFACE s_axilite port=an32Coef
8     #pragma HLS INTERFACE axis register both port=pstrmOutput
9     #pragma HLS INTERFACE axis register both port=pstrmInput
10    #pragma HLS INTERFACE s_axilite port=return
11    static int32_t an32ShiftReg[N];
12    int32_t n32Acc;
13    int32_t n32Data;
14    int32_t n32Temp;
15    int32_t n32Loop;
16    int32_t n32NumXfer4B;
17    int32_t n32XferCnt;
18    value_t valTemp;
19
20    n32NumXfer4B = (regXferLeng + (sizeof(int32_t) - 1)) / sizeof(int32_t);
21    XFER_LOOP:
22    for (n32XferCnt = 0; n32XferCnt < n32NumXfer4B; n32XferCnt++) {
23        #pragma HLS LOOP_TRIPCOUNT min=0 max=1000
24        n32Acc = 0;
25        value_t valTemp = pstrmInput->read();
26        n32Temp = valTemp.data;
27    SHIFT_ACC_LOOP:
```

B. 必須根據使用的 FPGA 版子決定參照的 ADDRESS

BOARD : KV260

```
"    ol = Overlay("/home/root/jupyter_notebooks/FIRN11MAXI.bit")\n",
"    ipFIRN11 = ol.fir_n11_maxi_0\n",
"\"
```

BOARD: PYNQ

```
ol = Overlay("/home/xilinx/jupyter_notebooks/FIRN11Stream.bit")\n",
```

5. SCREEN DUMPS(FIRN11MAXI)

➤ PERFORMANCE(FROM fir_n11_maxi_csynth.RPT)

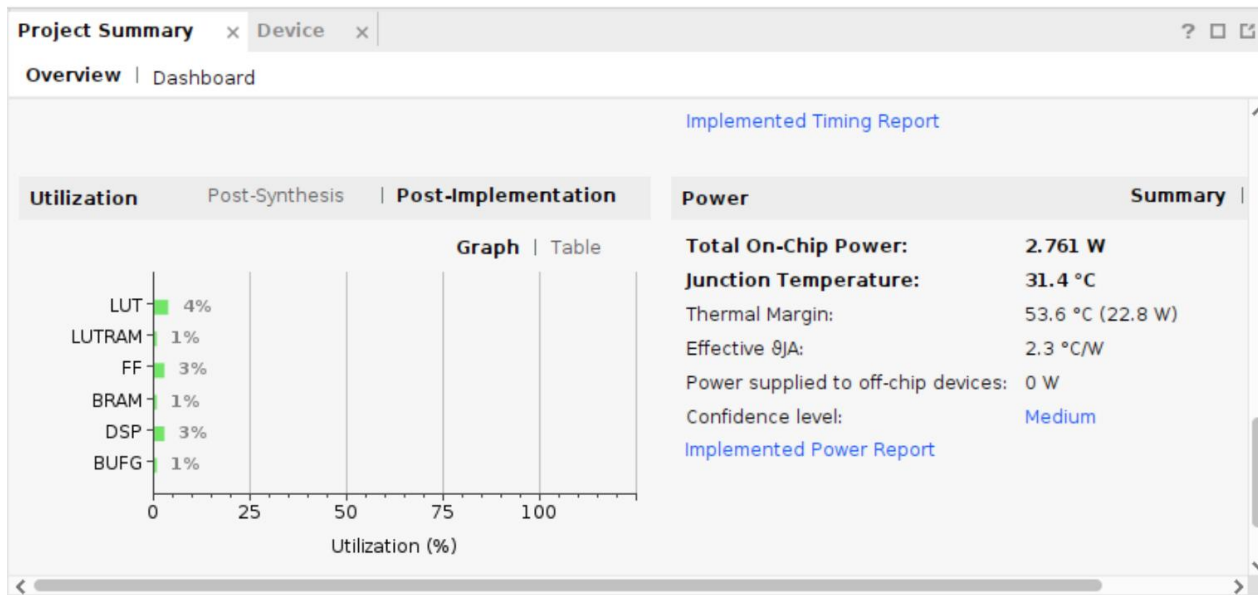
```
=====
== Performance Estimates
=====
+ Timing:
  * Summary:
  +-----+-----+-----+-----+
  | Clock | Target | Estimated | Uncertainty |
  +-----+-----+-----+-----+
  | ap_clk | 10.00 ns | 7.300 ns | 2.70 ns |
  +-----+-----+-----+-----+

+ Latency:
  * Summary:
  +-----+-----+-----+-----+-----+
  | Latency (cycles) | Latency (absolute) | Interval | Pipeline |
  | min | max | min | max | min | max | Type |
  +-----+-----+-----+-----+-----+
  | 25 | 1027 | 0.250 us | 10.270 us | 26 | 1028 | no |
  +-----+-----+-----+-----+-----+

+ Detail:
  * Instance:
  +-----+-----+-----+-----+-----+
  | Interval | Pipeline | Instance | Module | Latency (cycles) | Latency (absolute) |
  | min | max | Type | | min | max | min | max |
  +-----+-----+-----+-----+-----+
  | grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242 | fir_n11_maxi_Pipeline_XFER_LOOP | 12 | 1014 | 0.120 us | 10.140 us |
  | 12 | 1014 | no | | | | |
  +-----+-----+-----+-----+-----+

  * Loop:
  N/A
```

➤ UTILIZATION(FROM VIVADO & fir_n11_maxi_csynth.RPT)



```

=====
== Utilization Estimates
=====
* Summary:
+-----+-----+-----+-----+-----+
| Name | BRAM_18K | DSP | FF | LUT | URAM |
+-----+-----+-----+-----+-----+
| DSP | - | - | - | - | - |
| Expression | - | - | 0 | 40 | - |
| FIFO | - | - | - | - | - |
| Instance | 0 | 33 | 1467 | 2466 | 0 |
| Memory | - | - | - | - | - |
| Multiplexer | - | - | - | 175 | - |
| Register | - | - | 650 | - | - |
+-----+-----+-----+-----+-----+
| Total | 0 | 33 | 2117 | 2681 | 0 |
+-----+-----+-----+-----+-----+
| Available | 288 | 1248 | 234240 | 117120 | 64 |
+-----+-----+-----+-----+-----+
| Utilization (%) | 0 | 2 | ~0 | 2 | 0 |
+-----+-----+-----+-----+-----+

```

➤ Interface

```
=====
== Interface
=====
* Summary:
```

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_control_AWVALID	in	1	s_axi	control	array
s_axi_control_AWREADY	out	1	s_axi	control	array
s_axi_control_AWADDR	in	7	s_axi	control	array
s_axi_control_WVALID	in	1	s_axi	control	array
s_axi_control_WREADY	out	1	s_axi	control	array
s_axi_control_WDATA	in	32	s_axi	control	array
s_axi_control_WSTRB	in	4	s_axi	control	array
s_axi_control_ARVALID	in	1	s_axi	control	array
s_axi_control_ARREADY	out	1	s_axi	control	array
s_axi_control_ARADDR	in	7	s_axi	control	array
s_axi_control_RVALID	out	1	s_axi	control	array
s_axi_control_RREADY	in	1	s_axi	control	array
s_axi_control_RDATA	out	32	s_axi	control	array
s_axi_control_RRESP	out	2	s_axi	control	array
s_axi_control_BVALID	out	1	s_axi	control	array
s_axi_control_BREADY	in	1	s_axi	control	array
s_axi_control_BRESP	out	2	s_axi	control	array
ap_clk	in	1	ap_ctrl_hs	fir_n11_maxi	return value
ap_rst_n	in	1	ap_ctrl_hs	fir_n11_maxi	return value
interrupt	out	1	ap_ctrl_hs	fir_n11_maxi	return value
m_axi_gmem_AWVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_AWADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_AWID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_AWSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_AWBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_AWLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_AWCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_AWPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_AWQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_AWREGION	out	4	m_axi	gmem	pointer

m_axi_gmem_AWUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_WVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_WREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_WDATA	out	32	m_axi	gmem	pointer
m_axi_gmem_WSTRB	out	4	m_axi	gmem	pointer
m_axi_gmem_WLAST	out	1	m_axi	gmem	pointer
m_axi_gmem_WID	out	1	m_axi	gmem	pointer
m_axi_gmem_WUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_ARVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_ARADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_ARID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_ARSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_ARBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_ARLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_ARCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_ARPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_ARQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_ARREGION	out	4	m_axi	gmem	pointer
m_axi_gmem_ARUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_RVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_RREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_RDATA	in	32	m_axi	gmem	pointer
m_axi_gmem_RLAST	in	1	m_axi	gmem	pointer
m_axi_gmem_RID	in	1	m_axi	gmem	pointer
m_axi_gmem_RUSER	in	1	m_axi	gmem	pointer
m_axi_gmem_RRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_BREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_BRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BID	in	1	m_axi	gmem	pointer
m_axi_gmem_BUSER	in	1	m_axi	gmem	pointer

➤ Co-simulation transcript/waveform

Synthesis Summary(solution1) | FIR.cpp | Co-simulation Report(solution1) x

Cosimulation Report for 'fir_n11_maxi'

General Information

Date: Sat 30 Sep 2023 04:39:29 AM EDT
Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
Project: hls FIRN11MAXI
Status: **Pass**

Solution: solution1 (Vivado IP Flow Target)
Product family: zynqplus
Target device: xck26-fvc784-2LV-c

Cosim Options

Tool: Vivado XSIM
RTL: Verilog
Dump Trace: all

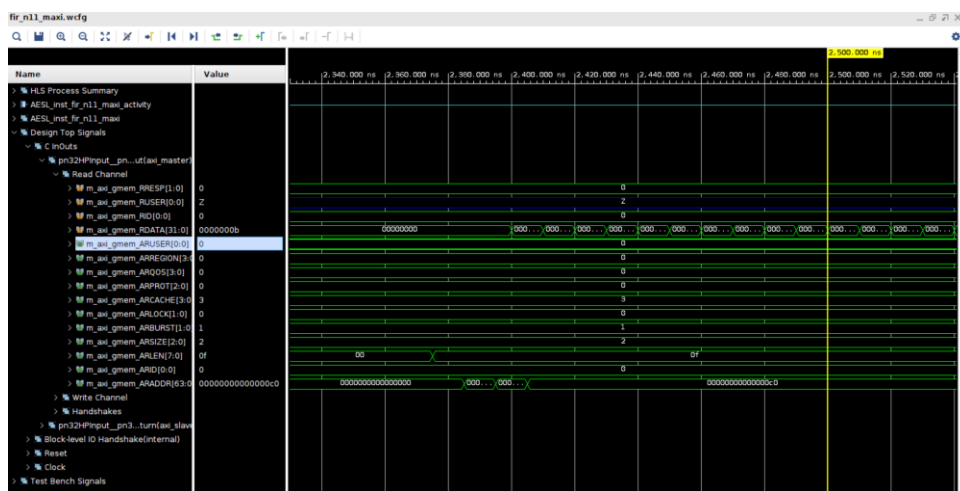
Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
o fir_n11_maxi	724	724	724			

Console | Errors | Warnings | Guidance | Properties | Man Pages | Git Repositories | Modules/Loops

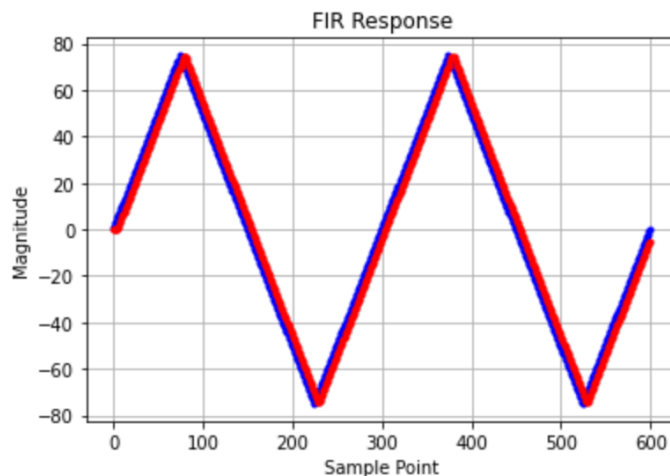
Vitis HLS Console

```
>> Comparing against output data...  
>> Test passed!  
.....  
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***  
INFO: [COSIM 212-211] It is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as all NA. If user  
INFO: [HLS 200-111] Finished Command cosim design CPU user time: 22.45 seconds, CPU system time: 3.51 seconds, Elapsed time: 61.13 seconds; current allocat  
INFO: [HLS 200-112] Total CPU user time: 26.69 seconds, Total CPU system time: 5.97 seconds, Total elapsed time: 93.04 seconds; peak allocated memory: 476.  
Finished C/RTL cosimulation.
```



➤ Jupyter Notebook execution results

Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0002689361572265625 s



=====
Exit process

5. SCREEN DUMPS(FIRN11Stream)

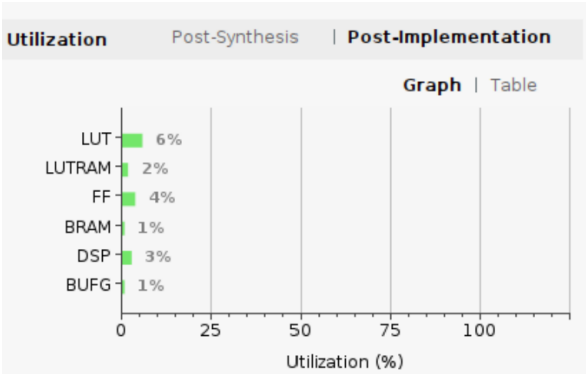
➤ PERFORMANCE(FROM fir_n11_maxi_csynth.RPT)

```
=====
== Performance Estimates
=====
+ Timing:
+ * Summary:
+-----+-----+-----+-----+
+ | Clock | Target | Estimated | Uncertainty |
+-----+-----+-----+-----+
+ | ap_clk | 10.00 ns | 6.290 ns | 2.70 ns |
+-----+-----+-----+-----+

+ Latency:
+ * Summary:
+-----+-----+-----+-----+
+ | Latency (cycles) | Latency (absolute) | Interval | Pipeline |
+-----+-----+-----+-----+
+ | min | max | min | max | min | max | Type |
+-----+-----+-----+-----+
+ | 16 | 11016 | 0.160 us | 0.110 ms | 17 | 11017 | no |
+-----+-----+-----+-----+

+ Detail:
+ * Instance:
+-----+-----+-----+-----+
+ | Interval | Pipeline | Instance | Module | Latency (cycles) | Latency (absolute) |
+-----+-----+-----+-----+
+ | min | max | Type | | min | max | min | max |
+-----+-----+-----+-----+
+ | grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112 | fir_n11_strm_Pipeline_XFER_LOOP | 13 | 11013 | 0.130 us | 0.110 ms | 13 | 11013 | no |
+-----+-----+-----+-----+
+ * Loop:
+-----+-----+-----+-----+
+ | N/A |
+-----+-----+-----+-----+
```

➤ UTILIZATION(FROM VIVADO & fir_n11_maxi_csynth.RPT)



```
-----
-- Utilization Estimates
-----
+ Summary:
+-----+-----+-----+-----+
+ | Name | BRAM_1BK | DSP | FF | LUT | URAM |
+-----+-----+-----+-----+
+ | DSP | - | - | - | - | - |
+ | Expression | - | - | 0 | 42 | - |
+ | FIFO | - | - | - | - | - |
+ | Instance | 0 | 33 | 916 | 1005 | 0 |
+ | Memory | - | - | - | - | - |
+ | Multiplexer | - | - | - | 35 | - |
+ | Register | - | - | 36 | - | - |
+-----+-----+-----+-----+
+ | Total | 0 | 33 | 952 | 1882 | 0 |
+-----+-----+-----+-----+
+ | Available | 288 | 1248 | 234240 | 117120 | 64 |
+-----+-----+-----+-----+
+ | Utilization (%) | 0 | 2 | ~0 | ~0 | 0 |
+-----+-----+-----+-----+

+ Detail:
+ * Instance:
+-----+-----+-----+-----+
+ | Instance | Module | BRAM_1BK | DSP | FF | LUT | URAM |
+-----+-----+-----+-----+
+ | control_s_axi_U | control_s_axi | 0 | 0 | 154 | 180 | 0 |
+ | grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112 | fir_n11_strm_Pipeline_XFER_LOOP | 0 | 33 | 762 | 825 | 0 |
+ | Total | 0 | 33 | 916 | 1005 | 0 |
+-----+-----+-----+-----+
+ * DSP:
+-----+-----+-----+-----+
+ | N/A |
+-----+-----+-----+-----+
+ * Memory:
+-----+-----+-----+-----+
+ | N/A |
+-----+-----+-----+-----+
+ * FIFO:
+-----+-----+-----+-----+
+ | N/A |
+-----+-----+-----+-----+
```

```
+ Expression:
+-----+-----+-----+-----+
+ | Variable Name | Operation | DSP | FF | LUT | Bitwidth P0 | Bitwidth P1 |
+-----+-----+-----+-----+
+ | ret_V_fu_171_p2 | + | 0 | 0 | 40 | 33 | 2 |
+ | grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_pstrmOutput_TREADY | and | 0 | 0 | 2 | 1 | 1 |
+ | Total | | 0 | 0 | 42 | 34 | 3 |
+-----+-----+-----+-----+

+ Multiplexer:
+-----+-----+-----+-----+
+ | Name | LUT | Input Size | Bits | Total Bits |
+-----+-----+-----+-----+
+ | ap_CS_fsm | 26 | 5 | 1 | 5 |
+ | pstrmInput_TREADY_int_regslice | 9 | 2 | 1 | 2 |
+ | Total | 35 | 7 | 2 | 7 |
+-----+-----+-----+-----+

+ Register:
+-----+-----+-----+-----+
+ | Name | FF | LUT | Bits | Const Bits |
+-----+-----+-----+-----+
+ | ap_CS_fsm | 4 | 0 | 4 | 0 |
+ | grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_ap_start_reg | 1 | 0 | 1 | 0 |
+ | tmp_reg_187 | 31 | 0 | 31 | 0 |
+ | Total | 36 | 0 | 36 | 0 |
+-----+-----+-----+-----+
```

➤ Interface

```
-- Interface
```

* Summary:						
RTL Ports	Dir	Bits	Protocol	Source Object	C Type	
s_axi_control_AWVALID	in	1	s_axi	control	array	
s_axi_control_AWREADY	out	1	s_axi	control	array	
s_axi_control_AWADDR	in	7	s_axi	control	array	
s_axi_control_WVALID	in	1	s_axi	control	array	
s_axi_control_WREADY	out	1	s_axi	control	array	
s_axi_control_WDATA	in	32	s_axi	control	array	
s_axi_control_WSTRB	in	4	s_axi	control	array	
s_axi_control_ARVALID	in	1	s_axi	control	array	
s_axi_control_ARREADY	out	1	s_axi	control	array	
s_axi_control_ARADDR	in	7	s_axi	control	array	
s_axi_control_RVALID	out	1	s_axi	control	array	
s_axi_control_RREADY	in	1	s_axi	control	array	
s_axi_control_RDATA	out	32	s_axi	control	array	
s_axi_control_RRESP	out	2	s_axi	control	array	
s_axi_control_BVALID	out	1	s_axi	control	array	
s_axi_control_BREADY	in	1	s_axi	control	array	
s_axi_control_BRESP	out	2	s_axi	control	array	
ap_clk	in	1	ap_ctrl_hs	fir_n11_strm	return value	
ap_rst_n	in	1	ap_ctrl_hs	fir_n11_strm	return value	
interrupt	out	1	ap_ctrl_hs	fir_n11_strm	return value	
pstrmInput_TDATA	in	32	axis	pstrmInput_V_data_V	pointer	
pstrmInput_TVALID	in	1	axis	pstrmInput_V_dest_V	pointer	
pstrmInput_TREADY	out	1	axis	pstrmInput_V_dest_V	pointer	
pstrmInput_TDEST	in	1	axis	pstrmInput_V_dest_V	pointer	
pstrmInput_TKEEP	in	4	axis	pstrmInput_V_keep_V	pointer	
pstrmInput_TSTRB	in	4	axis	pstrmInput_V_strb_V	pointer	
pstrmInput_TUSER	in	1	axis	pstrmInput_V_user_V	pointer	
pstrmInput_TLAST	in	1	axis	pstrmInput_V_last_V	pointer	
pstrmInput_TID	in	1	axis	pstrmInput_V_id_V	pointer	
pstrmOutput_TDATA	in	32	axis	pstrmOutput_V_data_V	pointer	
pstrmOutput_TVALID	out	1	axis	pstrmOutput_V_dest_V	pointer	
pstrmOutput_TREADY	in	1	axis	pstrmOutput_V_dest_V	pointer	
pstrmOutput_TDEST	out	1	axis	pstrmOutput_V_dest_V	pointer	
pstrmOutput_TKEEP	out	4	axis	pstrmOutput_V_keep_V	pointer	
pstrmOutput_TSTRB	out	4	axis	pstrmOutput_V_strb_V	pointer	
pstrmOutput_TUSER	out	1	axis	pstrmOutput_V_user_V	pointer	
pstrmOutput_TLAST	out	1	axis	pstrmOutput_V_last_V	pointer	
pstrmOutput_TID	out	1	axis	pstrmOutput_V_id_V	pointer	

➤ Co-simulation transcript/waveform

File Edit Project Solution Window Help

out_gold.dat FIRTester.cpp FIR.cpp FIR.h fir_n11_strm_csim.log Synthesis Summary(solution1) Co-simulation Report(solution1)

Explorer x Module Hier x

- FIRn11Stream
- Includes
- Source
 - FIR.cpp
 - FIR.h
- Test Bench
 - FIRTester.cpp
 - out_gold.dat
- solution1

Flow Navigator x

- C SIMULATION
 - Run C Simulation
 - Reports & Viewers
- C SYNTHESIS
 - Run C Synthesis
 - Reports & Viewers
 - Report
 - Function Call Graph
 - Schedule Viewer
 - Dataflow Viewer
- C/RTL COSIMULATION
 - Run Cosimulation
 - Reports & Viewers

Cosimulation Report for 'fir_n11_strm'

General Information

Date: Sat 30 Sep 2023 01:11:51 PM EDT
Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
Project: FIRn11Stream
Status: Pass

Solution: solution1 (Vivado IP Flow Target)
Product family: zynqplus
Target device: xc7z020-1gsg230e

Cosim Options

Tool: Vivado XSIM
RTL: Verilog
Dump Trace: all

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
0 fir_n11_strm	6603	6603	6603	6603	6603	6603
0 fir_n11_strm Pipeline XFER LOOP	6600	6600	6600	6600	6600	6600

Console Errors Warnings Guidance x Properties Man Pages Git Repositories

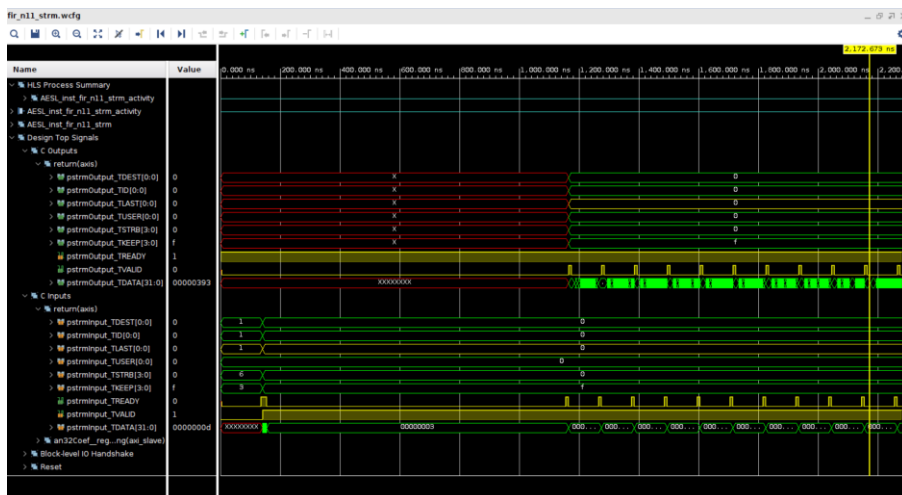
21 Guidance-Infos 7 Guidance-Warnings 0 Guidance-Errors

Name Web Help Details

All Categories

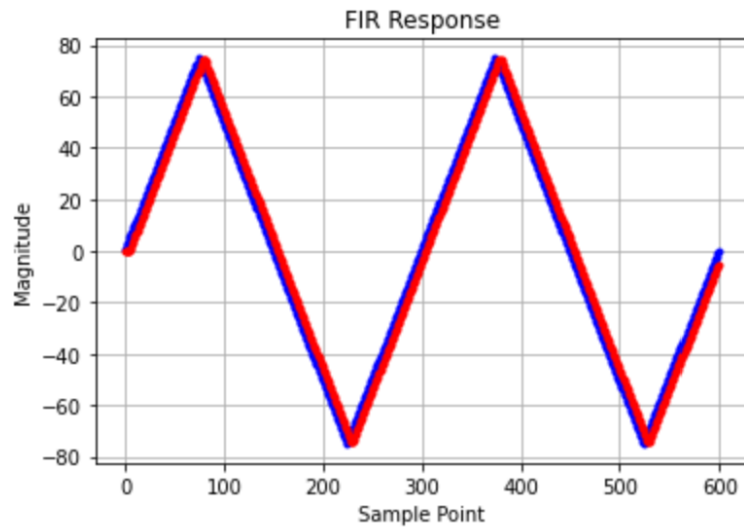
SCHEDULE

solution1 x



➤ Jupyter Notebook execution results

Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0008831024169921875 s



=====
Exit process