112 上學期

系統晶片設計

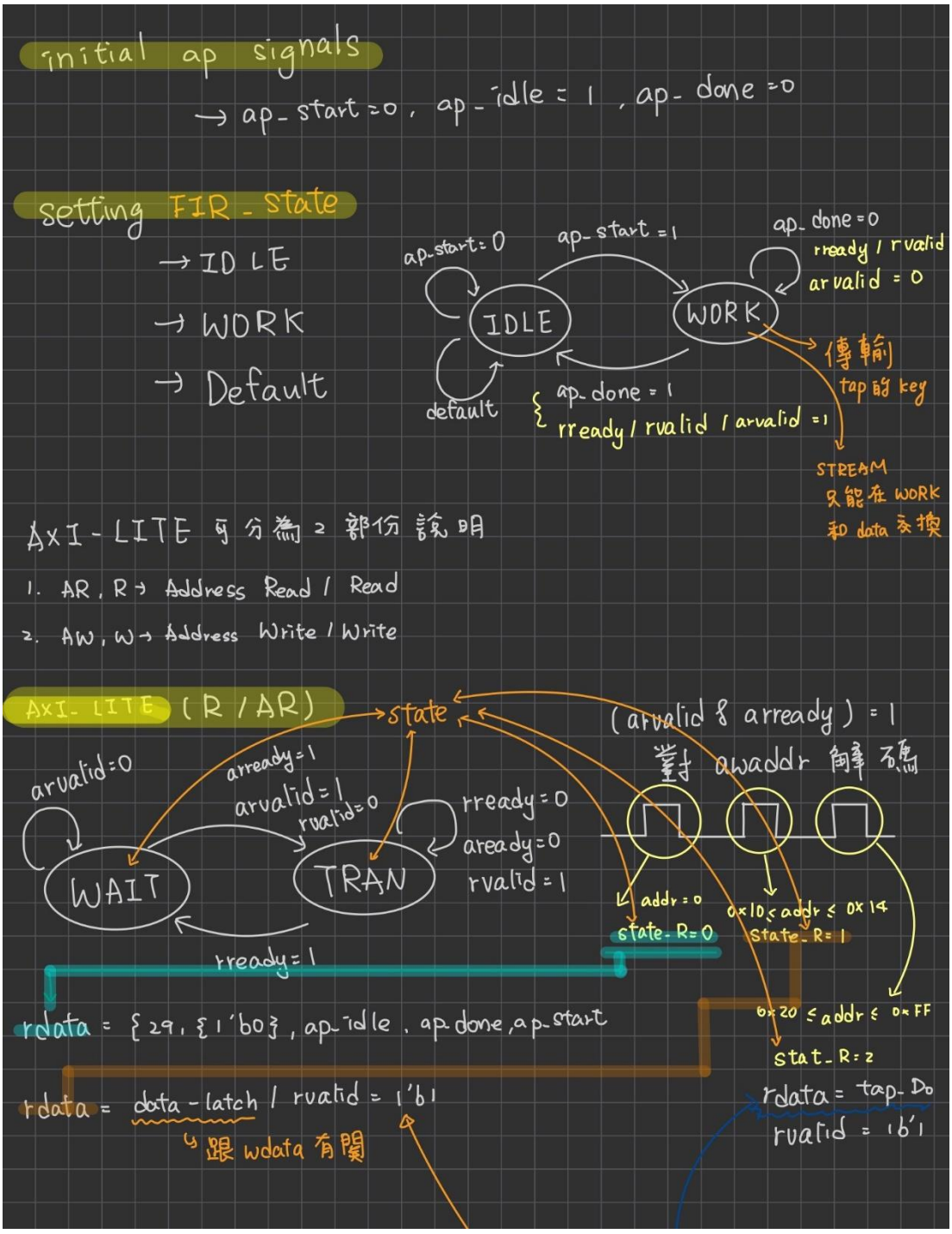
SOC Design Laboratory LAB3

- Block Diagram

架構分為

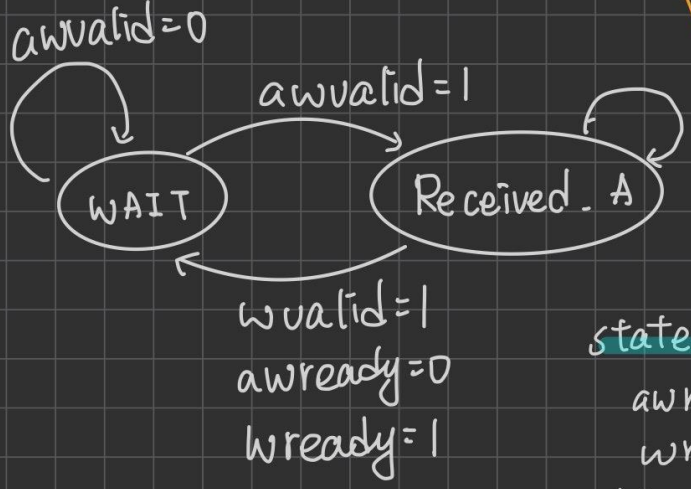
1. BRAM(老師提供)
2. FIR 本體(AXI-LITE + AXI-STREAM+運算)

- Describe operation



AXI-LITE (W/AW)

寫法跟 R/AR 一樣，內部參數更動



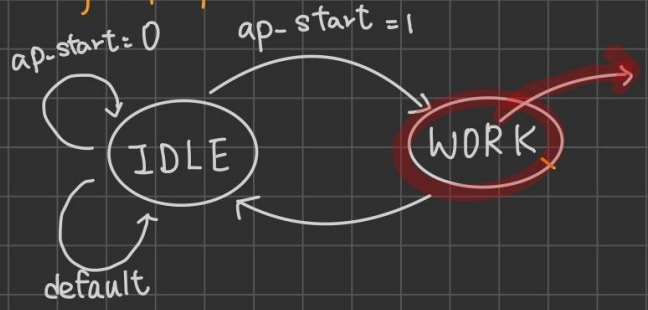
state_w=0
awready=1
wready=0
wdata[0]=1
ap_start=1
↳FIR_LOGIC START

state_w=1
awready=0
wready=1
data_latch=wdata

state_w=2
tap_Di=wdata

因為 ap_start 只要一个 cycle 就要↘

so, 判斷 ap_start FIR_STAT 要跟 W/AW 放一起



if (ap_start && ss_tavlid && ss_tready)
==1 → ap_start=0
other → ap_start=ap_start

Multiplier & Adder

跟 Tap & Data 相關，另外 write a module

notice input → x (Data) 透过 Stream and "Ram point" 可以傳送 有效 Data

input → tap

輸出 Yout → 到 sm_tdata

RAM POINT

因為 AXI-LITE 只可控制 Tap_Din / Tap_Dout
這裡把 Tap ↔ Data connect

Tap number = 11 so count loop 0 ~ 10

設定 data / tap count 的數值，表示記憶体的 size

參数 setting for BRAM

→ tap count << 2 位 for BRAM (tap)

→ data count if " tap count = A"

data count <= data count

<< 2 位 to BRAM (Data)

Tap Write or Read Control

Tap_w_R

01 Read	→ Tap_EN = 1	tap_WE = 4'd0000
10 write	→ Tap_EN = 1	tap_WE = 4'd1111
00 idle	→ tap_EN = 0	tap_WE = 4'd0000

IDLE:

① state_R & W → 2 (表示 Tap in / out)

判斷 W or R 是 R, W, I

→ (wvalid & wready) == 1 ⇝ write

→ (rvalid & rready) == 1 ⇝ Read (01)

other ⇝ idle (00)

(必須要依照有可能的 state 給指令

AXI-STREAM

用來確定 FIR 是否完成

SS_Tready ⟶ 這裡直接看波形圖寫 ss_tdata → Din

data 也是從這裡開始輸入

SM_Tready ⟶ Yout (就是 multipler 跟 Adder 結果)

↳ 輸出到 tdata_sm

一定要在 WORK 的時候

ss, sm 才和 data 交換資訊

- Resource usage: including FF, LUT, BRAM

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	0	0	0	53200	0.00
LUT as Logic	0	0	0	53200	0.00
LUT as Memory	0	0	0	17400	0.00
Slice Registers	0	0	0	106400	0.00
Register as Flip Flop	0	0	0	106400	0.00
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	0	0	0	13300	0.00
SLICEL	0	0			
SLICEM	0	0			
LUT as Logic	0	0	0	53200	0.00
LUT as Memory	0	0	0	17400	0.00
LUT as Distributed RAM	0	0			
LUT as Shift Register	0	0			
Slice Registers	0	0	0	106400	0.00
Register driven from within the Slice	0				
Register driven from outside the Slice	0				
Unique Control Sets	0		0	13300	0.00

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

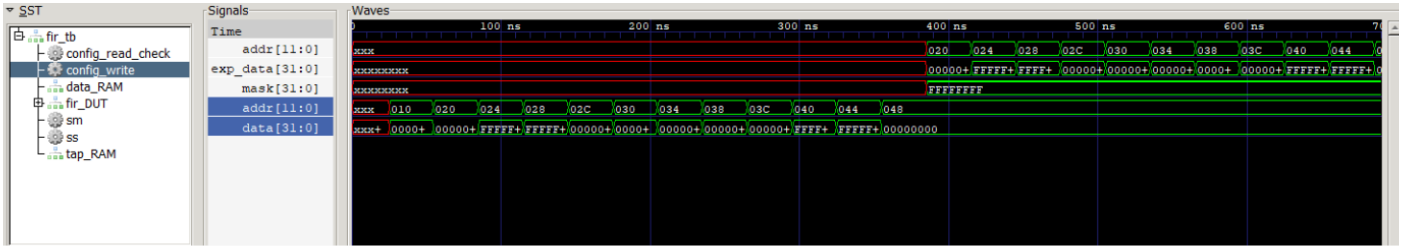
3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

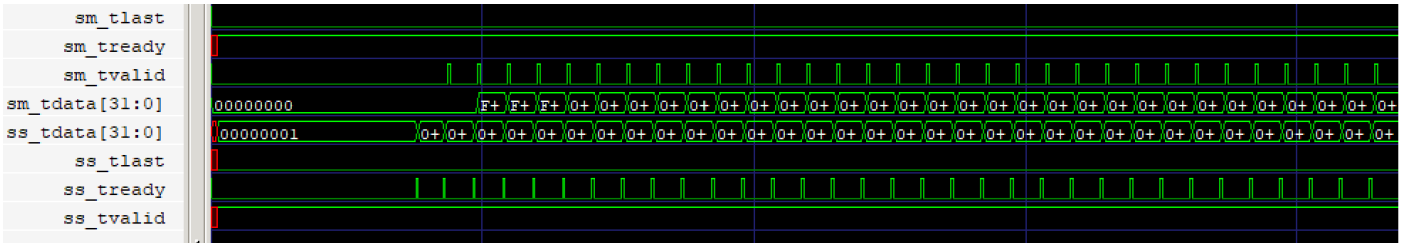
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

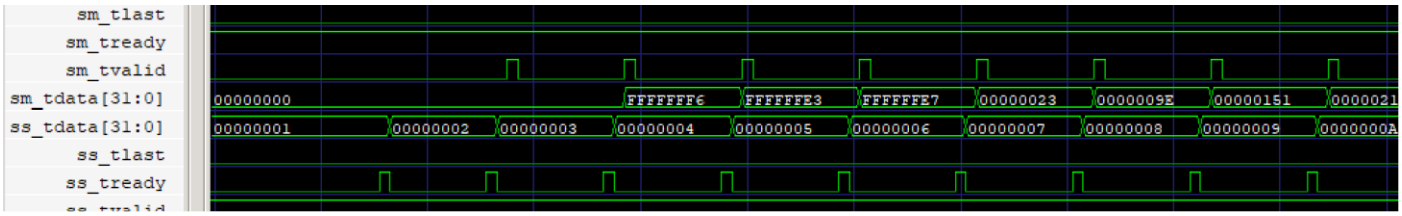
➢ Simulation Waveform, show

Coefficient program, and read back

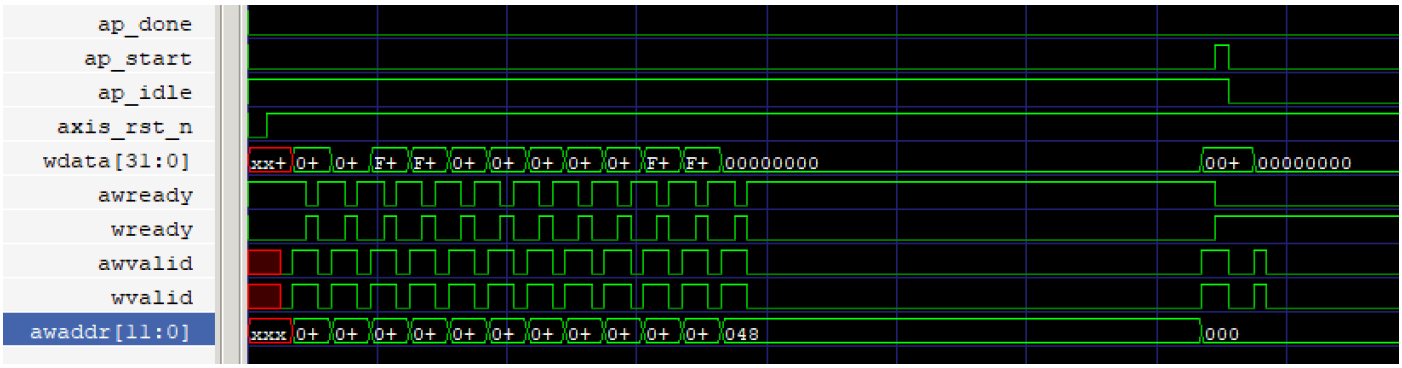


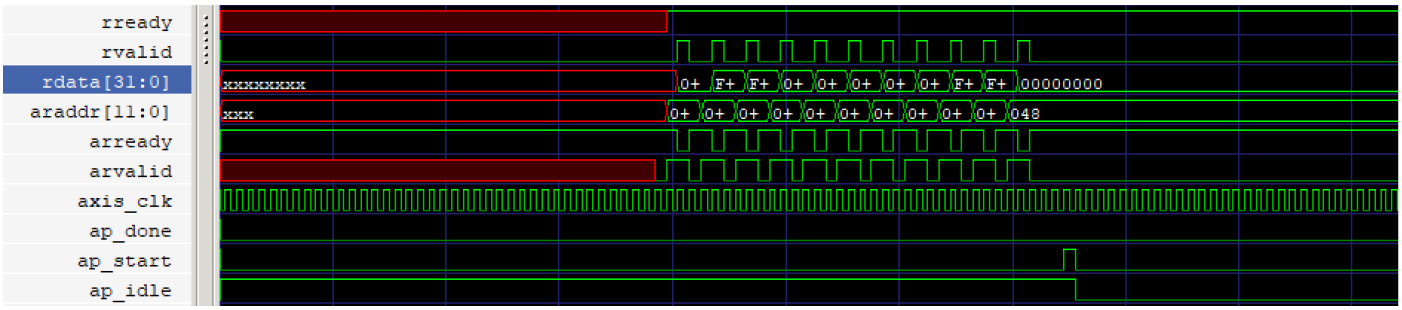
AXI-STREAM



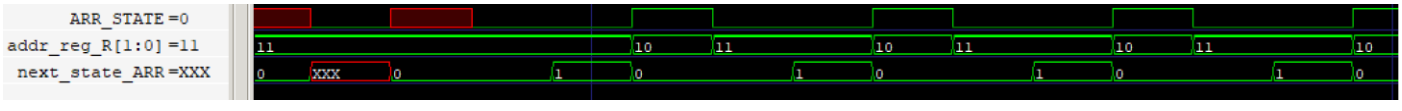


AXI-LITE & AP CONTROL



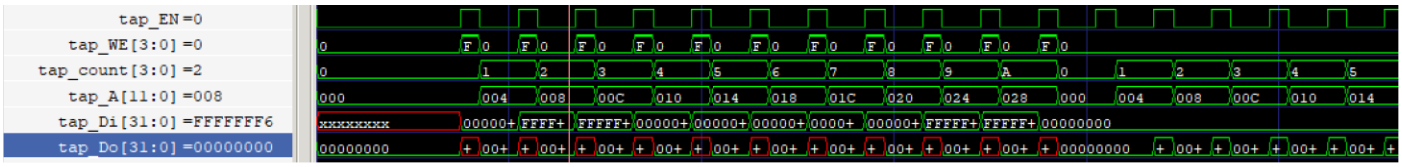


FSM



BRAM:

1. TAP-CONTROL (儲存 FIR 的輸入數據)



2. DATA-RAM (儲存 FIR 的係數(tap coefficients))