Digital Door Lock – Verilog + Zynq MPSoC (Vivado 2024.1)

Project Overview:

A secure hardware-based digital door lock system implemented using Verilog RTL, FSM, ROM password storage, and an alarm mechanism after consecutive wrong attempts. Integrated with Zynq MPSoC using Vivado IP Integrator.

Features:

- Hardware password verification
- FSM-based control
- Wrong attempt counter with alarm
- Display output via LEDs/7-Segment
- Vivado block design integration
- Fully synthesizable RTL modules

System Architecture:

Includes keypad input, FSM core, password ROM, and LED status display.

FSM:

IDLE → CHECK → UNLOCKED/WRONG → ALARM (after 3 wrong attempts)

Modules:

- fsm_controller.v: Handles password checking and state transitions
- rom_password.v: Stores fixed password
- status_display.v: LED/7-seg output
- topmodule.v: Integrates all modules

Simulation:

Performed using Icarus/GTKWave. Testbench verifies password entry, wrong attempts, and alarm triggering.

Vivado Integration:

Block design created with PS-PL connection through AXI interconnect. Screenshots included in the project.

Conclusion:

The system successfully implements a secure digital lock with hardware-level password authentication and alarm functionality.