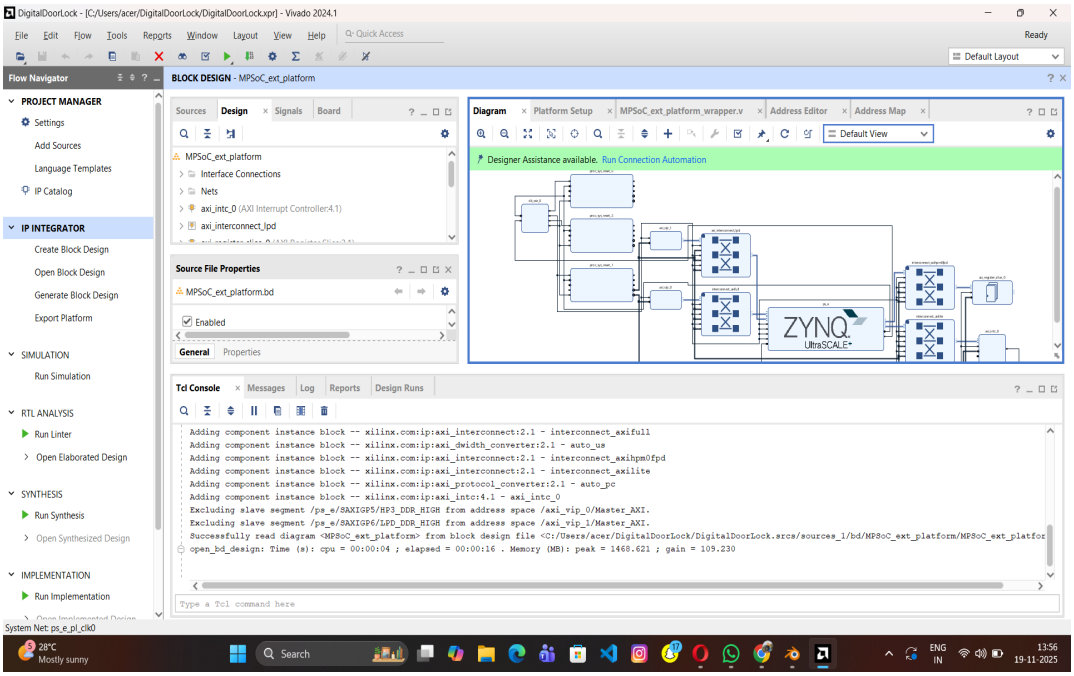
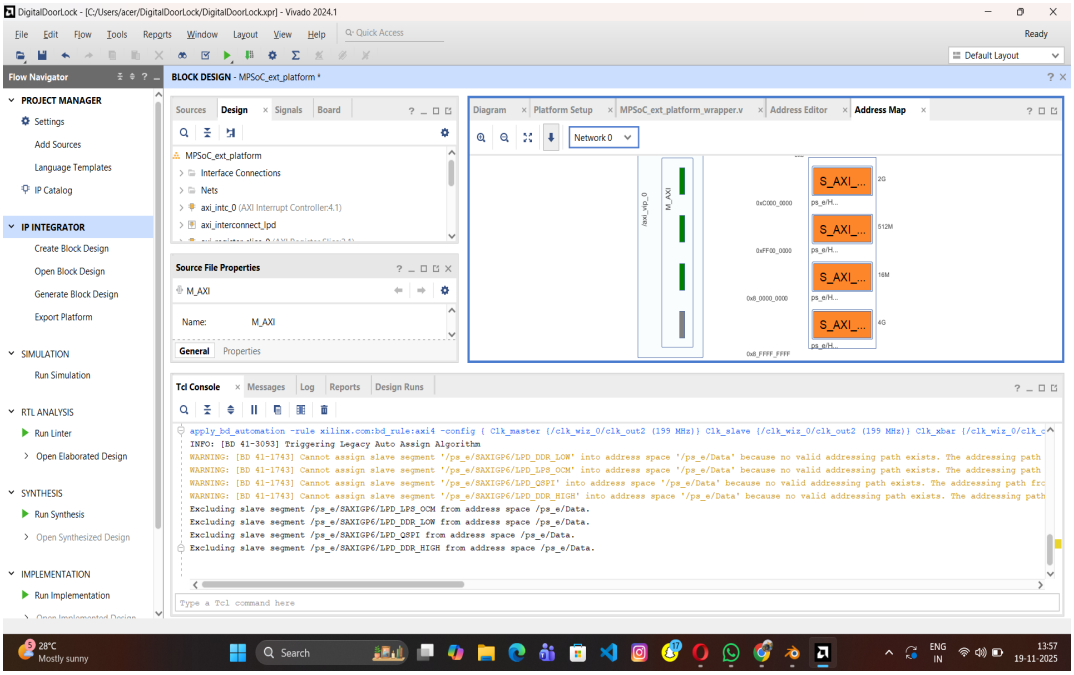
Design and Implementation of a Digital Door Lock System using Zynq UltraScale+ MPSoC

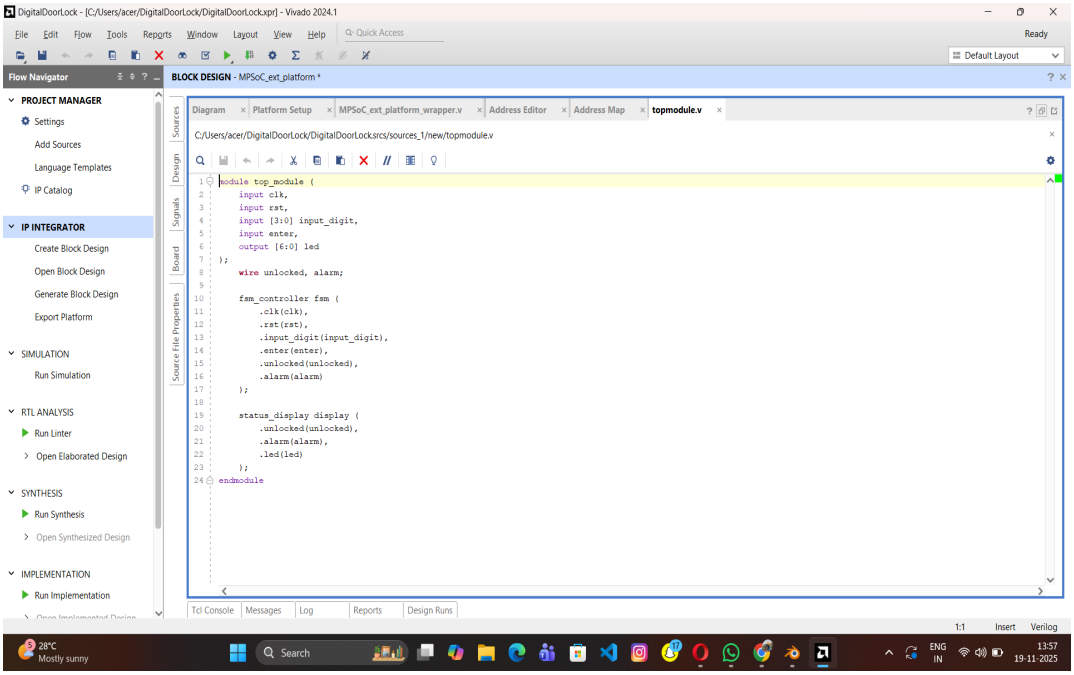
Abstract:
This document details the design and implementation of a secure four-digit Digital Door Lock system utilizing a Finite State Machine (FSM) implemented in Verilog HDL and deployed on a Xilinx Zynq UltraScale+ MPSoC platform. The system integrates the custom hardware logic into the Vivado IP Integrator flow, using AXI interfaces for PS–PL communication.

I. INTRODUCTION
Modern access control systems require secure and high-performance logic implementation. This project uses FPGA-based programmable logic to implement a digital door lock featuring multi-digit authentication using FSM design principles.

II. SYSTEM ARCHITECTURE
The hardware architecture consists of the Zynq UltraScale+ MPSoC, AXI interconnects, custom Verilog logic, and peripheral interfaces. Block design snapshots are included below.







III. HDL DESIGN

The top-level Verilog module integrates the FSM controller and status display units. The FSM handles password validation, and the display unit drives LEDs for UNLOCK and ALARM states.

IV. IMPLEMENTATION RESULTS

Vivado 2024.1 was used for synthesis and implementation. Console logs confirm successful block design validation and address map configuration.

V. CONCLUSION

The project demonstrates the successful integration of custom Verilog FSM logic into a Zynq-based SoC using AXI communication and Vivado IP Integrator.