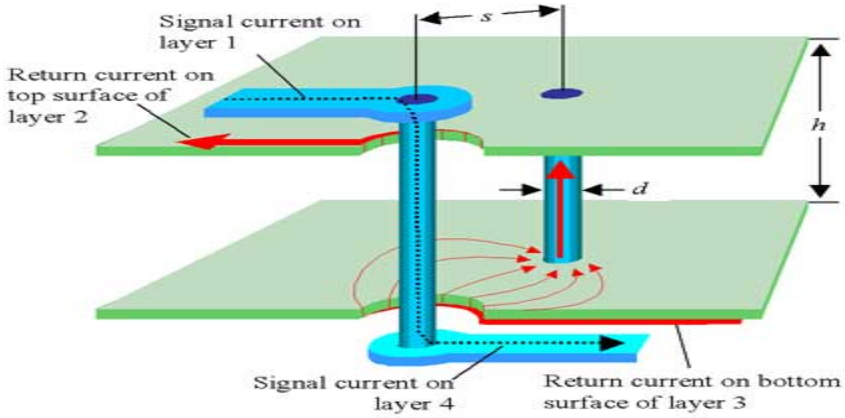
E- Provide an Efficient Path for Current Return:

On high-speed designs, each of your signals is going to seek a route from source to sink along the path of least impedance. For system clocks and other high speed, I/O devices, ensuring this smooth path of travel might require the use of a via. Without these, you might find yourself with currents spreading around splits in your ground plane, and in turn leading to a loss of signal integrity.



If you do find yourself using vias to return your currents to their termination, then make sure you use tightly coupled, impedance matched differential vias to ensure your signals arrive on time. And when placing your return vias, place them as close as possible to your signal vias to minimize the length your signal has to travel.

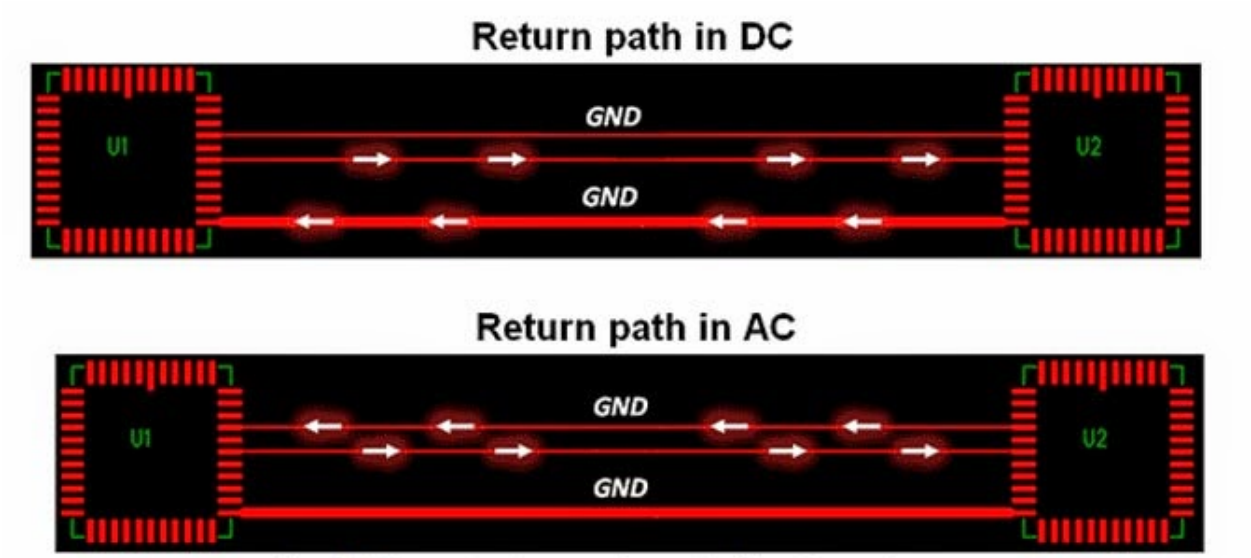


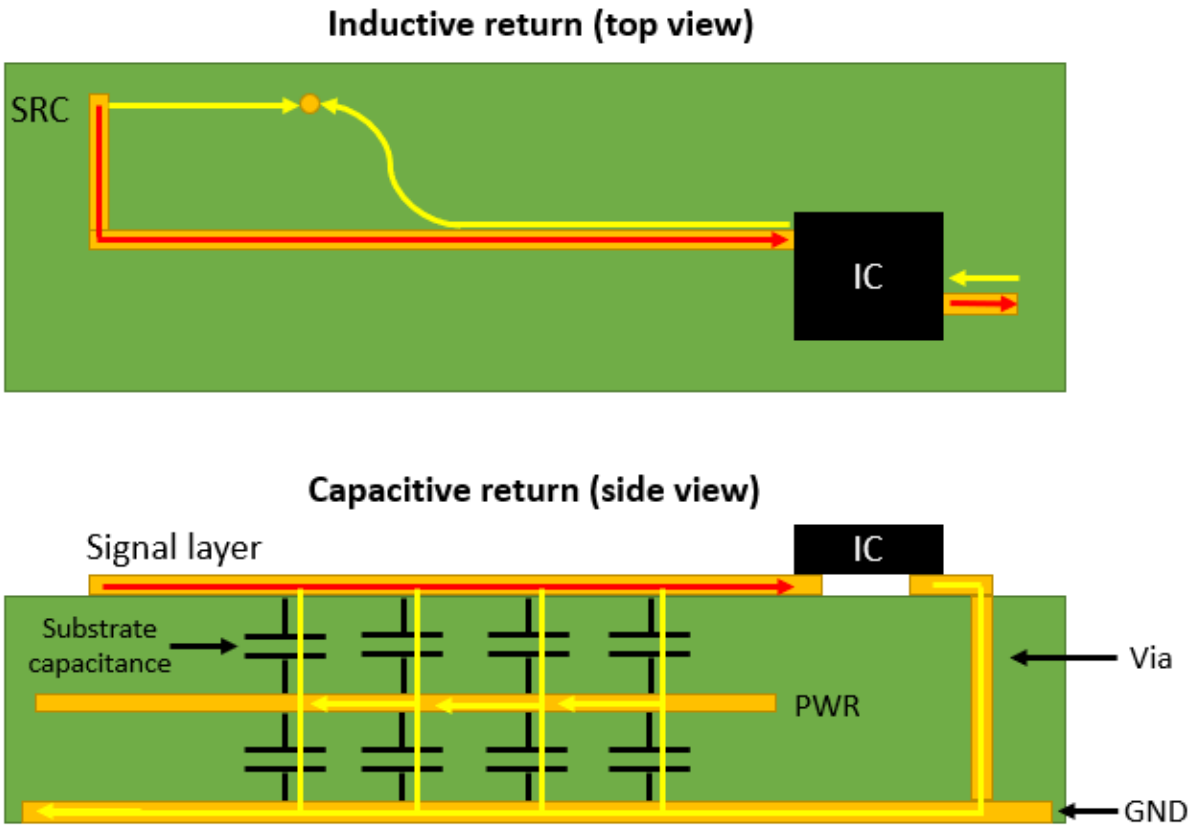
Fig. 5.5 Currents return on the path of least impedance

the return current for a propagating signal depends on the frequency and associated impedance seen by the signal as the electromagnetic field propagates along an interconnect.

Low Frequencies = Inductive Return Current Path

The return current will only follow directly below a trace at all frequencies, as was mentioned above. At low frequencies, the return current is inductively induced in a loop surrounding the circuit. This creates the apparent straight-line path at low frequencies shown in the above figure (left panel). In reality, there is a current loop beneath the trace that extends throughout the reference plane.

High Frequencies = Capacitive Return Current Path
In contrast, at sufficiently high frequencies, the capacitive nature of the PCB return current path will dominate. This is because there is stray capacitance between a trace and all nearby reference planes. The closest reference plane will have the highest parasitic capacitance and thus the lowest impedance. Therefore, the majority of the return current will be induced as a displacement current in the nearest reference plane at higher frequencies.



Designing a PCB Return Current Path

The return current path in a PCB is not something to be deliberately designed at every frequency. Instead, some simple stackup and layout choices will determine whether you can properly direct the return path in your PCB such that there is no interference between signals.

Use Adjacent Reference Planes

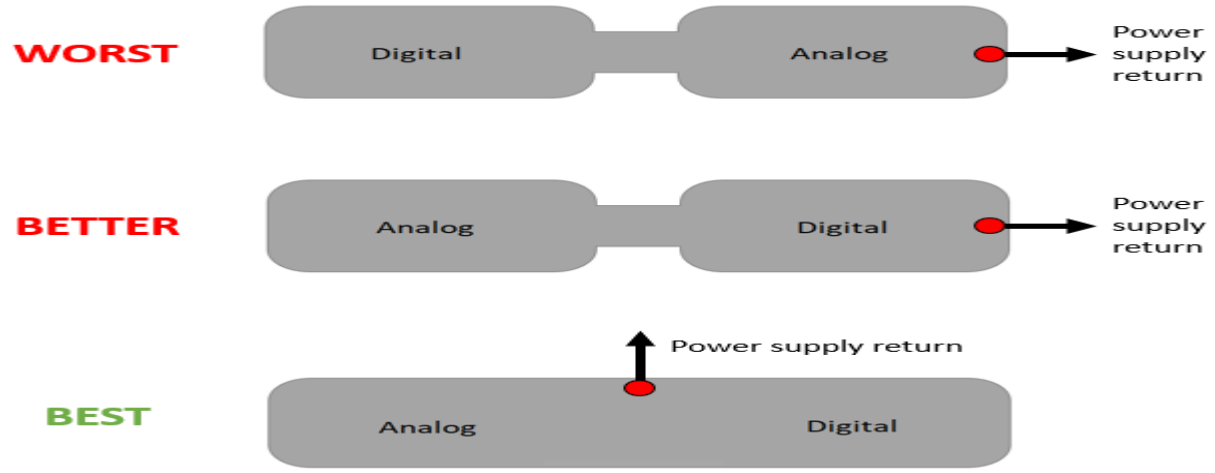
If you look at the examples with inductive and capacitive return paths above, you'll see that the use of an adjacent ground plane is the best way to provide a predictable return path. Otherwise, your signals will try to couple inductively or capacitively back to the nearest return plane. This then can cause interference as the return current path establishes itself between power, signal, and finally ground layers. Instead, provide an adjacent ground plane for return signals to prevent unintended coupling.

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	SM-002	Solder Mask		1mil	4	0.03
	Top Copper Plat...	PbSn	Copper plating		0.787mil		
1	Top Signal	CF-004	Signal	1oz	1.378mil		
	Dielectric 4	PP-006	Prepreg		2.8mil	4.1	0.02
2	Ground1	CF-004	Plane	1oz	1.378mil		
	Dielectric 2	PP-006	Prepreg		2.8mil	4.1	0.02
3	Power	CF-004	Plane	1oz	1.378mil		
	Dielectric 1	Core-009	Core		4mil	4.5	0.02
4	Power or Ground	CF-004	Plane	1oz	1.378mil		
	Dielectric 3	PP-006	Prepreg		2.8mil	4.1	0.02
5	Ground2	CF-004	Plane	1oz	1.378mil		
	Dielectric 5	PP-006	Prepreg		2.8mil	4.1	0.02
6	Bottom Signal	CF-004	Signal	1oz	1.378mil		
	Bottom Copper...	PbSn	Copper plating		0.787mil		
	Bottom Solder	SM-002	Solder Mask		1mil	4	0.03
	Bottom Overlay		Overlay				

Mixed Signal Return Current Paths?

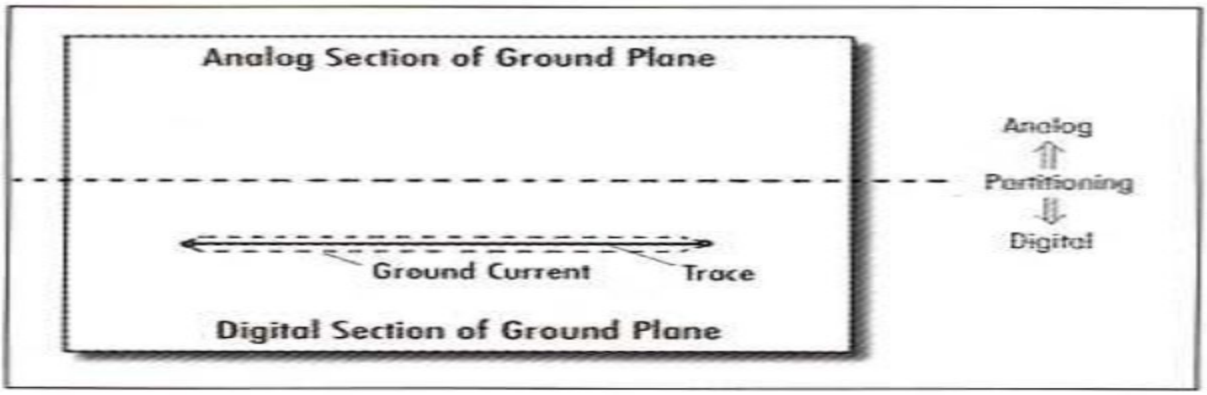
With mixed signal boards, controlling your return current paths is even more critical as you should try to prevent digital signals from inducing a current in analog sections of the board. Splitting your layout into analog and digital sections goes a long way towards reducing mixed signal crosstalk.

When I say "section," I am not talking about cutting a ground layer into two pieces and then routing signals over the gap (don't do this!!!!). I simply mean arrange analog components with each other in one region of the board, and arrange the digital components together in another region of the board. The goal is to prevent the digital signals from travelling beneath the analog region and causing interference.



what sort of benefits does split ground give you over a single? Less noise? more stable?

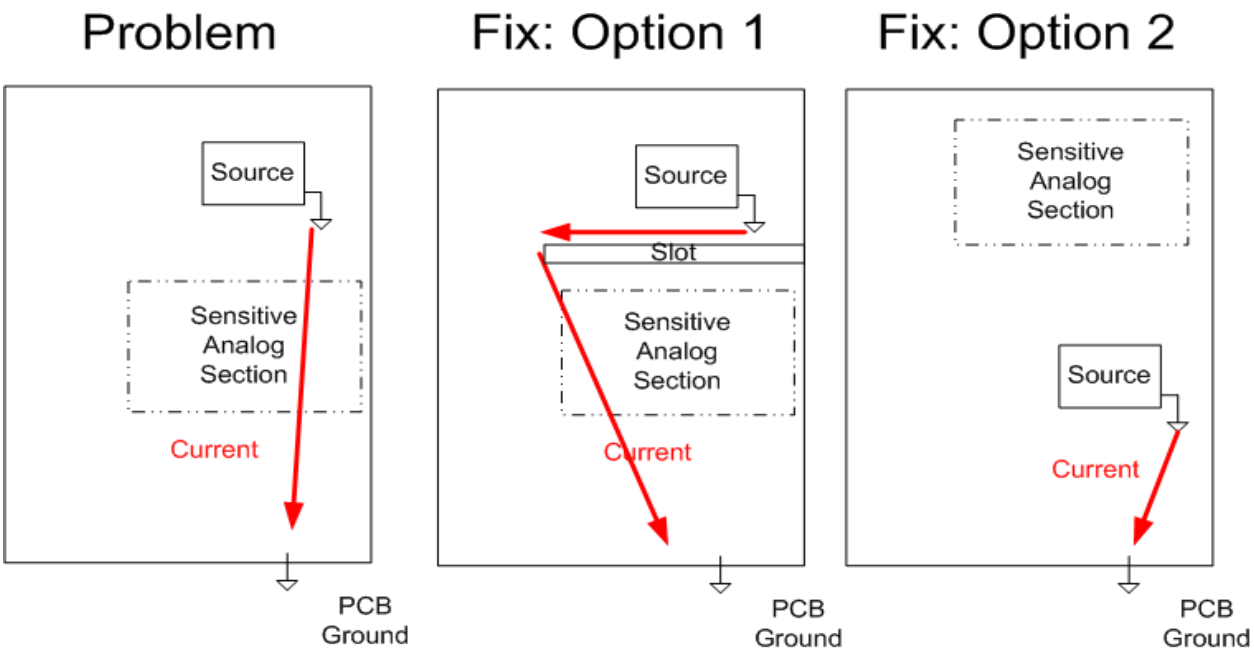
I don't; I keep the planes as continuous as possible and almost never use slots - they are bad for a few reasons which I will describe. I manage the return currents with the placement of components.



Once, I had a return current running through a sensitive analog section, and it was causing my signal to shift by 10%. The source was from a circuit 'above' the analog section; the path of the return current on the grounding plane needed to change. There are two options:

1) Put a slot in the board and redirect the return current around the section that I wanted to protect.

2) Rearrange the components



Creepage vs. Clearance

Both of these terms are used to define distances between conductors in a PCB layout and are specified in safety standards. Creepage and clearance are defined as the spacing between two neighboring conductors, although they are defined in two different ways.

CLEARANCE:

Clearance is the shortest distance through air between two conductors. I remember its definition by thinking of overhead clearance; how much room in the air before my head whacks into something. If the clearance anywhere on a PCB is too small, then an over-voltage event can cause an arc between neighboring conductive elements on the board.

Clearance is affected by many factors:

Material ,voltage, environmental conditions humidity changes the breakdown voltage of air and affects the likelihood of arcing. Dust is another factor, since particulates that collect on the surface of the PCB can form a track over time, shortening the distance between conductors.

CREEPAGE:

The shortest path between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured along the surface of the insulation (Figure 1). Similar to clearance, creepage measures distance between conductors on for high voltage PCB. However, instead of measuring distance in air, it measures the shortest distance along the surface of the insulation material. Board material and environment also affect creepage requirements. Moisture or particulate accumulation on the board can shorten creepage distance the same way they do for clearance. When you have a high density printed circuit board design, creepage can be a difficult requirement to meet. Since moving tracks is rarely the first choice, there are a couple other tricks for increasing the surface distance in your design. By adding either a slot between tracks, or a vertical barrier of insulation, you can significantly increase the creepage distance without changing the trace layout on the board.

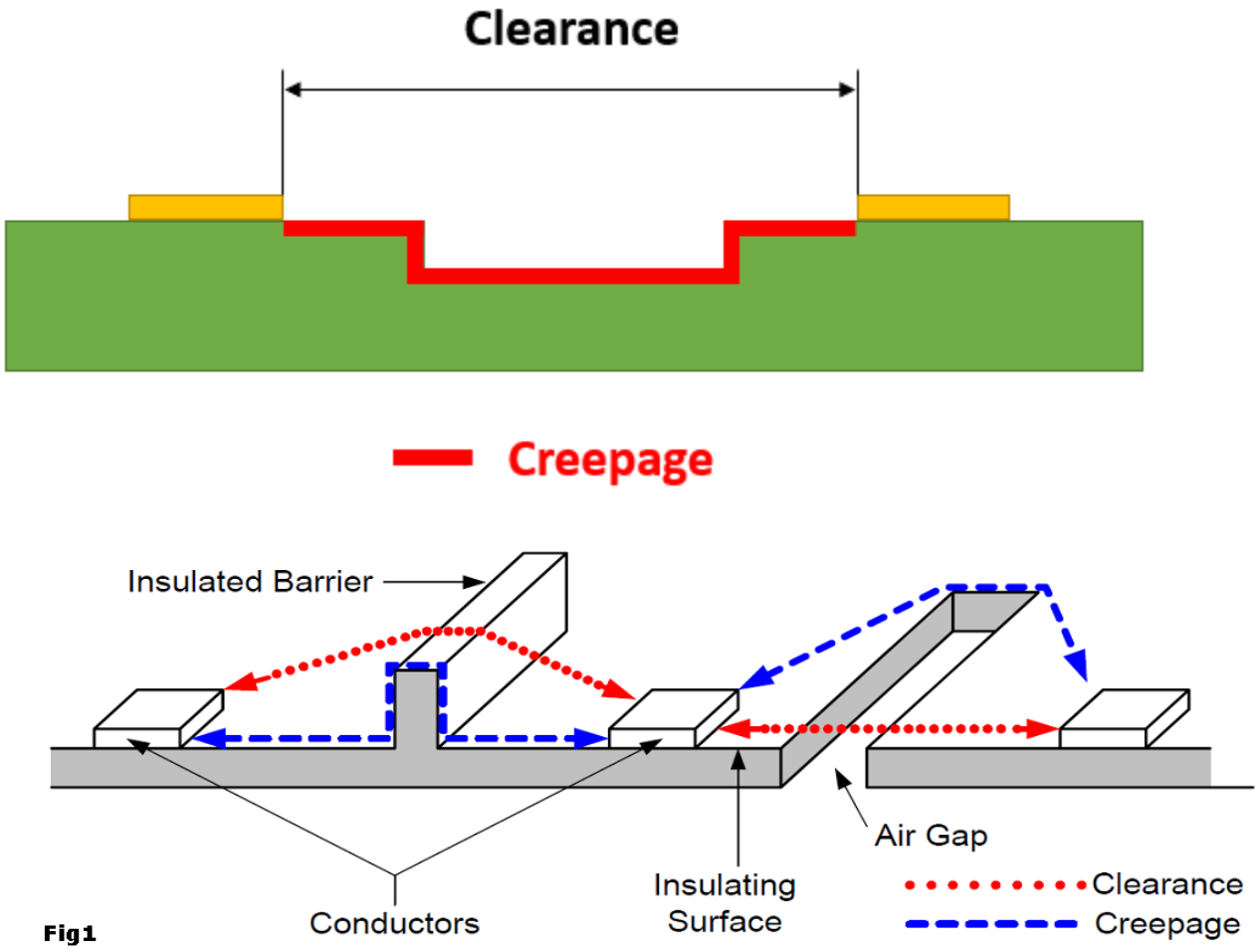


Fig1

The problem with split planes / slots is running traces over them creates problems with the return current. The other problem is unintentional radiating, however a lot of SMPSs are shielded with a case anyway so this may not be a problem if you're planning on shielding.

Conclusion:

DC current. With DC current, the return current path is simply the path of least resistance. This means the current follows a straight line from the source and back to the ground return point. This means the DC current in the ground plane just follows a straight line back to the power supply.

Low frequencies. At low frequencies, a portion of the return current path follows beneath the trace carrying the signal. The current is spread around the trace in a Gaussian-like distribution.

High frequencies. At high frequencies, the return current path closely follows the path beneath the trace.

The best way to ensure a stable return path with low loop inductance is to place a grounded via alongside the signal via during a layer transition. This is the best way to ensure the loop inductance remains small when routing between layers. If you do not do this, the return current will be provided by the zlowest impedance pass which could be the nearest decoupling capacitor, which can create very large loop inductance for the circuit in question.