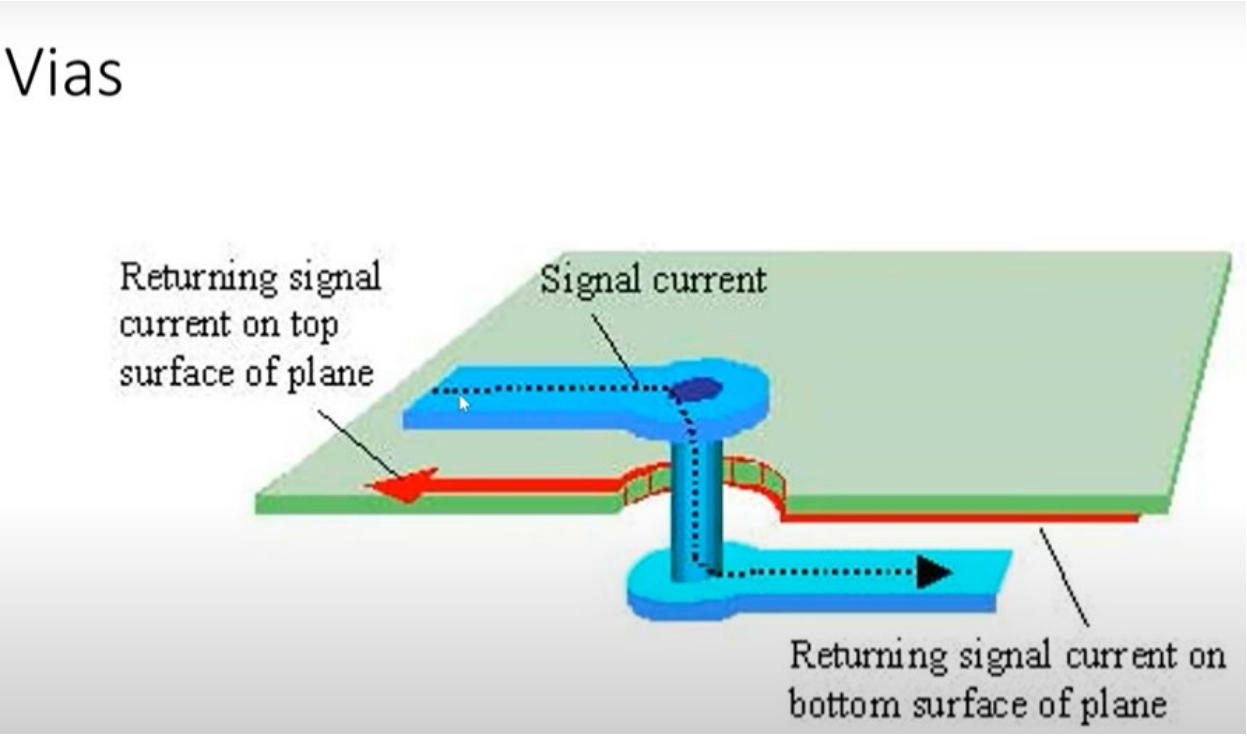
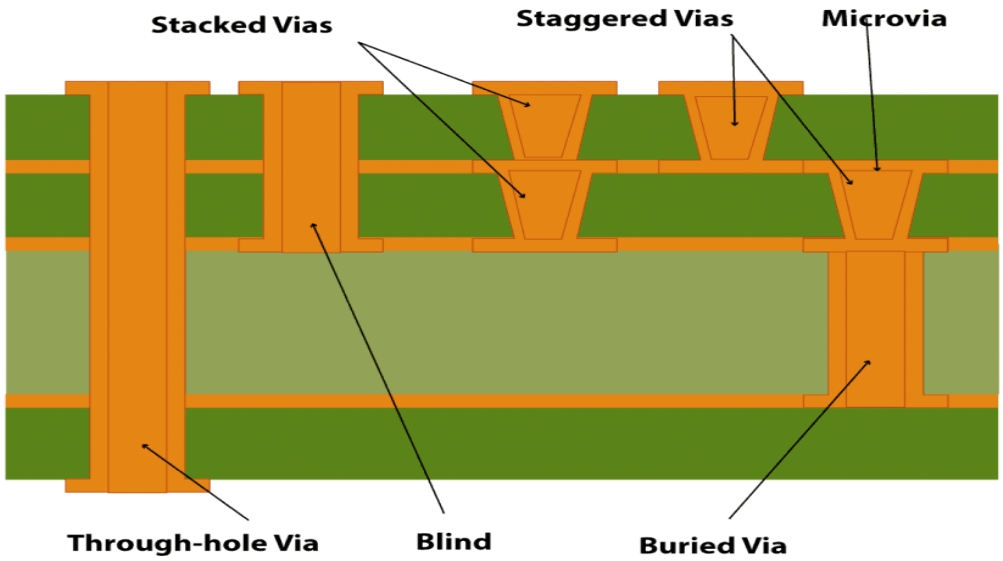
C- PADS AND VIAS:

1-VIAS



Vias when we need to pass from one copper layer another layer which when we have a trace which go through a plated hole (vias) to the wire or trace on the other layer all boards have these things but we do our best to avoids as much as possible through careful layout routing.

Via Types:



Through-hole vias

The hole penetrates from the top layer to the bottom layer. They can be either PTH or NPTH. For PTH, the connection is established from the top to the bottom layer.

Blind Vias

The hole penetrates from an exterior layer and ends at an interior layer. Here, the hole doesn't penetrate through the entire board but connects the PCB's exterior layers to at least one interior layer. Either the connection is from the top layer to a layer in the center or from the bottom layer to some layer in the interior region. The other end of the hole cannot be seen once the lamination is done. Hence, they are called blind vias.

Buried Vias (hidden vias)

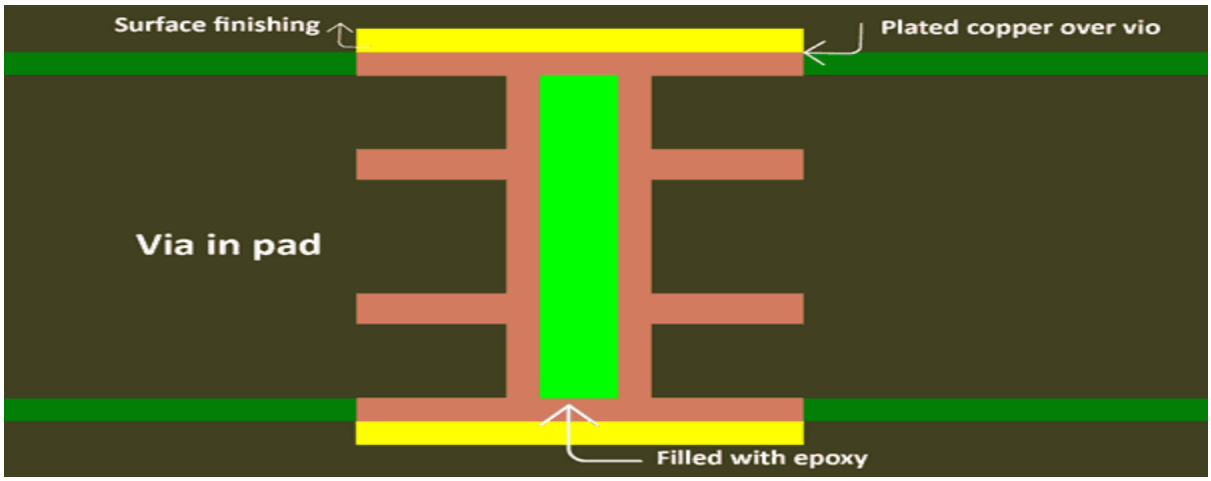
These vias are located in the interior region of the PCB. The buried vias have no paths to the outer layers. They connect the inner layers and stay hidden from sight. As per IPC standards, buried vias and blind vias must be 6 mils (150 micrometers) in diameter or less.

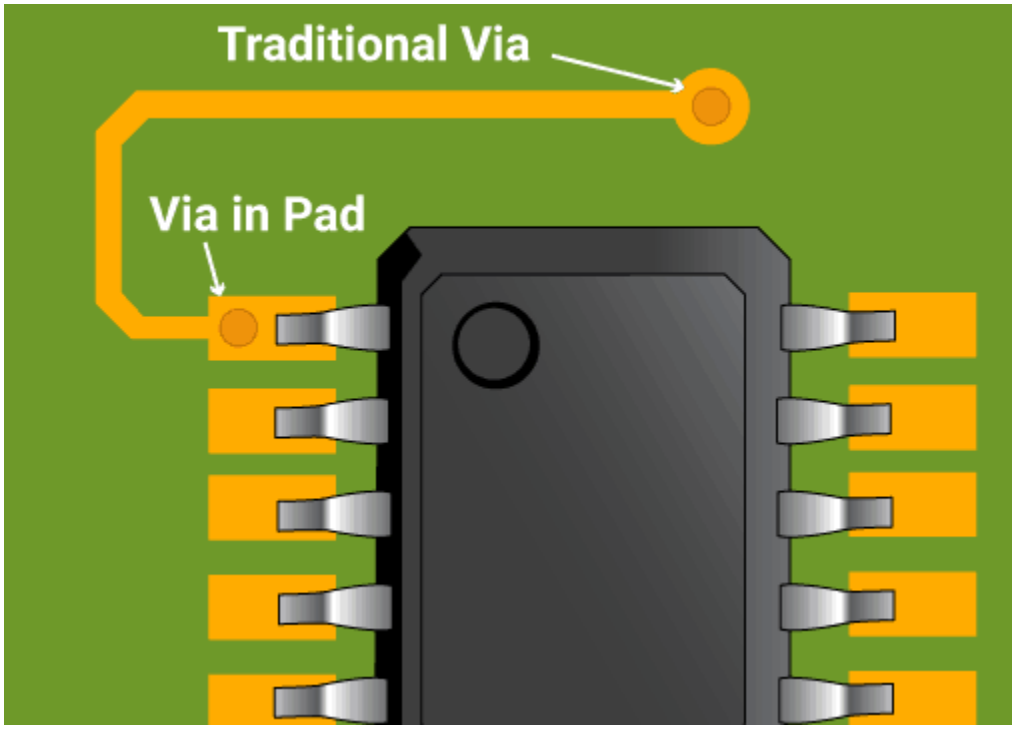
The most commonly known vias are the microvias (μvias). During PCB manufacturing, microvias are drilled by lasers and have a smaller diameter compared to the standard through-hole vias. Microvias are generally implemented in High-Density Interconnection (HDI) PCBs. The depth of a microvia isn't usually more than two layers deep since the plating of copper inside these small vias is a tedious task. The smaller the diameter of a via, the higher should be the throwing power of the plating bath to achieve electroless copper plating.

Microvias can be classified into stacked vias and staggered vias based on their location in the PCB layers.

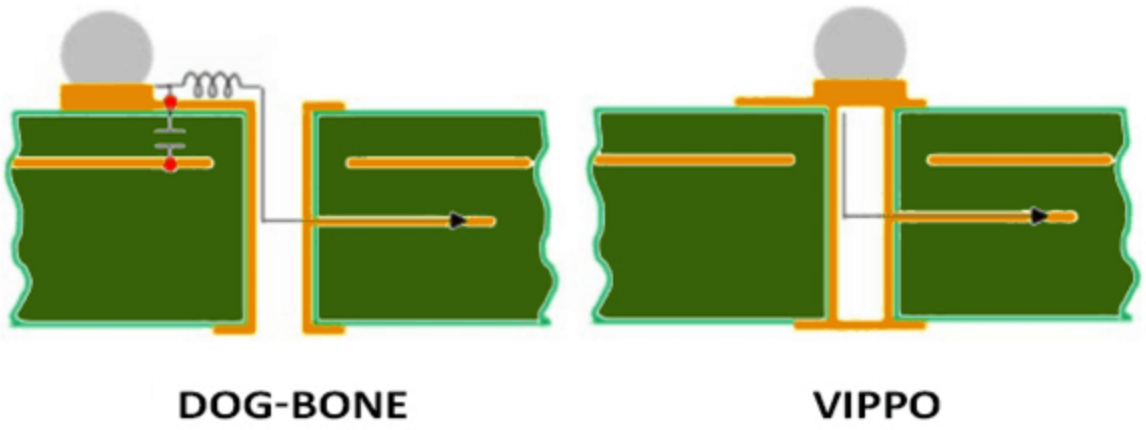
- Stacked vias are piled on top of one another in different layers.
- Staggered vias are scattered in the different layers. And they are more expensive.
- Additionally, there is another type of microvias called skipvias. Skipvias skip one layer, meaning, they pass through a layer making no electrical contact with that specific layer. The skipped layer will not form an electric connection with that via.

Via-In-Pad





in traditional vias, the signal trace is routed away from the pad and then to the via. You can see this in the above diagram. This is done to avoid seepage of the solder paste into the via during the reflow process. In a via-in-pad, the drilled via is present right below a pad. To be precise, the via is placed within the pad of a surface mount component.

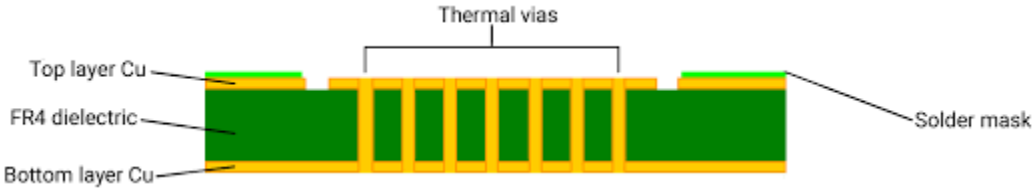


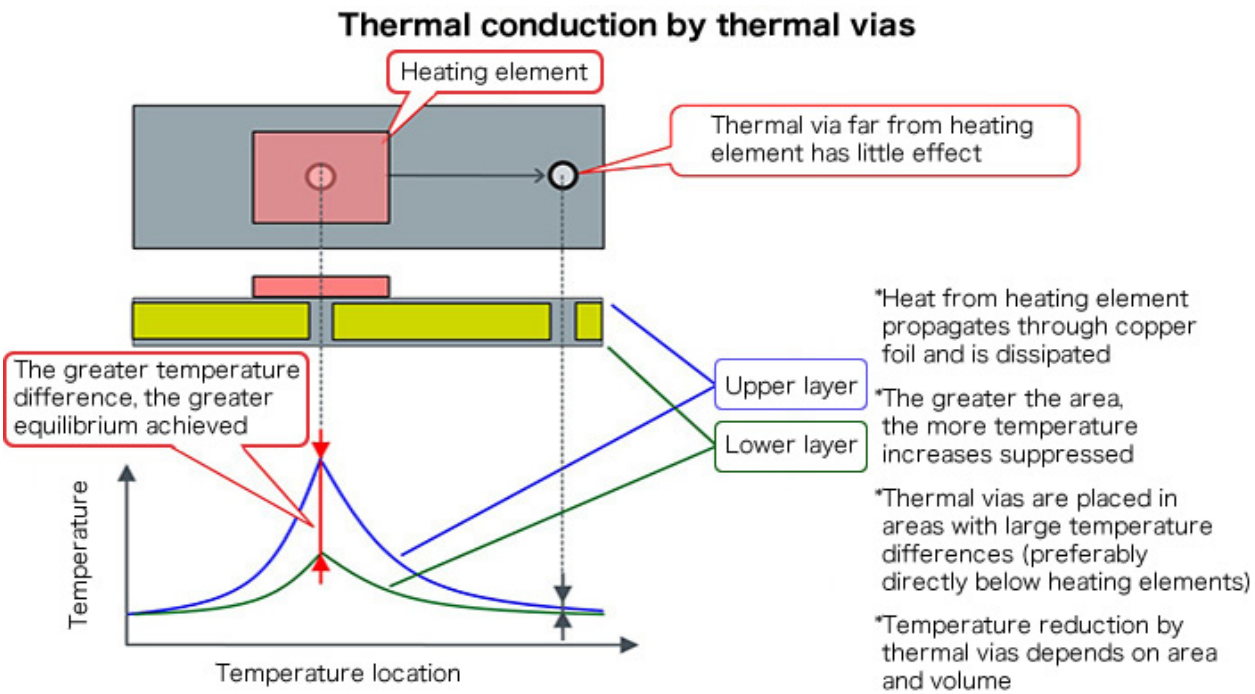
First, the via is filled with non-conductive epoxy depending on the designer's requirement. Later, this via is capped and plated to regain the land area. This technique shrinks the signal path lengths and as a result eliminates the parasitic inductance and capacitance effect.

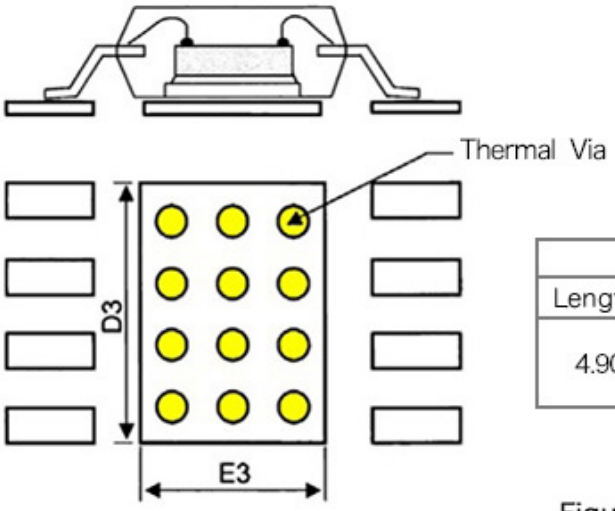
The via-in-pad accommodates smaller component pitch sizes and shrinks the PCB's overall size. This technology is ideal for BGA footprint components.

To make things better, back-drilling process is implemented along with the via-in-pad. The back drilling is performed to eliminate the signal reflections within the unused portion of the via. The unwanted via stub is drilled to remove any kind of signal reflection. This ensures signal integrity.

Placement of Thermal Vias



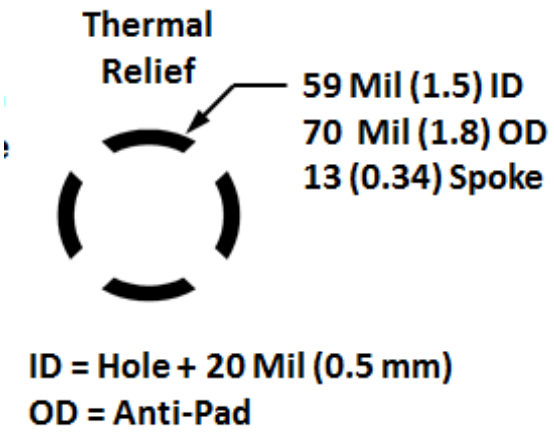




Central land		Thermal via	
Length D3	Width E3	Pitch	Diameter
4.90mm	3.20mm	1.20mm	ϕ0.30

Figure 4.
Dimensional diagram of thermal vias for a package with back-surface heat dissipation

Your ground plane needs to be complete. By this we mean not splitting your ground plane any routed signal.If you create a split in this plane ,signals will have to go around the void ,which can lead to some nasty EMI and signal timing issues If you do need to split a ground plane, then be sure to add a 0 Ohm resistor alongside the signal trace so that your return signal has a bridge to make its return path easier



ANTIPAD:

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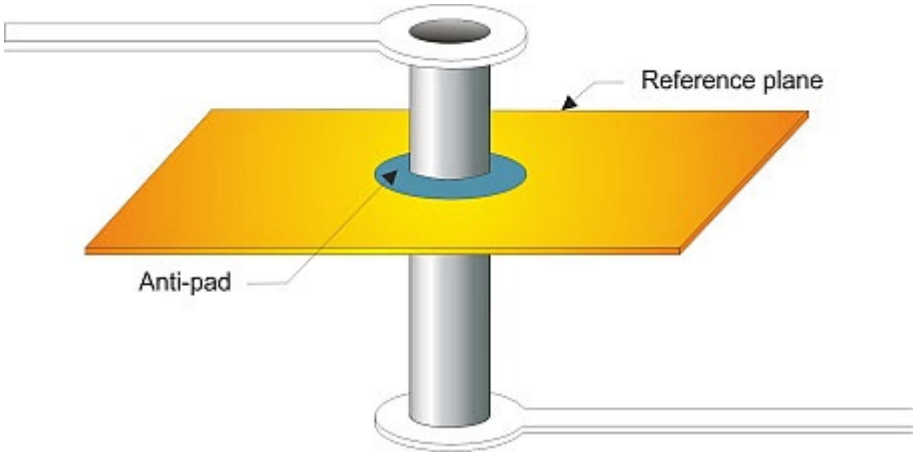
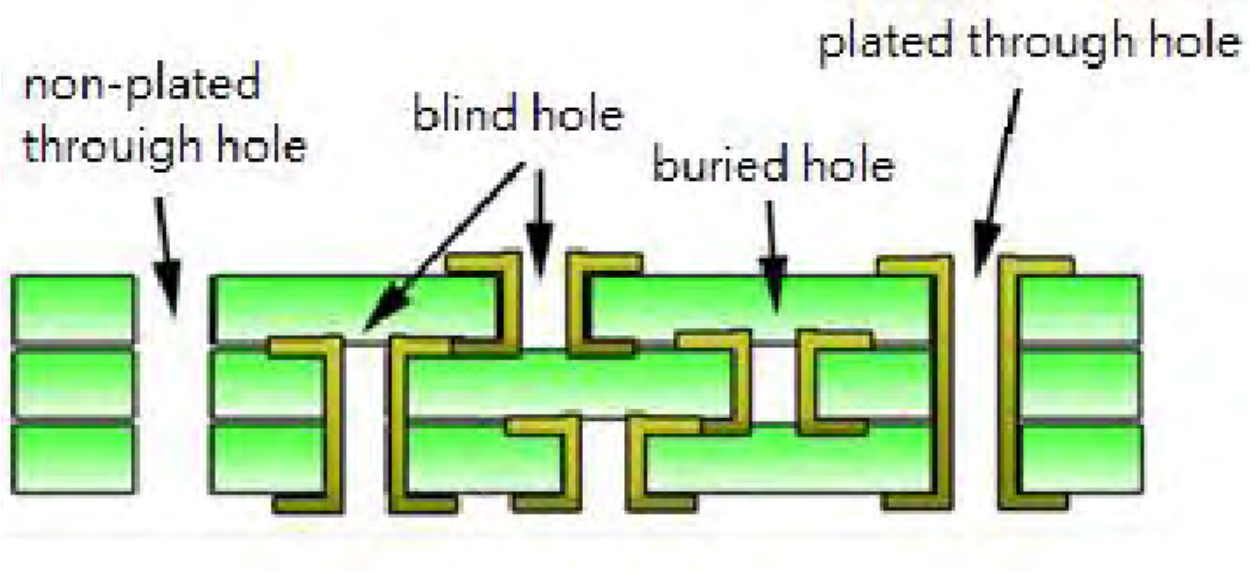
The antipad is the space around the via on the plane layers that the via is not meant to connect to in order to prevent short-circuit.



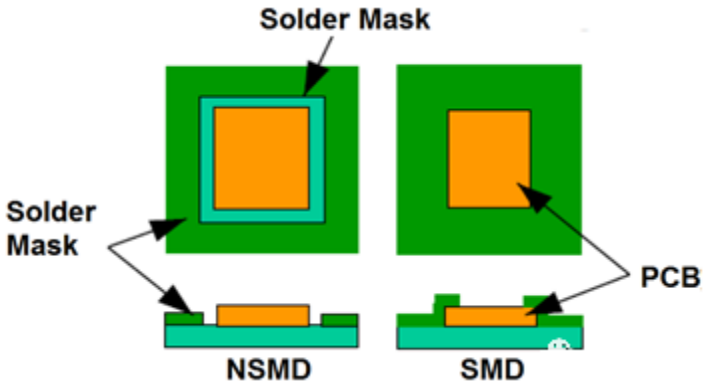


2- PADS:

A pad is a small surface of copper in a printed circuit board that allows soldering the component to the board. You can think of a pad as a piece of copper where the pins of the component are mechanically supported and soldered. There are 2 types of pads; thru-hole and smd (surface mount).

- SMD (Surface Mount Device) PAD:

TYPES:



- SMD(Solder Masked Defined) PAD:

SMD PAD is smaller than the solder mask area as shown above

Pros: reduces the likelihood of PAD detachment during soldering or disordering

Cons: this reduces the copper area for solder joint and reduces space between adjacent pads this limit thickness of trace between pads and may affect the use of vias

- NSMD(NON Solder Masked Defined) PAD:

NSMD refers to the padding process in which the solder mask opening is larger than the pad.

Pros:

This process provides a larger surface area for solder joint connections.

It provides more enormous gaps between pads (compared to SMD), allowing for broader trace widths and more through-hole flexibility.

Cons:

during the soldering and disordering process, the NSMD is more likely to fall off. Even so, NSMD still has better soldering performance and is suitable for solder joint package pads.

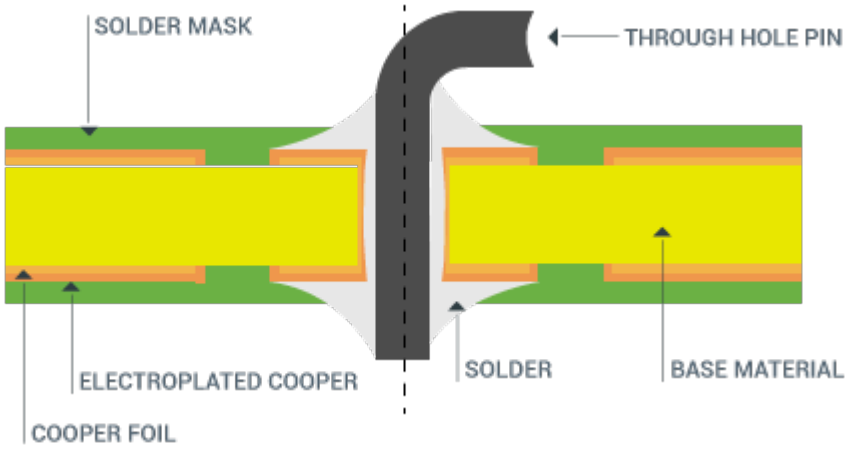
- THROUGH HOLE:

- PTH (Plated Through Hole) PAD: (copper pad >> drilled hole)

The main characteristic of this type of holes is that, during the manufacturing process, after drilling the boards a thin copper layer is plated onto the walls of the holes, providing them with electrical conductivity. This way, after the PCB Assembly is finished, the link between the component's leads and the copper tracks has a lower resistance and better mechanical stability.

Today most PCBs are double sided, or multi-layered, and most of the Through Holes are plated, this way the components can connect to the required layers in the board. The mounting scheme of a PTH can be seen in Figure.

FIGURE 2



- NPTH (Non-Plated Through Hole) PAD (Copper pad << drilled hole):

As its name says, in this type of Through Holes there is no copper plated onto the walls of the holes, so the barrel of the hole has not electrical properties. They were very popular when Printed Circuits only had copper tracks printed on one side, but their use decreased as the number of layers in PCBs increased.

The main advantages of NPTH are that the manufacturing process for these is simpler, and obviously quicker. Nowadays, they are frequently, but not exclusively, used as Tooling/Mounting holes: used to fix the PCB to its operational location. However, they can also be used for components mounting as shown in Figures below.

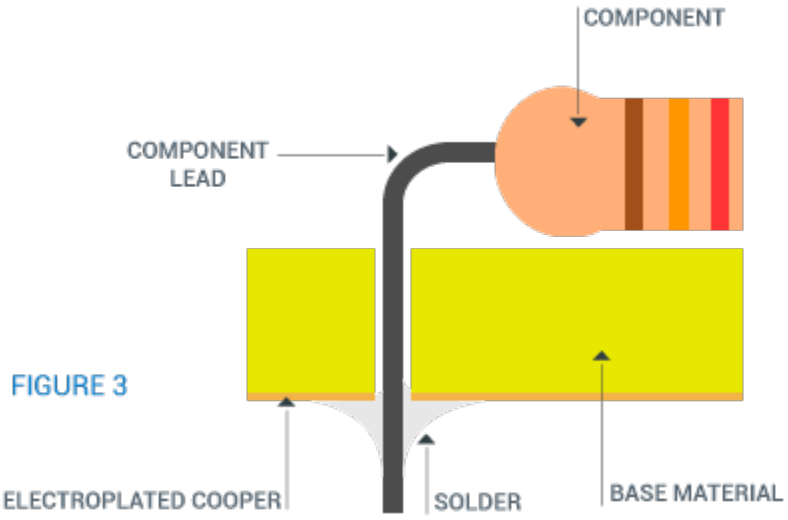
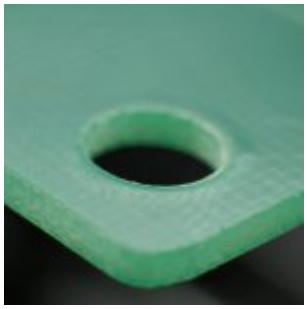
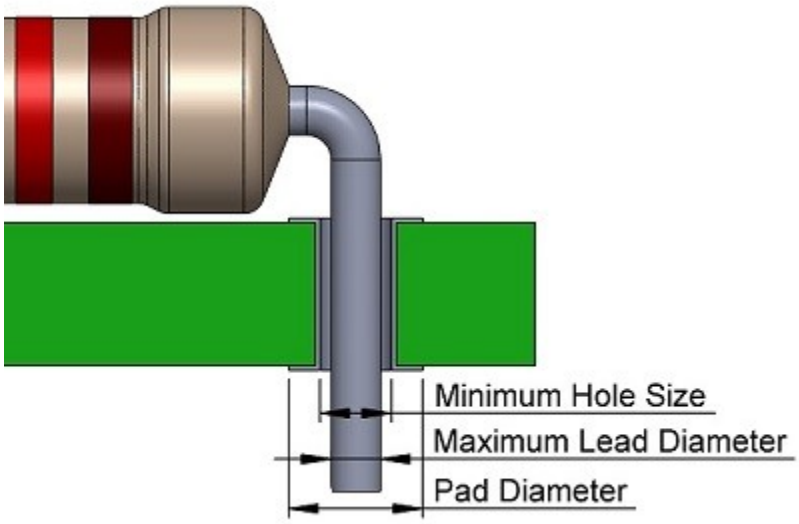


FIGURE 3

So, we have NPTH and PTH: the only difference is Non-plated through holes are simple features that are either drilled or milled through your circuit board, which expressly do not receive a plating of conductive copper. Typical uses of NPTH features are mounting holes to allow screws or other fasteners to pass through your board.



- VIA AND PAD DIMENSIONS:



1. Calculate the Minimum Hole Size:

Minimum Finished hole size the size of hole in which leads of the components can be easily inserted and Solder can easily flow through the lead.

Minimum Hole Size =Maximum Lead dia+Hole Diameter Factor

Minimum Hole Size = Maximum Lead Diameter + 0.25mm (for Density Level A)

Minimum Hole Size = Maximum Lead Diameter + 0.20mm (for Density Level B)

Minimum Hole Size = Maximum Lead Diameter + 0.15mm (for Density Level C)

* Density Levels A, B and C describe the measure of the relative ease of manufacturing.

Density Level A is used for General Design Producibility. It is a Preferred Level. Level A is used for the Low component density. In this case, footprint geometry is ‘Maximum’. This method is applied to the most robust producibility.

Density Level B is used for Moderate Design Producibility. It is a Standard Level. Level B conditions are suitable for reflow, wave, drag or dip soldering.

Density Level C is used for High Design Producibility. It is a Reduced Level. Level C is used for the High component density. In this case footprint geometry is 'Minimum'. This method is applied to a hand-held and portable appliances.

3. Calculate the Pad Diameter

After you calculate the Minimum Hole Size, you should know that the Minimum Annular Ring is0.05mm (50um). According to IPC-2221 the Minimum Fabrication Allowance is 0.6mm for Level A, 0.5mm for Level B and 0.4mm for Level C.

Minimum Annular Ring = (*Min Ring Border*) * 2 + (*Hole Size*) + (*Tolerance*)

Minimum Annular Ring on the Inner Layer	0.1mm
Minimum Annular Ring on the Outer Layer	0.05mm

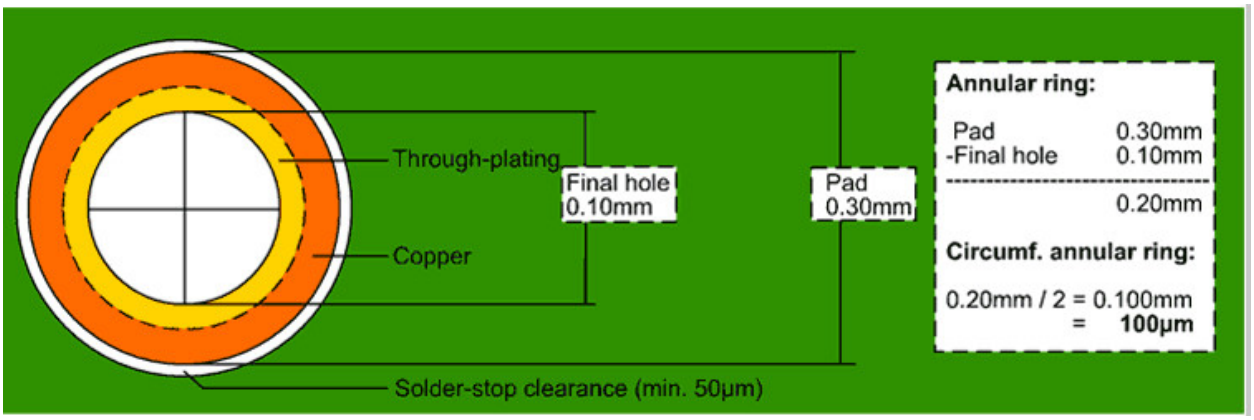
Pad Diameter = Minimum Hole Size[Finished] + Minimum Annular Ring X 2 + Minimum Fabrication Allowance

Pad Diameter = Minimum Hole Size + 0.1mm + 0.40mm (for Level A of IPC-2221)

Pad Diameter = Minimum Hole Size + 0.1mm + 0.25mm (for Level B of IPC-2221)

Pad Diameter = Minimum Hole Size + 0.1mm + 0.20mm (for Level C of IPC-2221)

Annular Ring: An annular ring is the area of copper pad around a drilled and finished hole. The finished hole we are talking about here is nothing but a copper-plated via. All around this via there should be enough copper to form a solid connection between the copper traces and the via in a multi-layer PCB. Therefore, the main purpose of an annular ring is to establish a good connection between a via and the copper trace. Generally, we keep 10mils annular ring.



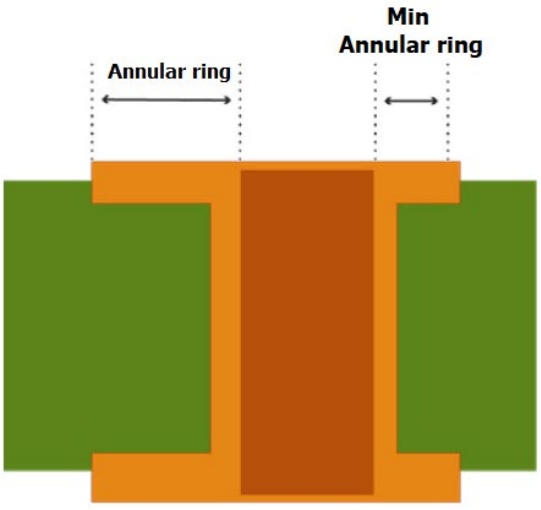
Ideally, designers want their annular rings with holes located dead-center in order to get the best connection possible between the vias and the layers.

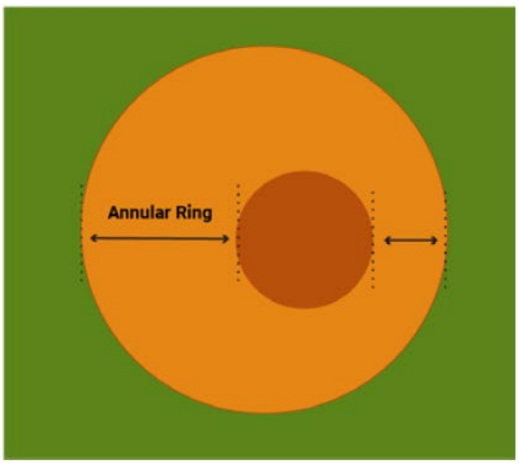
The perfect annular ring width is the difference between the diameter of the copper pad and the diameter of the finished hole divided by two.

Annular ring width = (Diameter of the pad – Diameter of the finished hole) / 2

Why does the annular ring size matter?

The width of the ring should be sufficiently thick to allow reliable electrical connection with via. The minimum length of the annular ring should be greater than or equal to the specified width for the design.





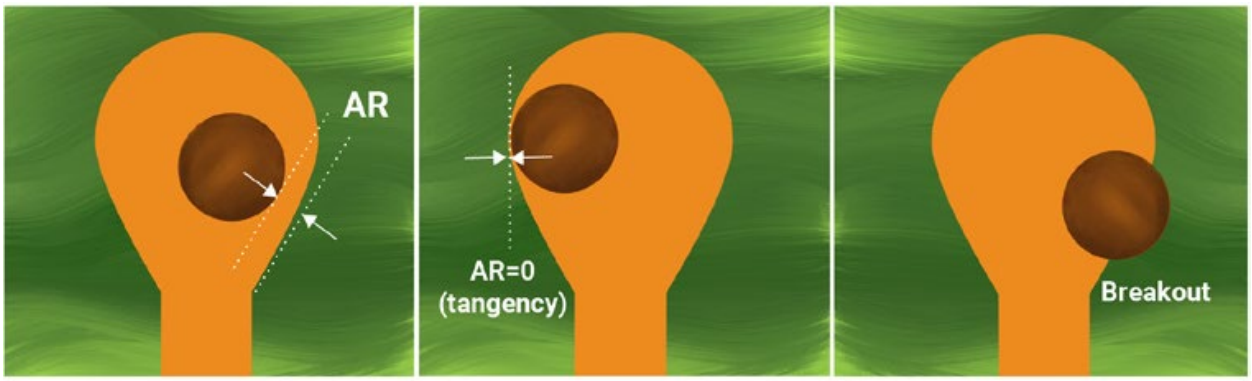
Common annular ring issues

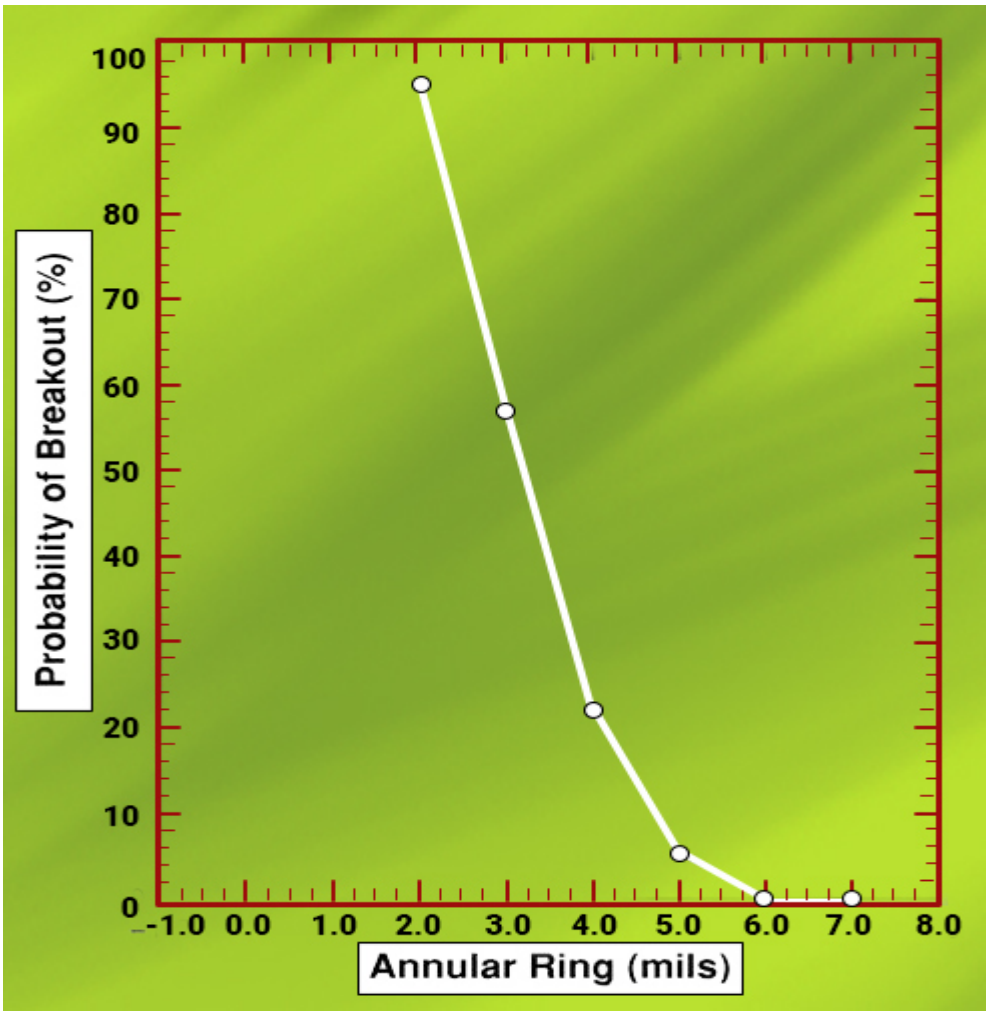
Undesired annular ring

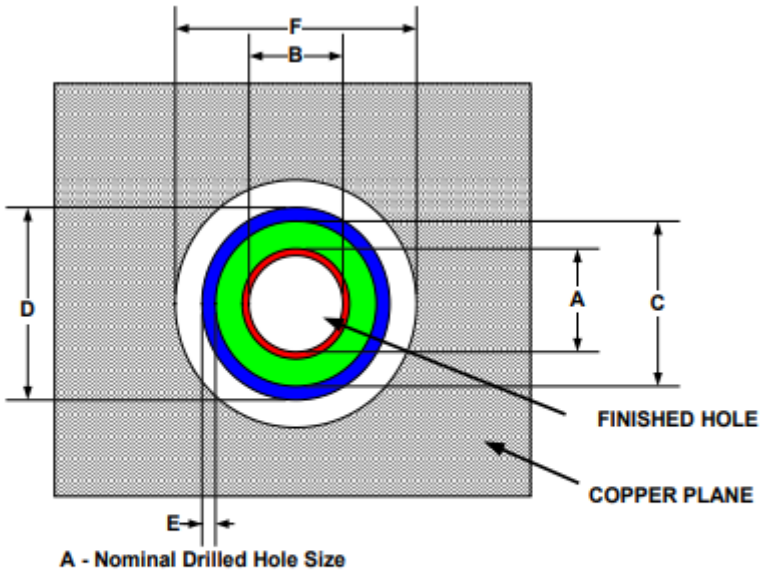
Tangency

Breakout

All the above may arise due to insufficient annular ring width in the design.







A - Nominal Drilled Hole Size
B - Plated Hole Size (Finished Hole Diameter)
C - Maximum Wander of Drilled Hole
D - Capture Pad Size
E - Minimum Annular Ring
F - Clearance to Nearest Copper (all layers)
This is the diameter of the cylinder piercing all layers.

is the top-down view of the plated through-hole or via. It shows the clearance hole or pad in a power plane of the F diameter. This is the minimum opening in the power planes needed to guarantee that there is enough room for the drilled hole, the drill wander, and the minimum insulation to nearest copper in any layer, be it signal or power.