

# Reference Design for Line AC Voltage Generation From Low-Voltage DC Source for Sensor Excitation



## Description

This reference design demonstrates a method for designers to achieve high-voltage signals that can be used for flame detection using discrete components. The reference design is built with a low BOM cost and small solution size in mind. By using push-pull converter topology, it is possible to achieve a wide input range and low start-up time.

## Resources

<a href="#">TIDA-01426</a>	Design Folder
<a href="#">TL494</a>	Product Folder
<a href="#">TL431</a>	Product Folder
<a href="#">CSD19538Q3A</a>	Product Folder
<a href="#">TLV171</a>	Product Folder

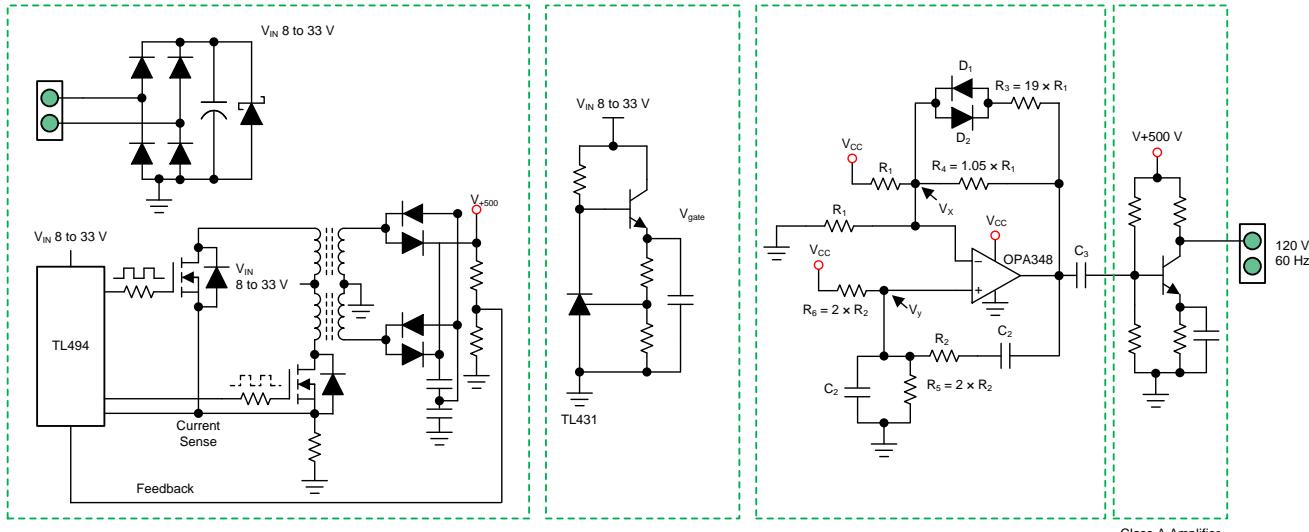

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## Features

- Universal Input Range of 10 to 36 V
- 120-V, 60-Hz Output up to 4% THD
- 56-ms Startup Time at 10 V
- 5% Output Accuracy
- Output Power up to 1 W
- Low Footprint and BOM Cost

## Applications

- HVAC Valve And Actuator Control
- HVAC Sensor Transmitter
- HVAC System Controller



Low-Cost, High-Efficiency Push-Pull Boost Converter

Low-Cost Regulated LDO

Low THD, Sine Wave Oscillator  
\*Can be generated using MCU based SPWM

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## 1 System Description

A burner system is an integral part of a heating, ventilation, and air conditioning (HVAC) system. A burner system helps generate hot water or steam for heating purposes. The hot water is circulated either for utility purposes or for temperature control. The burner system has control electronics as shown in [Figure 1](#) to operate in optimum conditions and prevent any failure with a predictive diagnosis alarm. The electronics unit has actuator control and field sensing cards for the motor drive, damper control, flow control, temperature and pressure sensing, and so on. The unit also ignites and senses flame inside the burner as shown by ECU4 (see [Figure 1](#)). This reference design focuses on the excitation power supply for the flame rod.

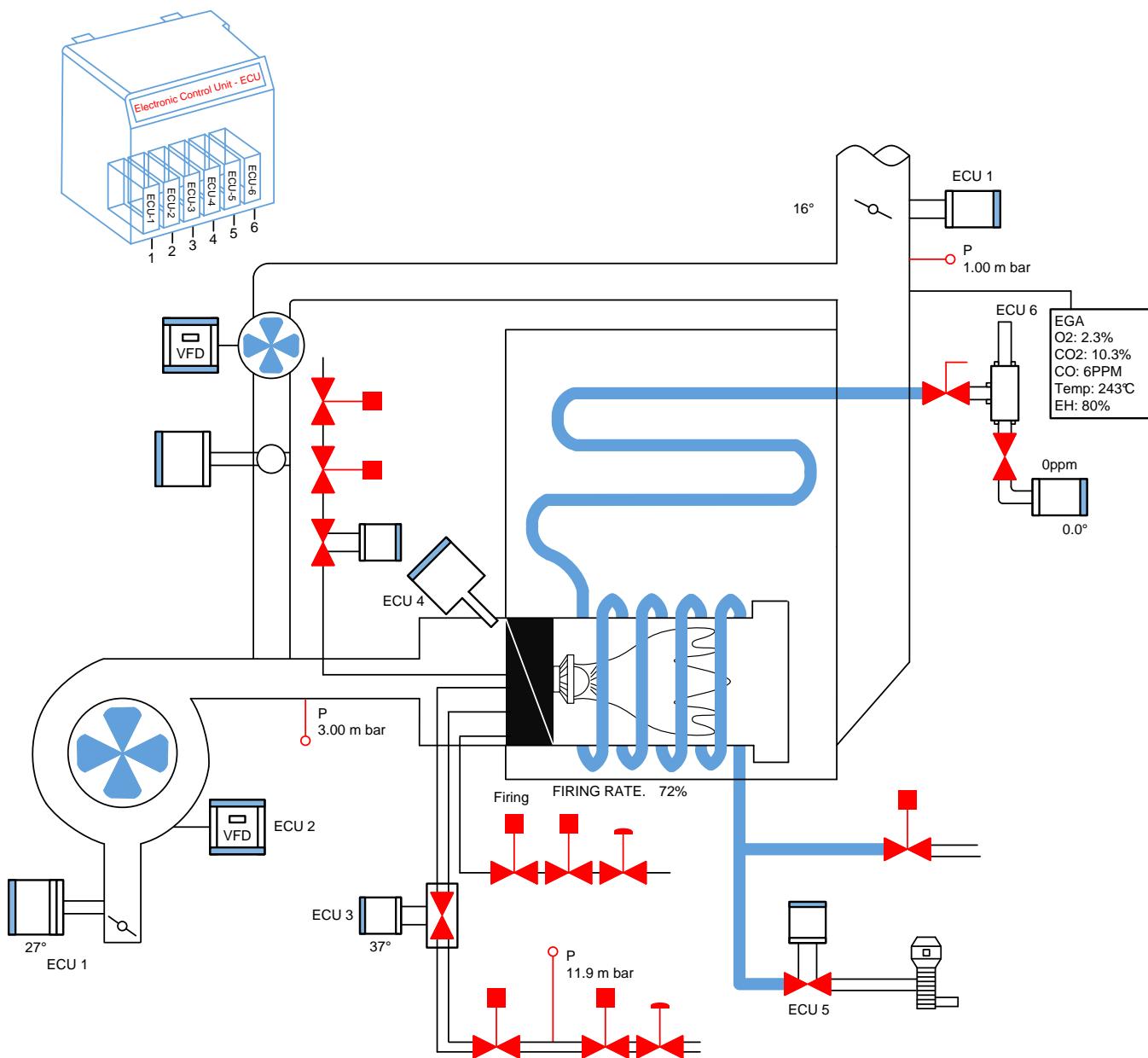
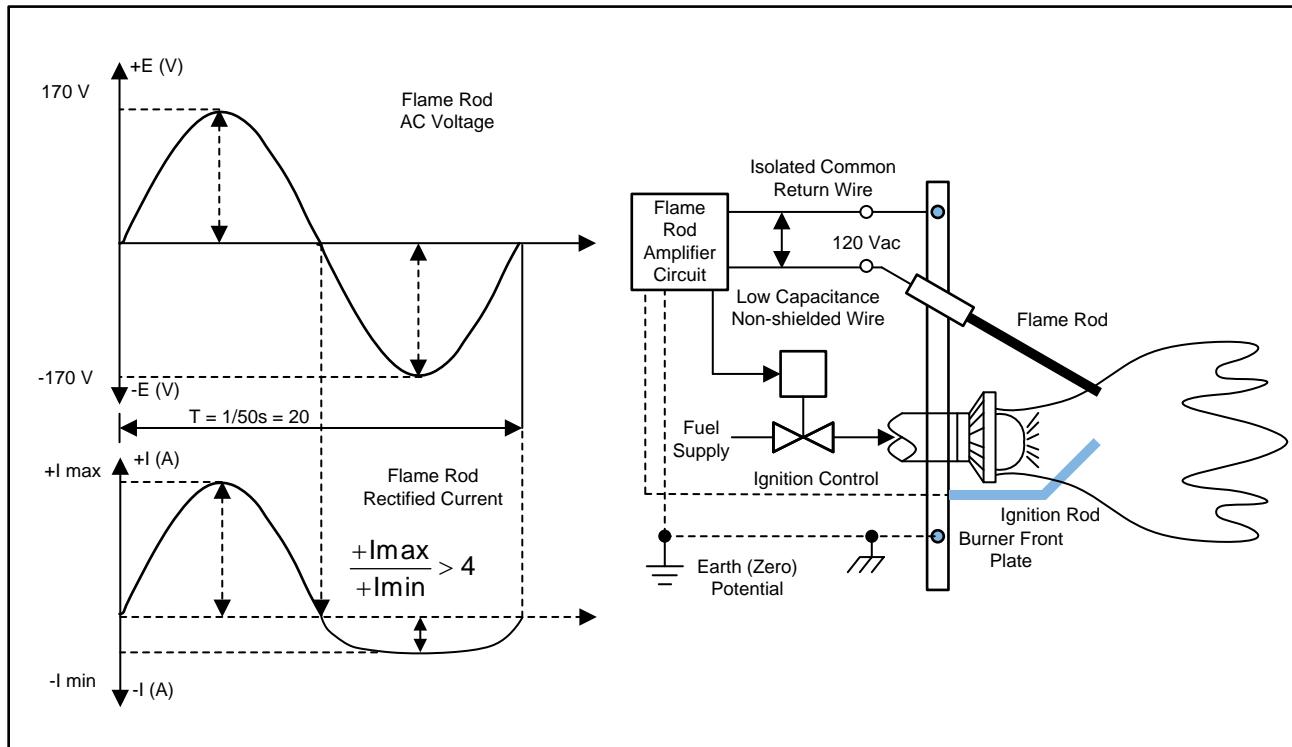


Figure 1. Burner Control

The flame rod sensor is a high impedance sensor. Under the presence of flame, an ionization effect takes place due to which current flows from the flame rod to earth. This current is proportional to flame intensity. As shown in [Figure 2](#), a high-voltage excitation is required for ionization effect. To prevent carbonization effect, AC excitation is applied. This excitation is usually a line supply 50- or 60-Hz signal. A low-frequency AC signal is used to prevent losses due to cable capacitance and skin effect. The geometric ratio of flame rod and earth plate decides the conduction in positive and negative polarity. Usually the ratio is lower to make the flame rod conduct more in positive half cycles and negligible in negative half cycles. This ratio results in output similar to a half wave rectifier. Thus, the flame rod is equivalent to a forward bias diode with a high series impedance, which is the function of flame intensity as shown in [Figure 2](#). A signal chain amplifies the lower AC current and controls the fuel supply for the burner firing rate.



**Figure 2. Flame Sensing Using Flame Rod**

### 1.1 Key System Specifications

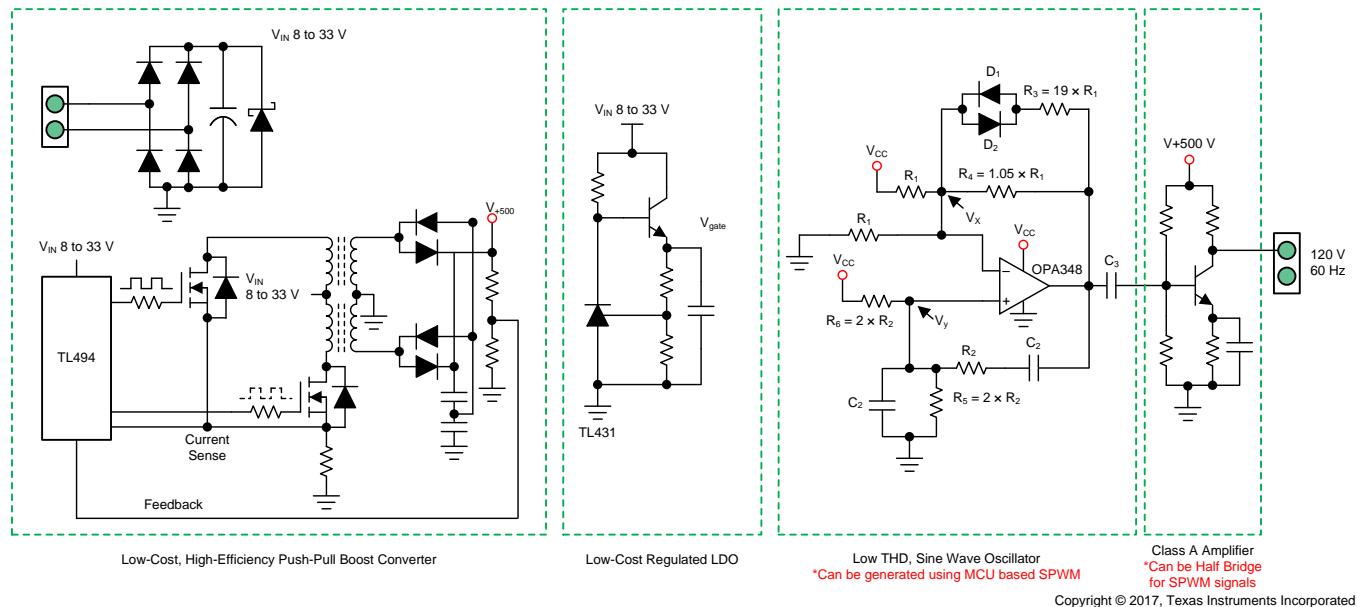
**Table 1. Key System Specifications**

PARAMETER	SPECIFICATIONS			
	MIN	TYP	MAX	UNIT
Input supply voltage ( $V_{IN}$ )	DC	10	24	33
	AC at 50 or 60	18	24	33
Quiescent current ( $I_Q$ )	—	—	0.3	A
Output voltage ( $V_O$ )	105	120	140	V
Output current ( $I_O$ )	—	—	0.0015	A
Output load ( $R_L$ ) Max cable capacitance 720 pF, assuming 22 AWG, 60 feet, 1 pair twisted cable 12 pF/ft	1	40	100	MΩ
Performance	Initial accuracy	—	5	%
	THD	—	4	%
	Startup time at 10 V	—	100	ms

## 2 System Overview

### 2.1 Block Diagram

The power block can be divided into four sections (as shown in [Figure 3](#)) for understanding system design calculations.

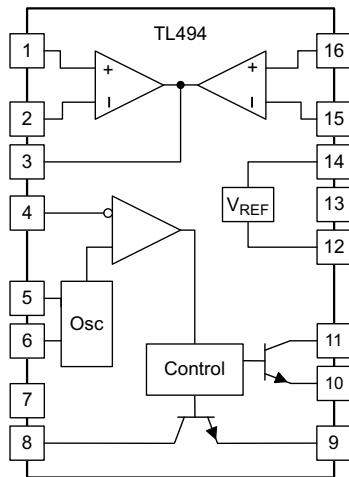


**Figure 3. System Block Diagram**

### 2.2 Highlighted Products

#### 2.2.1 TL494

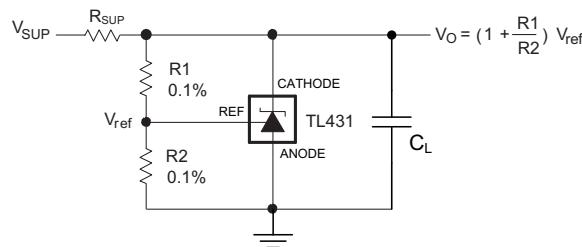
The TL494 device incorporates all the functions required in the construction of a control circuit for pulse width modulation (PWM) on a single chip. The TL494 device contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output control circuits. The error amplifiers exhibit a common-mode voltage ranging from  $-0.3$  V to  $V_{CC} - 2$  V. The DTC comparator has a fixed offset that provides approximately 5% dead time. The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 device provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation. The TL494C device is characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . The TL494I device is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



**Figure 4. TL494 Block Diagram**

### 2.2.2 TL431

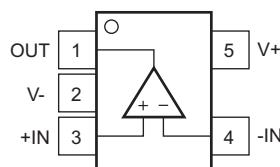
The TL431 device is a three-terminal adjustable shunt regulator. The output voltage can be set to any value between  $V_{REF}$  (approximately 2.5 V) and 36 V with two external resistors. These devices have a typical output impedance of  $0.2 \Omega$ . Active output circuitry provides a very sharp turnon characteristic, making these devices excellent replacements for Zener diodes in onboard regulation, adjustable power supplies, and switching power supplies.



**Figure 5. TL431 Shunt Regulator**

### 2.2.3 TLV171

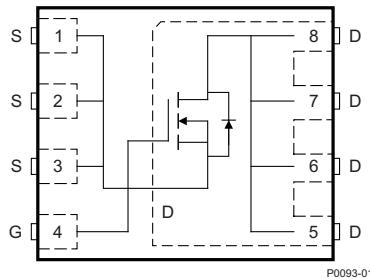
The 36-V TLV171 device provides a low-power option for cost-conscious industrial systems requiring an electromagnetic interference (EMI)-hardened, low-noise, single-supply operational amplifier (op amp) that operates on supplies ranging from 2.7 V ( $\pm 1.35$  V) to 36 V ( $\pm 18$  V). The TLV171 provides low offset, drift, and quiescent current balanced with high bandwidth for the power. Input signals beyond the supply rails do not cause phase reversal. The TLV171 is stable with capacitive loads up to 200 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation.



**Figure 6. TLV171 Block Diagram**

## 2.2.4 CSD19538Q3A

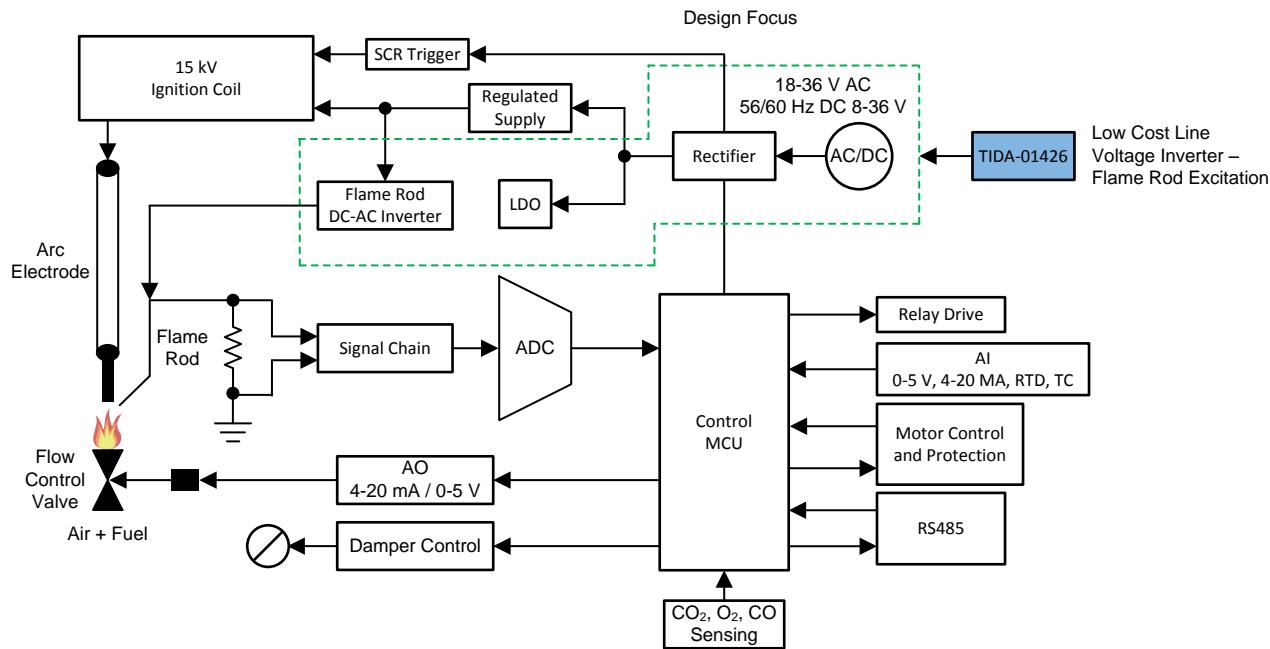
The CSD19538Q3A is NexFET™ power MOSFET with a drain-to-source voltage of 100 V, a low  $R_{DS(on)}$  of 49 mΩ, and small footprint SON of 3.3 mm × 3.3 mm to achieve very low conduction losses and reduce board space.



**Figure 7. MOSFET CSD19538Q3A**

## 2.3 System Design Theory

The TIDA-01426 design focuses on the design of a power supply targeted for flame rod excitation in burner control, as shown in [Figure 8](#). The supply needs to generate a low-voltage regulated supply for low-power peripherals and line supply voltage for flame rod excitation. Using the TL494 and TL431 devices generates the required low- and high-voltage supplies.



**Figure 8. Typical Electronics Control Board**

### 2.3.1 Designing Push-Pull Converter

#### 2.3.1.1 TL494 Calculations

To generate high DC bus voltage, push-pull topology is implemented in this reference design. Using flux swing in both polarities and high switching frequency makes it easy to design the small size magnetic transformer. TL494 integrated peripherals like an oscillator, dead-time controller, error amplifier, and PWM generator make it possible to design a low-cost, regulated output, push-pull converter.

### 2.3.1.1.1 Oscillator Calculations

The oscillator of the TL494 is set by  $R_t$  and  $C_t$ . To design a smaller magnetic transformer, a 100-kHz oscillating frequency is selected. For push-pull configuration with a  $C_t$  of 1 nF, the computed  $R_t$  value is 5k as shown in [Equation 1](#). The closest standard value is 4.99k. In the schematic,  $R_6$  and  $C_6$  denotes  $R_t$  and  $C_t$ . For stable oscillations, a low-ppm resistor and C0G capacitor are recommended.

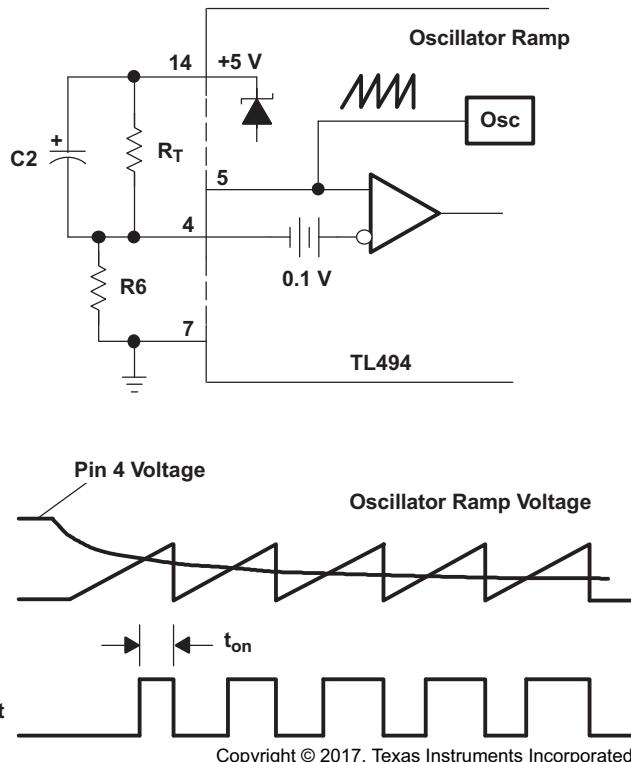
$$R_T = \frac{1}{2 \times f_{OSC} \times C_T} = \frac{10^9}{2 \times 100000 \times 1} = 5 \text{ k} \quad (1)$$

### 2.3.1.1.2 Soft-Start and Dead-Time Calculations

The TL494 can be tailored for custom soft-start and dead time to prevent high in-rush current and cross conduction. As shown in [Figure 9](#), capacitor  $C_2$  with  $R_6$  applies a negative slop waveform, allowing the pulse width to increase slowly. Initially capacitor  $C_2$  forces the DTC to follow an input of 5 V, which results in 100% dead time. Soft-start can be configured in multi of clock cycle as shown in [Equation 2](#).

$$C_2 = \frac{100 \times \frac{1}{f_{SW}}}{R_6} = \frac{100 \times \frac{1}{100000}}{1000} = 1 \mu\text{F} \quad (2)$$

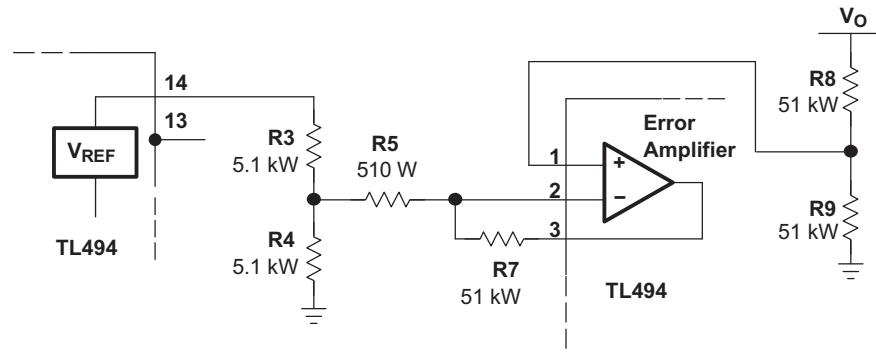
As the soft-start slope slowly decays, the potential due resistor divider  $R_6$  and  $R_7$  with an internal 0.1-V offset result into a tailored dead time. After soft-start, the voltage at the pin is a ratio of  $R_6:R_7$  multiplied by  $V_{REF}$ . The value for dead time is computed based on the turnon and turnoff time of the MOSFET so that enough blanking is provided to prevent cross conduction. For this reference design, a blanking time of 500 ns is provided with resistor  $R_7$  of 5k.



**Figure 9. Soft-Start Circuit**

### 2.3.1.1.3 Voltage Error Amplifier

A simple non-inverting error amplifier is implemented with one of the TL494 internal op amps. An internal reference of 5 V is divided to 2.5 using resistors  $R_{11}$  and  $R_{14}$  in board. Figure 10 is shown with resistors  $R_3$  and  $R_4$ . The desired output is scaled to 2.5 V using resistors  $R_{10}$  and  $R_7$ . The closed loop gain of the op amp (= 101) helps to maintain stable output. Resistors  $R_9$  and  $R_4$  are feedback resistors on board to get the desired closed loop gain.

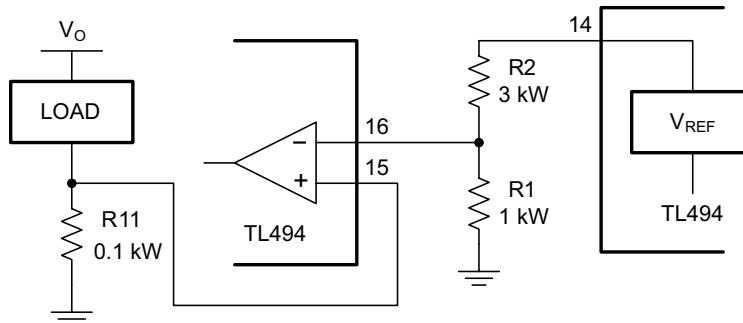


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**Figure 10. Feedback Error Amplifier**

### 2.3.1.1.4 Overcurrent Protection

Overcurrent protection is implemented using one of the internal op amps of the TL494. A stable 1 V is applied to the negative terminal of the op amp using resistors  $R_{13}$  and  $R_{15}$  in the actual circuit. A current sense resistor  $R_{12}$  of 1 Ω is connected to the source pin of the MOSFET Q<sub>1</sub> and Q<sub>2</sub>. The circuit is limited to a peak current of 1 A once the voltage across sense resistor  $R_{12}$  increases to a 1-V reference.



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**Figure 11. Current-Limiting Circuit**

### 2.3.1.2 Magnetic Design

The objective for this application is to have a smaller footprint transformer. To achieve the same, this reference design has a 100-kHz switching frequency and a max duty cycle of 40%. In this application, Wurth E13 core transformer is used. For a custom transformer design, the proper core material needs to be selected. N87, N88, N95, N96, and N97 are some standard core materials available from TDK Epcos for a switching frequency up to 500 kHz. N87 core can be selected which has saturation flux of 0.39 T at 100°C with core loss of 3.75 mW / mm<sup>3</sup> at 100 kHz switching. This application uses a custom Wurth Transformer. The design equations shown in Table 3 can be used for a custom transformer design. For a cost-sensitive application, a Toroid core can also be used. For ease of design, the maximum flux swing ( $B_m$ ) can be limited to 0.2 T with current density ( $J$ ) of 3 A/mm<sup>2</sup>. The E13 core is selected to show design calculations.

**Table 2. E13 Core Calculations**

SR NO	PARAMETER	VALUE	UNIT
1	Cross sectional area ( $A_c$ )	12.4	mm <sup>2</sup>
2	Window area ( $A_w$ )	$\left(\frac{(8.9 - 3.7)}{2} - 0.3\right) \times (4.5 - 0.3) = 9.66$ where 0.3 is for bobbin clearance	mm <sup>2</sup>
3	Area product ( $A_p$ )	$A_c \times A_w = 82.58$	mm <sup>4</sup>
4	Nominal inductance ( $A_i$ )	850	nH

**E 13/7/4 (EF 12.6)****Core****B66305**

- To IEC 61246
- For miniature transformers
- Available with SMD coil former
- E cores with high permeability for common-mode chokes and broadband applications
- Delivery mode: single units

**Magnetic characteristics (per set)**

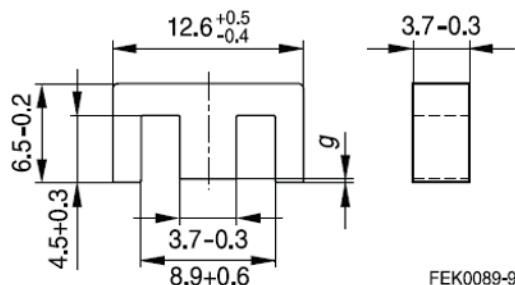
$$\Sigma l/A = 2.39 \text{ mm}^{-1}$$

$$l_e = 29.6 \text{ mm}$$

$$A_e = 12.4 \text{ mm}^2$$

$$A_{\min} = 12.2 \text{ mm}^2$$

$$V_e = 367 \text{ mm}^3$$

**Approx. weight** 2 g/set

FEK0089-9

**Ungapped**

Material	$A_L$ value nH	$\mu_e$	$P_V$ W/set	Ordering code
N30	1000 +30/-20%	1900		B66305G0000X130
T46	$3600 \pm 30\%$	6839		B66305F0000X146
N27	800 +30/-20%	1510	< 0.40 (200 mT, 100 kHz, 100 °C)	B66305G0000X127
N87	850 +30/-20%	1620	< 0.20 (200 mT, 100 kHz, 100 °C)	B66305G0000X187

**Figure 12. E13 Core Specification**

**Table 3. Transformer Calculations**

SR NO	PARAMETER	EQUATION	COMPUTED VALUE	SELECTED VALUE
1	Required area product	$A_p = \frac{(\sqrt{2} \times V_{DC} \times I_{DC}) \times \left(1 + \frac{1}{\eta}\right)}{4 \times k_w \times B_m \times f_s \times J}$ where $k_w = 0.4$ , $\eta = 0.8$ , $V_{DC} = 500$ V, and $I_{DC} = 2$ mA	33.14 mm <sup>4</sup>	Area product computed as shown in <a href="#">Table 2</a> is greater
2	Primary turns	$N_1 = \frac{V_{MIN}}{4 \times B_m \times f_s \times A_c}$ where $A_c$ is the cross section of the core	10	10
3	Turns ratio	$n = \frac{V_{DC}}{2 \times D_{MAX} \times V_{MIN}}$ where $D_{MAX} = 0.4$	62.5	63
4	Secondary turns	$N_2 = n \times N_1$	630	630
5	Secondary RMS current	$I_2 = \sqrt{D_{MAX} \times I_{DC}}$	1.43 mA	—
6	Primary RMS current	$I_1 = n \times I_2$	90.5 mA	—
7	Cross section area of primary wire	$a_1 = \frac{I_1}{J}$	0.026 mm <sub>2</sub>	36 SWG 0.02927 mm <sub>2</sub>
8	Cross sectional area of secondary wire	$a_2 = \frac{I_2}{J}$	0.0004 mm <sub>2</sub>	45 SWG 0.003973 mm <sub>2</sub>
9	Total winding area	$\sum_{i=1}^2 a_i N_i = (2 \times N_1 \times a_1) + (N_2 \times a_2)$	3.08 mm <sub>2</sub>	—
10	Utilization factor	$\left( \frac{\text{Total Winding Area}}{\text{Window Area } A_w} \right) \times 100$	31.88 %	Value < 40 %

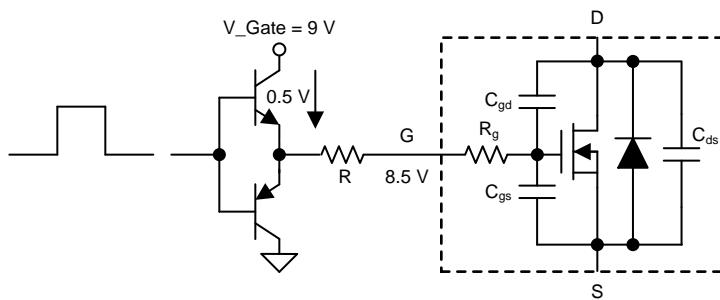
Inductors can be added in series with output diodes and capacitors to limit ripple current.

### 2.3.1.3 MOSFET Drive and Losses

The fast switching speed, low drop voltage, and high input impedance of MOSFETs make them suitable for push-pull switching. The TI NexFET CSD19538Q3A with low drain-to-source channel resistance is selected for push-pull drive. The MOSFET is driven using an external totem pole transistor for a better drive capability.

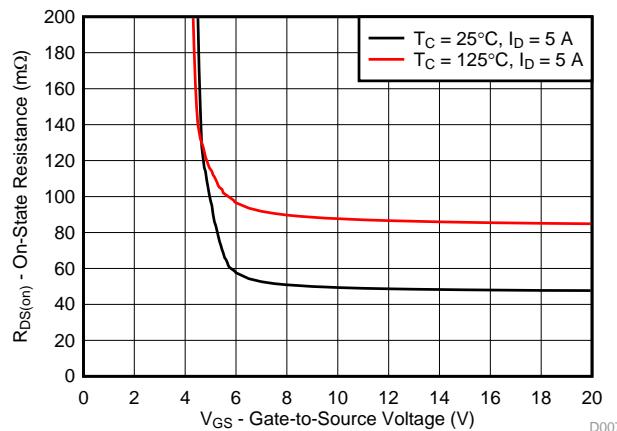
#### 2.3.1.3.1 Conduction Losses

The MOSFET gate drive is driven through the totem pole circuit as shown in Figure 13.



**Figure 13. MOSFET Totem Pole Drive**

During high pulse, the NPN transistor conducts resulting in a gate drive voltage of 8.5 V due to a 0.5-V drop across the collector-emitter. From the MOSFET datasheet, the typical  $R_{DS(on)}$  for a 8-V gate-to-source voltage is 50 m $\Omega$ .



**Figure 14. MOSFET On-State Resistance**

Power loss during conduction phase is computed as shown in Equation 3.

$$P_{\text{cond}} = \frac{1}{T} \int_0^{\text{ton}} (n \times I_0)^2 \times R_{\text{DSon}} dt = \frac{1}{T} (n \times I_0)^2 \times R_{\text{DSon}} \times \text{ton} = (n \times I_0)^2 \times R_{\text{DSon}} dt \times D = 317 \mu W \quad (3)$$

### 2.3.1.3.2 Gate Drive Power Loss

During turnon, the gate-to-source capacitance ( $C_{GS}$ ) charges through resistor  $R + R_g$ . The current waveform is exponential decay. During this period there is power loss across the N-channel transistor.  $Q_{GS}$  is obtained from the MOSFET datasheet as shown in [Table 4](#).

**Table 4. Electrical Characteristics<sup>(1)</sup>**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>					
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100.0	—	—
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0 \text{ V}, V_{DS} = 80 \text{ V}$	—	—	1.0 $\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$	—	—	100.0 $\text{nA}$
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.8	3.2	3.8
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 6 \text{ V}, I_D = 5 \text{ A}$	—	58.0	72.0
		$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	—	49.0	59.0
$g_{fs}$	Transconductance	$V_{DS} = 10 \text{ V}, I_D = 5 \text{ A}$	—	6.1	—
<b>DYNAMIC CHARACTERISTICS</b>					
$C_{iss}$	Input capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}$	—	349.0	454.0 $\text{pF}$
$C_{oss}$	Output capacitance		—	69.0	90.0 $\text{pF}$
$C_{rss}$	Reverse transfer capacitance		—	12.6	16.4 $\text{pF}$
$R_G$	Series gate resistance	—	—	4.6	9.2 $\Omega$
$Q_g$	Gate charge total (10 V)	$V_{DS} = 50 \text{ V}, I_D = 5 \text{ A}$	—	4.3	— $\text{nC}$
$Q_{gd}$	Gate charge gate-to-drain		—	0.8	— $\text{nC}$
$Q_{gs}$	Gate charge gate-to-source		—	1.6	— $\text{nC}$
$Q_{g(th)}$	Gate charge at $V_{th}$		—	1.0	— $\text{nC}$
$Q_{oss}$	Output charge	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	—	12.3	— $\text{nC}$
$t_{d(on)}$	Turnon delay time	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}, R_G = 0 \Omega$	—	5.0	— $\text{ns}$
$t_r$	Rise time		—	3.0	— $\text{ns}$
$t_{d(off)}$	Turnoff delay time		—	7.0	— $\text{ns}$
$t_f$	Fall time		—	2.0	— $\text{ns}$
<b>DIODE CHARACTERISTICS</b>					
$V_{SD}$	Diode forward voltage	$I_{SD} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	—	0.85	1 $\text{V}$
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 50 \text{ V}, I_F = 5 \text{ A}, dI/dt = 300 \text{ A}/\mu\text{s}$	—	94.00	— $\text{nC}$
$t_{rr}$	Reverse recovery time		—	32.00	— $\text{ns}$

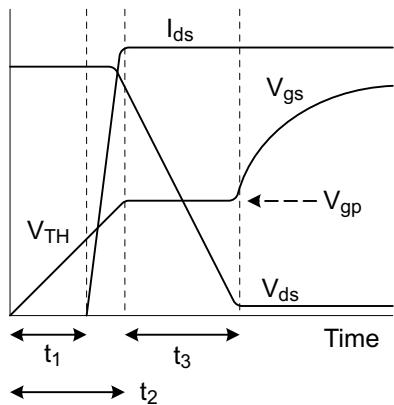
<sup>(1)</sup>  $T_A = 25^\circ\text{C}$

Power lost due to gate switching is computed as shown in [Equation 4](#).

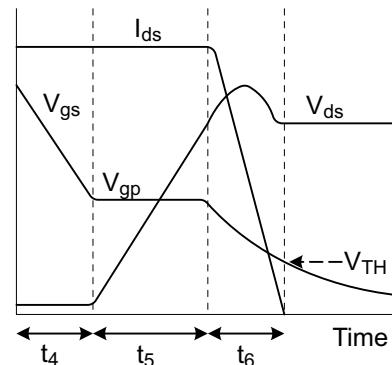
$$P_{GATE} = V_{GS} \times Q_{GS} \times f_{SW} = 8.5 \times 1.6 \times 10^{-9} \times 100000 = 1.36 \text{ mW} \quad (4)$$

### 2.3.1.3.3 MOSFET Switching Losses

During turnon and turnoff, the gate voltage rises slowly as the input capacitance charges, this results in switching loss across MOSFET. These losses can be computed independently for turn on and turn off by computing timing of each phase. As shown in [Figure 15](#) and [Figure 16](#), during turnon initially the input capacitance charges until the gate potential reaches the gate threshold voltage. After reaching the threshold, the drain current starts to increase until the gate voltage reaches Miller voltage. After reaching Miller voltage, the drain-to-source voltage falls as the gate-to-drain capacitance charges. Switching losses are in the region between the threshold voltage to Miller voltage and from the Miller voltage to the fall of the drain-to-source voltage.

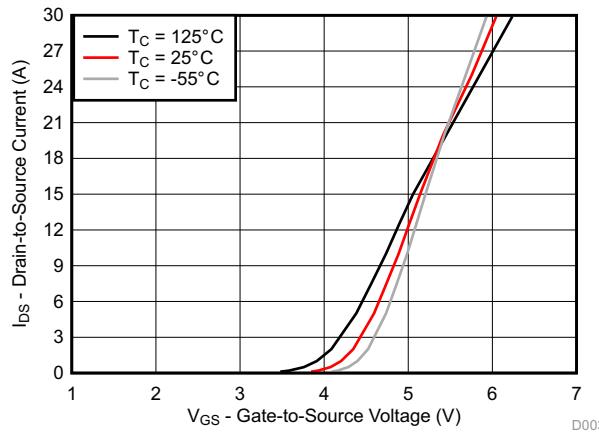


**Figure 15. MOSFET Turnon Characteristics**



**Figure 16. MOSFET Turnoff Characteristics**

To compute the timings, the gate threshold voltage and plateau voltage need to be computed. From the MOSFET datasheet, gate voltage is computed using a two-point equation (see [Figure 17](#) and [Equation 5](#)).



**Figure 17. MOSFET Transfer Characteristics**

$$V_{TH} = \frac{V_{GS1} \times \sqrt{I_{D2}} - V_{GS2} \times \sqrt{I_{D1}}}{\sqrt{I_{D2}} - \sqrt{I_{D1}}} = \frac{4.5 \times \sqrt{28} - 6 \times \sqrt{3}}{\sqrt{28} - \sqrt{3}} = 3.77 \text{ V} \quad (5)$$

The Miller voltage is computed as shown in [Equation 6](#).

$$V_P = V_{TH} + \sqrt{\frac{0.07968}{K}} = 3.77 + \sqrt{\frac{0.07968}{(V_{GS1} - V_{TH})^2}} = 3.77 + \sqrt{\frac{0.0905}{(8 - 3.77)^2}} = 4 \text{ V} \quad (6)$$

With the gate threshold and Miller voltage computed, turnon timings  $t_1$ ,  $t_2$ , and  $t_3$  are shown in [Equation 7](#), [Equation 8](#), and [Equation 9](#), respectively.

$$t_1 = (R_g + R_{ext}) \times C_{iss} \times \ln \left( \frac{1}{1 - \left( \frac{V_{TH}}{V_{GS}} \right)} \right) = (4.6 + 4.7) \times 349 \text{ pF} \times \ln \left( \frac{1}{1 - \left( \frac{1}{1 - \left( \frac{3.77}{8.5} \right)} \right)} \right) = 1.9 \text{ ns} \quad (7)$$

$$t_2 = (R_g + R_{ext}) \times C_{iss} \times \ln \left( \frac{1}{1 - \left( \frac{V_P}{V_{GS}} \right)} \right) = (4.6 + 4.7) \times 349 \text{ pF} \times \ln \left( \frac{1}{1 - \left( \frac{4}{8.5} \right)} \right) = 1.98 \text{ ns} \quad (8)$$

$$t_3 = (R_g + R_{ext}) \times C_{GD} \times \frac{V_{MIN}}{(V_{GS} - V_{GP})} = (4.6 + 4.7) \times 12.6 \text{ pF} \times \frac{12}{(8.5 - 3.89)} = 305 \text{ ps} \quad (9)$$

With timings  $t_1$ ,  $t_2$ , and  $t_3$  computed, power loss during turnon time is calculated using [Equation 10](#).

$$P_{ton} = \left( V_{IN} \times \frac{(n \times I_0)}{2} \times (t_2 - t_1) \times f_{SW} \right) + \left( n \times I_0 \times \frac{(V_{IN})}{2} \times t_3 \times f_{SW} \right) = 18.4 \mu\text{W} \quad (10)$$

Similarly, the turnoff timings  $t_4$ ,  $t_5$ ,  $t_6$ , and turnoff loss is computed as shown in [Equation 11](#), [Equation 12](#), and [Equation 13](#).

$$t_4 = (R_g + R_{ext}) \times C_{iss} \times \ln \left( \frac{V_{GS}}{V_P} \right) = (4.6 + 4.7) \times 349 \text{ pF} \times \ln \left( \frac{12}{4} \right) = 3.65 \text{ ns} \quad (11)$$

$$t_5 = (R_g + R_{ext}) \times C_{GD} \times \frac{V_{DS}}{V_P} = (4.6 + 4.7) \times 12.6 \text{ pF} \times \frac{12}{4} = 361 \text{ ps} \quad (12)$$

$$t_6 = (R_g + R_{ext}) \times C_{iss} \times \ln \left( \frac{V_P}{V_{TH}} \right) = (4.6 + 4.7) \times 349 \text{ pF} \times \ln \left( \frac{4}{3.77} \right) = 1001 \text{ ps} \quad (13)$$

With timings  $t_4$ ,  $t_5$ , and  $t_6$  computed, power loss during turnoff time is calculated using [Equation 14](#).

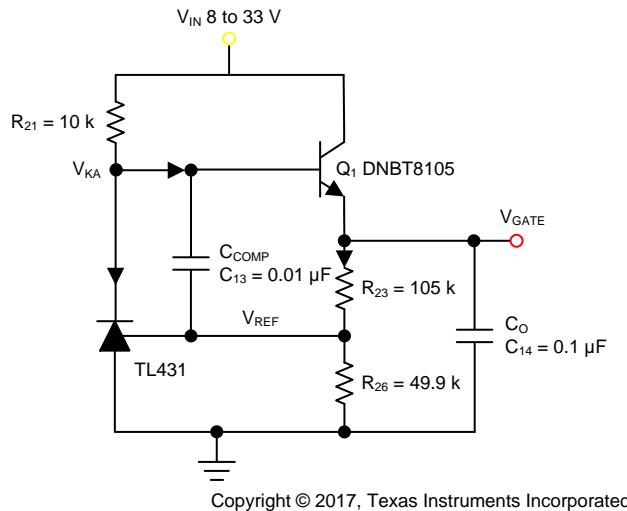
$$P_{toff} = \left( n \times I_0 \times \frac{(V_{IN})}{2} \times t_5 \times f_{SW} \right) + \left( V_{IN} \times \frac{(n \times I_0)}{2} \times t_6 \times f_{SW} \right) = 22.1 \mu\text{W} \quad (14)$$

The total power loss in MOSFET is calculated using [Equation 15](#):

$$P_T = P_{cond} + P_{GATE} + P_{ton} + P_{toff} = 1.7 \text{ mW} \quad (15)$$

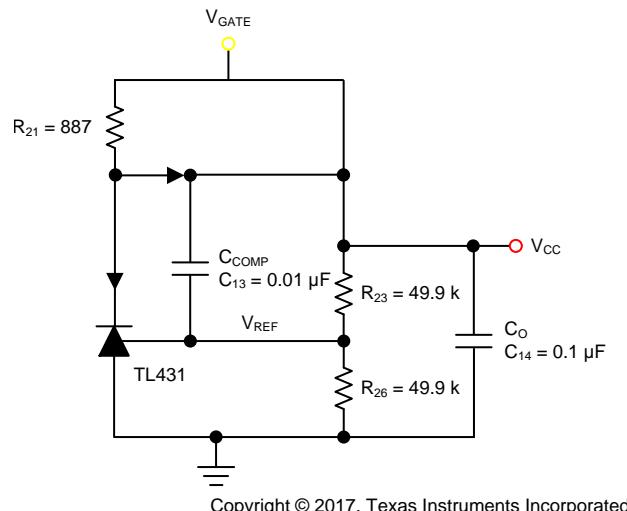
### 2.3.1.4 LDO Using TL431

The regulated gate drive supply and peripheral supply are generated using a discrete LDO designed with the TL431. This peripheral supply can be used to power up the MCU, op amp, and other peripherals in a burner control system. In this reference design, the LDO powers up the sine wave oscillator. The components in the gate drive supply as shown in [Figure 18](#) is computed as per Section 2.2.2.1 of the [TIDA-01065 design guide](#) with a feedback current of 50  $\mu$ A. The capacitor  $C_{13}$  is introduced for stability by adding zero in the feedback loop. This capacitor improves the phase margin and reduces oscillation in output.



**Figure 18. Gate Voltage Supply**

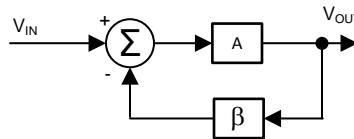
The peripheral LDO is designed with an output current of 1 mA and 5 V. The values of discrete components as shown in [Figure 19](#) are computed as per Section 2.2.2.1 of the [TIDA-01065 design guide](#) with a feedback current of 50  $\mu$ A. The capacitor  $C_{13}$  is introduced for stability by adding zero in the feedback loop. This capacitor improves the phase margin and reduces oscillation in output.



**Figure 19. Peripheral Supply**

### 2.3.1.5 Sine Wave Oscillator

In this reference design, a sine wave oscillator is used to generate a 50-Hz line signal by using a low THD+noise op amp. With this approach, it is possible to produce very low distorted output. As shown in Figure 20, the oscillator must satisfy the criteria for a closed loop positive feedback for the circuit to oscillate. Due to positive feedback, the denominator value becomes zero, resulting in instability known as Barkhausen Criterion. In unstable mode, the output of circuit tends to infinity due to the limitation of the power rail in circuit output will saturate to rail supply. For active devices, the gain of the circuit changes as output approaches the supply rail. This results in a change of value A and forces  $A\beta$  away from the singularity. Due to this change, trajectory towards power rail slows and eventually halts.



$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta}$$

if  $A\beta = -1 = 1 \neq -180$

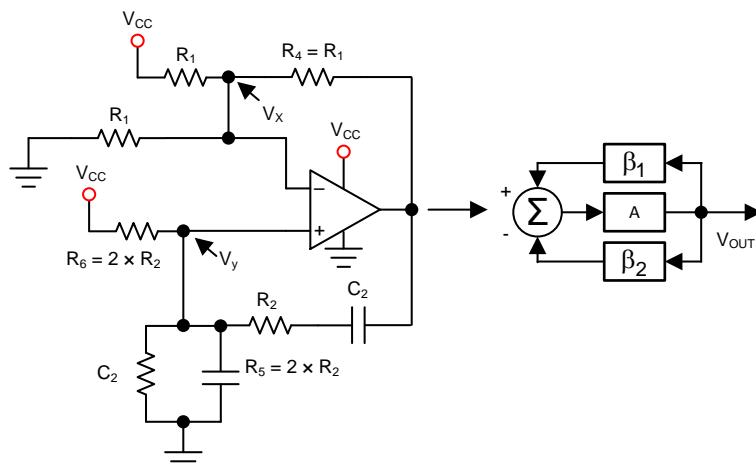
**Figure 20. Oscillator Control Loop**

At this point, any one of these three possible conditions can occur:

- Nonlinearity in saturation or a cutoff region may result to become stable and latch at a particular output
- Initial change may cause the active device to be saturated or cut off for a long period before becoming linear and then moving to an opposite rail
- The circuit stays linear and reverses polarity to an opposite rail

The second condition results in a distorted output and is usually preferred for generating quasi square wave signals, while the third conditions produces sine wave output. The gain and phase of the circuit play a critical role for designing a sine way oscillator. For an op-amp based circuit, the phase margin of the op amp must be negligible so that the closed loop positive feedback achieves  $\angle -180$  phase shift at oscillating frequency. Considering these conditions, the closed loop gain, phase shift, THD distortion, and slew rate are some key parameters for selecting an op amp to design sine wave oscillators.

This reference design uses a single-supply Wein bridge oscillator. The classic Wein bridge oscillator has both positive and negative feedback. This helps in getting a very low distorted output. For analysis, consider the circuit as shown in Figure 21. The circuit operating can be modeled as a non-inverting amplifier.



**Figure 21. Sine Wave Oscillator for Op Amp**

Voltage at the positive terminal of the op amp is given using [Equation 16](#).

$$V_y = V_O \times \left( \frac{sR_2C_2}{1 + 3sR_2C_2 - (sR_2C_2)^2} \right) \quad (16)$$

A simple form of [Equation 16](#) in a frequency parameter is given using [Equation 17](#).

$$\beta = \frac{V_y}{V_O} = \frac{1}{3 + j \left( \frac{f}{f_{R_2C_2}} - \frac{f_{R_2C_2}}{f} \right)}, \text{ where } f_{R_2C_2} = \frac{1}{2\pi R_2 C_2} \quad (17)$$

From a classic non-inverting amplifier, the closed loop gain equation ignoring the dominant pole effect at a low frequency is given using [Equation 18](#).

$$V_O = V_y \times \left( 1 + \frac{R_4}{R_1} \right) \quad (18)$$

As a result, the forward gain is found using [Equation 19](#).

$$A = \frac{V_O}{V_y} = \left( 1 + \frac{R_4}{R_1} \right) \quad (19)$$

The total loop gain is given using [Equation 20](#).

$$T(jf) = A\beta = \frac{\left( 1 + \frac{R_4}{R_1} \right)}{\left( 3 + j \left( \frac{f}{f_{R_2C_2}} - \frac{f_{R_2C_2}}{f} \right) \right)} \quad (20)$$

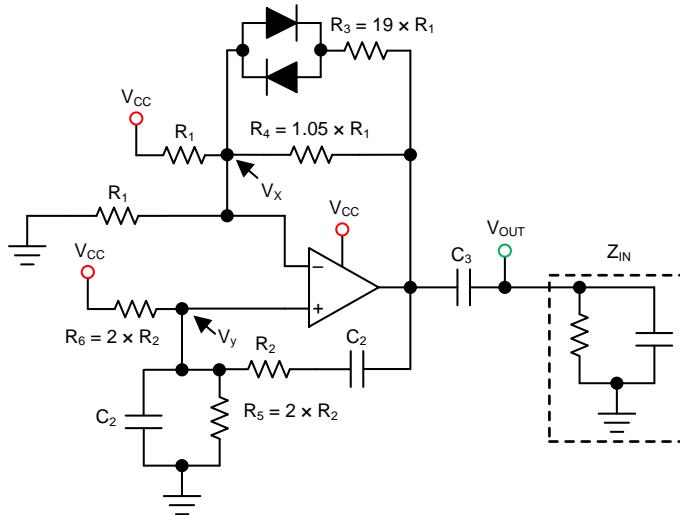
These equations imply system response of bandpass filter, at higher and lower frequency it approaches to zero and at peak frequency of  $f = f_{R_2C_2}$ , the total loop gain reduces to:

$$t(f_{R_2C_2}) = \frac{\left( 1 + \frac{R_4}{R_1} \right)}{3} \quad (21)$$

The magnitude of the total loop gain has three possibilities:

- $T(jf_{R_2C_2}) < 1$ : The pole pair lies in the left half of the complex plane, resulting in an exponentially decaying signal.
- $T(jf_{R_2C_2}) > 1$ : This condition results in unstable operation, resulting in oscillation of growing amplitude. The pole pair lies on the right half of a complex plane. The oscillation builds up until the op amp saturates to the power rail. This condition results in a distorted output.
- $T(jf_{R_2C_2}) = 1$ : This condition results in neutral stability. The pole pair lies exactly on an imaginary axis of the complex plane. It satisfies the Barkhausen criterion of the loop gain of unity and a phase shift of 360°. The output is sinusoidal with very low distortion. For this condition, the  $R_4/R_1$  ratio needs to satisfy a magnitude of 2.

Due to the drift of active and passive devices, the total loop gain does not maintain a magnitude of value 1, so modify the circuit as shown in [Figure 22](#) to achieve automatic gain control (AGC). At initial startup condition, diodes D<sub>1</sub>, D<sub>2</sub>, and R<sub>3</sub> result into condition T(jf<sub>R2C2</sub>) > 1, resulting into oscillations quickly building up. After the oscillation has built up, the gain stabilizes to match the Barkhausen criteria due to effective resistors R<sub>3</sub> and R<sub>4</sub>, which are in parallel to achieve a ratio close to a magnitude of 2.



**Figure 22. Practical Op Amp Oscillator**

Select an op amp that has very low distortion for oscillating frequency, low noise, and enough of a slew rate to achieve sustain oscillation. The closed loop bandwidth needs to be greater than  $270 f_{\text{osc}}$ . Therefore, for a 50-Hz  $f_{\text{osc}}$  signal, the sine wave oscillator needs a closed-loop bandwidth greater than 13.5 kHz and a slew rate of  $> 2\pi f_{\text{osc}} V_o$ . Selecting TLV171 from the device datasheet gets a unity gain bandwidth of 3 MHz and a typical open loop gain of 130 dB.

**Table 5. TLV171 Electrical Characteristic**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>					
V <sub>OS</sub>	V <sub>A</sub> = 25°C	—	0.75	±2.7	mV
	V <sub>A</sub> = -40°C to +125°C	—	—	±3.0	
dV <sub>OS</sub> /dT	V <sub>A</sub> = -40°C to +125°C	—	1	—	µV/°C
PSRR	V <sub>S</sub> = 4 V to 36 V, T <sub>A</sub> = -40°C to +125°C	90	105	—	dB
<b>INPUT BIAS CURRENT</b>					
I <sub>B</sub>	Input bias current	—	—	±10	pA
I <sub>os</sub>	Input offset current	—	—	±4	pA
<b>NOISE</b>					
e <sub>n</sub>	Input voltage noise	f = 0.1 Hz to 10 Hz	—	3	—
		f = 100 Hz	—	27	—
		f = 1 kHz	—	16	nV/vHz
<b>INPUT VOLTAGE</b>					
V <sub>CM</sub>	Common-mode voltage range	—	(V-) - 0.1	—	(V+) - 2
CMRR	V <sub>S</sub> = ±18 V, (V-) - 0.1 V < V <sub>CM</sub> < (V+) - 2 V, T <sub>A</sub> = -40°C to +125°C	94	105	—	dB
<b>INPUT IMPEDANCE</b>					
Differential	—	—	100    3	—	MΩ    pF
	—	—	6    3	—	10 <sup>12</sup> Ω    pF
Common-mode	—	—	—	—	—
	—	—	—	—	—

**Table 5. TLV171 Electrical Characteristic (continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OPEN-LOOP GAIN</b>					
A <sub>OL</sub> Open-loop voltage gain	V <sub>S</sub> = 36 V, (V-) + 0.35 V < V <sub>O</sub> < (V+) - 0.35 V, T <sub>A</sub> = -40°C to +125°C	94	130	—	dB
<b>FREQUENCY RESPONSE</b>					
GBP Gain bandwidth product	—	—	3.0	—	MHz
SR Slew rate	G = +1	—	1.5	—	V/μs
t <sub>s</sub> Settling time	To 0.1%, V <sub>S</sub> = ±18 V, G = +1, 10-V step	—	6	—	μs
	To 0.01% (12 bits), V <sub>S</sub> = ±18 V, G = +1, 10-V step	—	10	—	
Overload recovery time	V <sub>IN</sub> × gain > V <sub>S</sub>	—	2	—	μs
THD+N Total harmonic distortion + noise	G = +1, f = 1 kHz, V <sub>O</sub> = 3 V <sub>RMS</sub>	—	0.0002%	—	—

As a result, the dominant pole frequency of the TLV171 is given using [Equation 22](#).

$$f_{\text{dom}} = \frac{f_{\text{unity}}}{10^{20}} = \frac{130}{10^{20}} = 0.948 \text{ Hz} \quad (22)$$

The closed loop AC gain for a non-inverting topology with a feedback factor of 1/3 at a frequency of 15 kHz is given using [Equation 23](#).

$$A_{\text{cl}} = \frac{\frac{A_{\text{DC\_OPEN}}}{1 + \beta \times A_{\text{DC\_OPEN}}}}{\sqrt{1 + \frac{f^2}{f_{\text{dom}}^2} \frac{1}{(1 + \beta A_{\text{DC\_OPEN}})^2}}} = \frac{\frac{3162277}{1 + 0.33 \times 3162277}}{\sqrt{1 + \left(\frac{15000^2}{0.948^2}\right) \times \left(\frac{1}{(1 + 0.33 \times 3162277)^2}\right)}} = 3.029 \quad (23)$$

So the TLV171 meets approximately a closed loop gain of 3. Calculate the phase margin error using [Equation 24](#) to get a phase error of 0.003°.

$$\phi = 90^\circ - \left( \tan^{-1} \frac{f}{f_{\text{dom}}} \right) = 0.003^\circ \quad (24)$$

From the slew rate requirement, considering an output voltage of 4 V and a 50-Hz f<sub>OSC</sub> slew rate needs to be greater than 1.25 mV/μs (ignoring asymmetric slew rate error in non-inverting mode due to a common-mode parasitic).

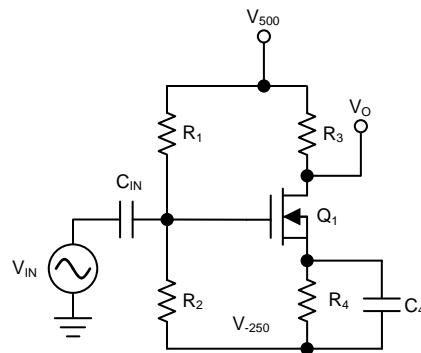
$$\text{SR} > 2\pi \times f_{\text{OSC}} \times V_O \times 10^{-6} = 2\pi \times f_{\text{OSC}} \times V_O \times 10^{-6} > 1.25 \frac{\text{mV}}{\mu\text{s}} \quad (25)$$

By cross verifying with the TLV171 FPB, check that the slew rate satisfies the closed loop bandwidth requirement by using [Equation 26](#).

$$\text{FPB} = \frac{\text{SR in } \frac{\text{V}}{\mu\text{s}}}{2\pi \times V_O} = \frac{1.5 \times 10^6}{8\pi} = 59.7 \text{ kHz} \quad (26)$$

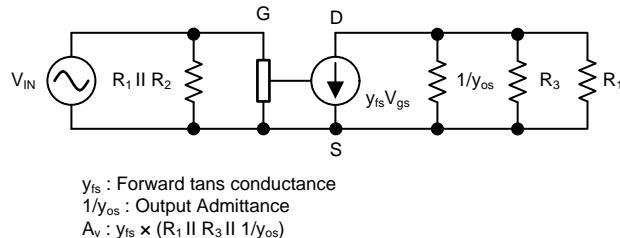
### 2.3.1.6 High Gain Amplifier

To achieve a 120-V sine wave output, there needs to be an amplifier; this amplifier can be a topology like Class A, Class AB, and so on. To achieve the cost target, a Class A amplifier has been implemented in this reference design. Class AB can be implemented to achieve high efficiency and low distortion with a filter circuit. A Class A amplifier as shown in [Figure 23](#) operates in the linear operating region, due to which output distortion are low. In a Class A amplifier, additional quiescent current is required to bias the transistor in the operating region. Calculate the bias point to achieve linear output. This reference design uses the BSS127-S N-channel, high-voltage, low-cost MOSFET to design this Class A amplifier.



**Figure 23. Class A Amplifier**

Resistors  $R_1$  and  $R_2$  provide bias voltage to  $Q_1$ . To calculate  $R_1$  and  $R_2$ , first calculate the Q point of  $Q_1$  for the required gain. The AC equivalent of a circuit is as shown in [Figure 24](#).



**Figure 24. AC Equivalent Circuit**

The drain current of the MOSFET is parabolic in nature, so the drain current is given using [Equation 27](#).

$$I_{ds} = K \times (V_{GSON} - V_{GSOFF})^2 \quad (27)$$

Solving [Equation 27](#) for  $V_{GSON} = 10$  V,  $V_{GSOFF} = 3$  V, and  $I_{ds} = 16$  mA from the datasheet, compute K as shown in [Equation 28](#).

### Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>PSS</sub>	600	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	0.1	μA	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V
Gate-Body Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	3	—	4.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	80	160	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 16mA
		—	95	190		V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 16mA
Forward Transfer Admittance	Y <sub>f</sub>	—	76	—	mS	V <sub>DS</sub> = 10V, I <sub>D</sub> = 16mA
Diode Forward Voltage	V <sub>SD</sub>	—	—	1.5	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 16mA
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	—	21.8	—	pF	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	2.2	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	0.3	—		
Total Gate Charge	Q <sub>g</sub>	—	1.08	—	nC	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 300V, I <sub>D</sub> = 0.01A
Gate-Source Charge	Q <sub>gs</sub>	—	0.08	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	0.50	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	5.0	—	ns	V <sub>DD</sub> = 300V, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 6Ω, I <sub>D</sub> = 10mA
Turn-On Rise Time	t <sub>R</sub>	—	7.2	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	28.7	—	ns	
Turn-Off Fall Time	t <sub>F</sub>	—	168	—	ns	
Reverse Recovery Time	t <sub>RR</sub>	—	131	—	ns	V <sub>R</sub> = 300V, I <sub>F</sub> = 0.016A, di/dt = 100A/μs
Reverse Recovery Charge	Q <sub>RR</sub>	—	32	—	nC	

- Notes:
5. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
  6. Device mounted on 1" x 1" FR-4 PCB with high coverage 2 oz. Copper, single sided.
  7. Repetitive rating, pulse width limited by junction temperature, 10μs pulse, duty cycle = 1%.
  8. Short duration pulse test used to minimize self-heating effect.
  9. Guaranteed by design. Not subject to production testing.

**Figure 25. MOSFET Electrical Characteristics**

$$k = \frac{dI_{dsq}}{dV_{GSq}} = 2 \times K \times (V_{GSq} - V_{GSOFF}) \quad (28)$$

The transconductance of the MOSFET is found by taking the derivative of the transfer function for the drain current at a bias point of the amplifier.

$$y_{fq} = \frac{dI_{dsq}}{dV_{GSq}} = 2 \times K \times (V_{GSq} - V_{GSOFF}) \quad (29)$$

Assuming the high load resistance and output admittance is sufficiently high, the impedance seen by the MOSFET is almost equal to R<sub>3</sub>. For a good biasing point, it is good to bias the output at half of the supply rails. As a result, the drain resistance is given using [Equation 30](#).

$$R_3 = 0.5 \times \frac{(V_{DD} + V_{SS})}{I_{DQ}} \quad (30)$$

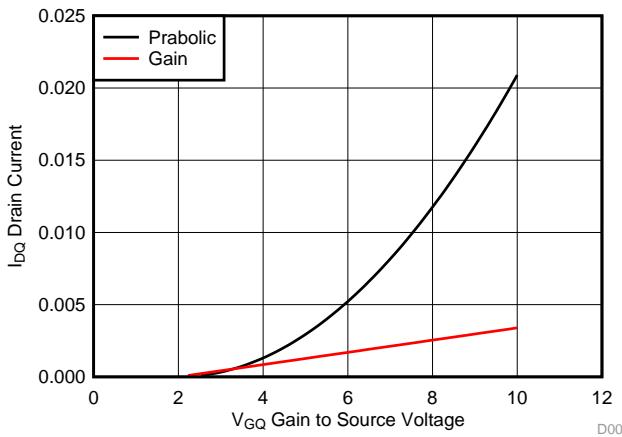
By substituting R<sub>3</sub> and y<sub>fq</sub> for the total gain in [Equation 31](#):

$$A_{vq} = y_{fq} \times R_3 = 2 \times K \times (V_{GSq} - V_{GSOFF}) \times 0.5 \frac{(V_{DD} - V_{SS})}{I_{DQ}} \quad (31)$$

Rearranging the terms for I<sub>DQ</sub> leads to [Equation 32](#):

$$I_{DQ} = \frac{2 \times K \times (V_{GSq} - V_{GSOFF}) \times 0.5 \times (V_{DD} - V_{SS})}{A_{vq}} \quad (32)$$

Solving [Equation 27](#) and [Equation 32](#) graphically with  $V_{dd}$  of 500 V,  $V_{GSOFF} = 3$  V and a gain of 330, bias points  $V_{GSQ}$  and  $I_{DQ}$  can be computed using interpret of two curves (see [Figure 26](#)).



**Figure 26. Bias Point Calculations**

[Figure 26](#) shows that the curve intercepts the x-axis at 3.3 V and the y-axis at 551  $\mu$ A. So the bias point for BSS127-S is  $V_{GSQ} = 3.3$  V and  $I_{DQ} = 551 \mu$ A.

Solving the equation with  $I_{DQ} = 551 \mu$ A results in  $R_3 = 442$  k $\Omega$ . Selecting a closed standard value of 442 k $\Omega$  at the source can be set close to 0.09 times the supply rail. Computing for a  $V_{dd}$  of 500 V and  $I_{DQ} = 551 \mu$ A results in  $R_4 = 82$  k $\Omega$ . Selecting the next standard resistor with a 5% tolerance we select 88.7 k $\Omega$ . With 88.7 k $\Omega$  and  $I_{DQ} = 551 \mu$ A, the source voltage is 48.8 V. Adding the gate-to-source bias voltage, the gate voltage needs to be 52.1 V. Using voltage divider logic, R1 and R2 can be easily computed for a low-bias current. Assuming an R<sub>2</sub> of 2.2 M $\Omega$  and a supply rail  $V_{dd}$  of 500 V, the required resistance R<sub>1</sub> is 18 M $\Omega$ . The nearest standard value to select is 18 M $\Omega$ . Capacitance C<sub>4</sub> is a bypass capacitor for a higher AC gain value. To calculate C<sub>4</sub>, assume impedance by capacitance for a 50-Hz frequency as 0.1 times of R<sub>4</sub>.

$$X_C = 0.1 \times R_4 = 8.8 \text{ k}\Omega \quad (33)$$

By knowing the impedance of a capacitor at a specific frequency, it is easy to calculate capacitance using [Equation 34](#).

$$C_4 = \frac{1}{2\pi f X_C} = 361 \text{ nF} \quad (34)$$

The next standard value selected is a 470-nF capacitor. Capacitance C<sub>in</sub> is a high-pass-filter capacitor that blocks DC level from the oscillator output. The parallel resistance value of resistors R<sub>1</sub> and R<sub>2</sub> with C<sub>in</sub> together form the high pass filter. By selecting a cutoff frequency of 5 Hz, compute C<sub>in</sub> as per [Equation 35](#).

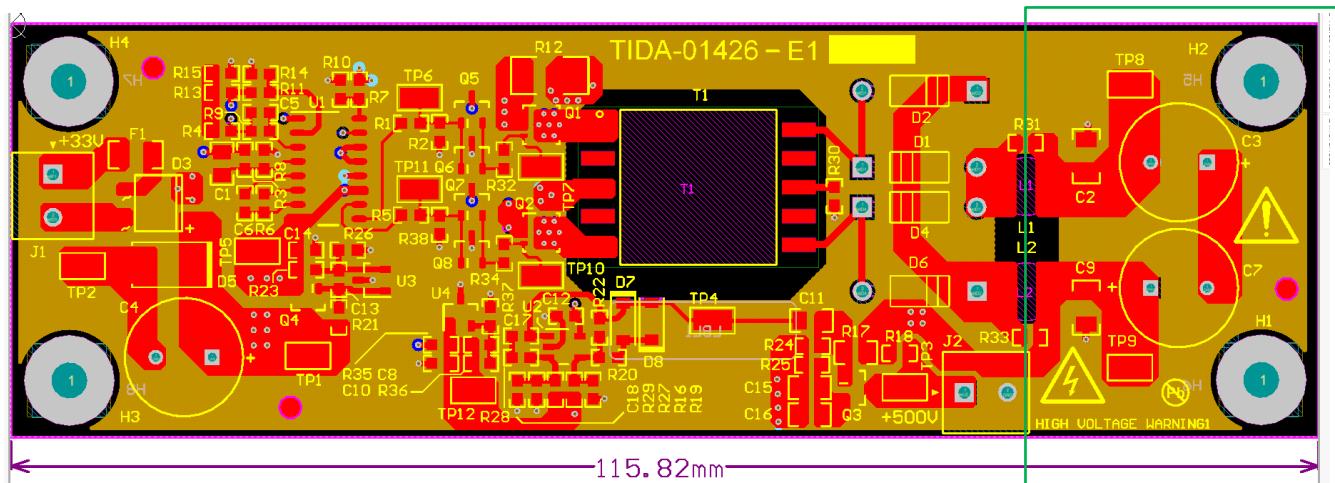
$$C_{in} = \frac{1}{2\pi f_C \times 0.1 \times (R_1 \| R_2)} = 162 \text{ nF} \quad (35)$$

The next standard value of 220 nF is selected for the input filter capacitor.

### 3 Hardware, Testing Requirements, and Test Results

#### 3.1 Hardware

Before powering up the TIDA-01426 board, verify for any components not populated as per the schematic. Check for power nodes and shock hazard symbols to avoid electric shocks as shown in [Figure 27](#).



**Figure 27. High-Voltage Section**

##### 3.1.1 Connectors

The interface board has two connectors as described in [Table 6](#).

**Table 6. Input Output Connectors**

CONNECTOR	DESCRIPTION	VOLTAGE
J1	Input voltage	12 to 36 V
J2	Output voltage	120 V <sub>RMS</sub> , 60 Hz

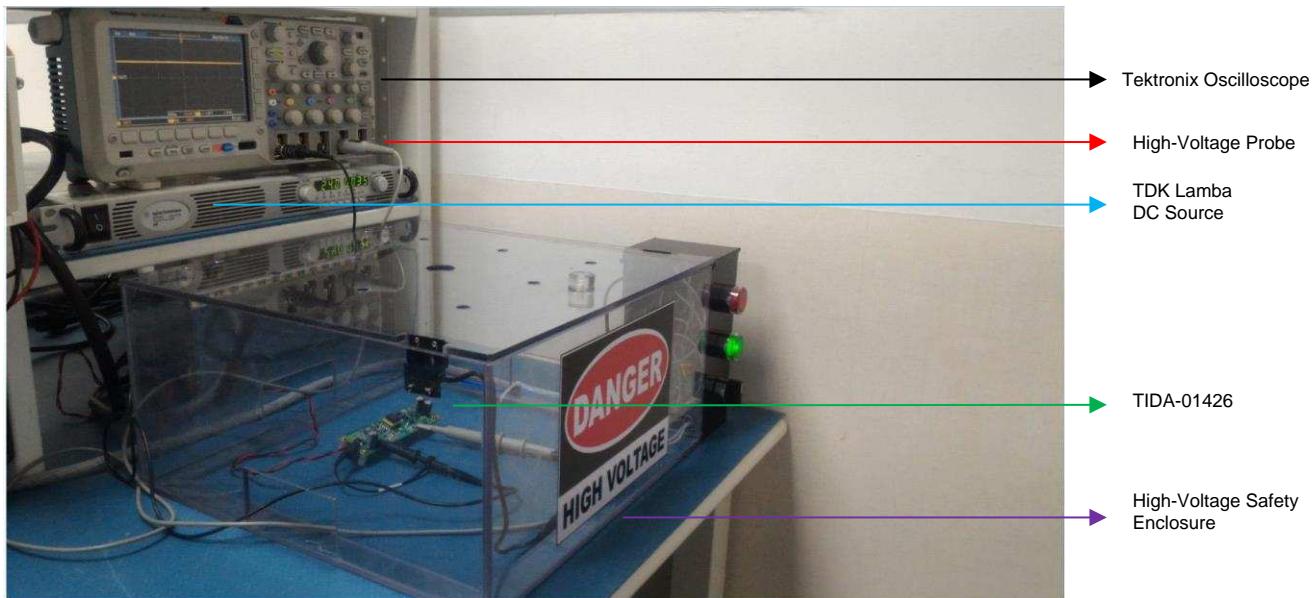
##### 3.1.2 Test Points

The required test points have been populated on the interface board to measure signals. See [Table 7](#) for more details.

**Table 7. Test Points**

TEST POINT NO	DESCRIPTION	VOLTAGE VALUE
TP1	Supply voltage	12 to 36 V
TP2, TP9	GND	0 V
TP5	Gate supply	8 V
TP12	Op amp supply	5 V
TP4	Sine wave oscillator	1.5 V <sub>RMS</sub> , 60 Hz
TP3	Class A amplifier output	120 V <sub>RMS</sub> , 60 Hz
TP6	Emitter 1 output	7-V, 100-kHz PWM
TP11	Emitter 2 output	7-V, 100-kHz PWM
TP7	Totem Pole 1 output	8-V, 100-kHz PWM
TP10	Totem Pole 2 output	8-V, 100-kHz PWM
TP8	Positive high voltage	500 V

The test setup is as shown in [Figure 28](#). Ensure the board is placed inside a safety enclosure to prevent any shock or short-circuit hazard.



**Figure 28. Test Setup**

## 3.2 Testing and Results

### 3.2.1 Gate Supply

The following figures show the gate output voltage changes as the line voltage changes from the minimum supply to the maximum supply.

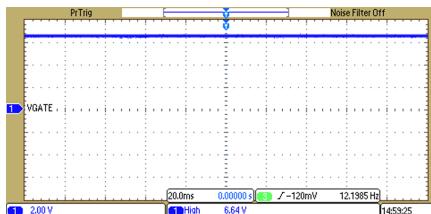


Figure 29. Gate Supply at 12 V<sub>IN</sub>

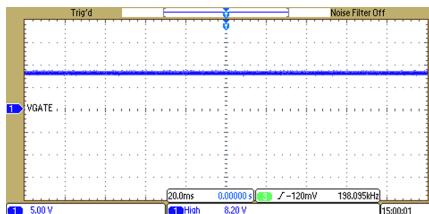


Figure 30. Gate Supply at 24 V<sub>IN</sub>

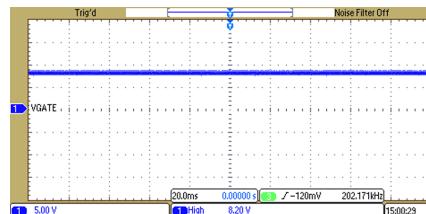


Figure 31. Gate Supply at 33 V<sub>IN</sub>

### 3.2.2 LDO Supply

The following figures show the LDO output voltage as the line voltage changes from the minimum supply to the maximum supply.

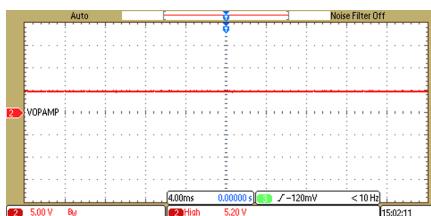


Figure 32. LDO Supply at 12 V<sub>IN</sub>

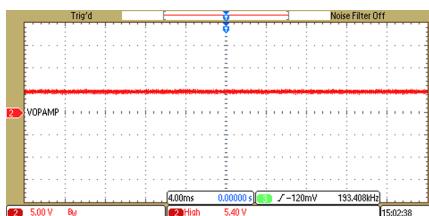


Figure 33. LDO Supply at 24 V<sub>IN</sub>

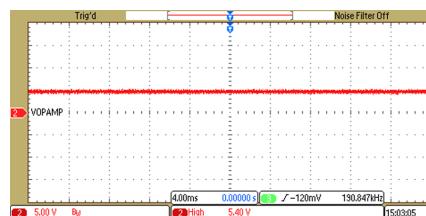


Figure 34. LDO Supply at 36 V<sub>IN</sub>

### 3.2.3 Push-Pull Output

The start-up time for 500 V is tested at the lowest input supply. You get a start-up time of 100 ms to achieve 55 ms as shown in Figure 35.

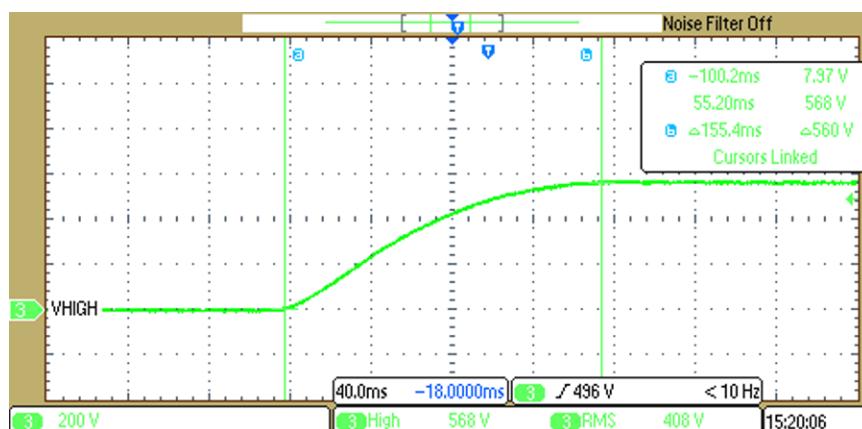
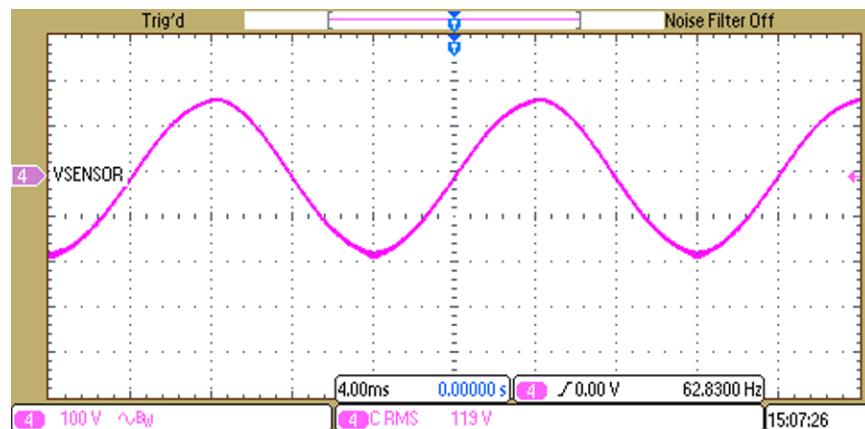


Figure 35. Start-up Time

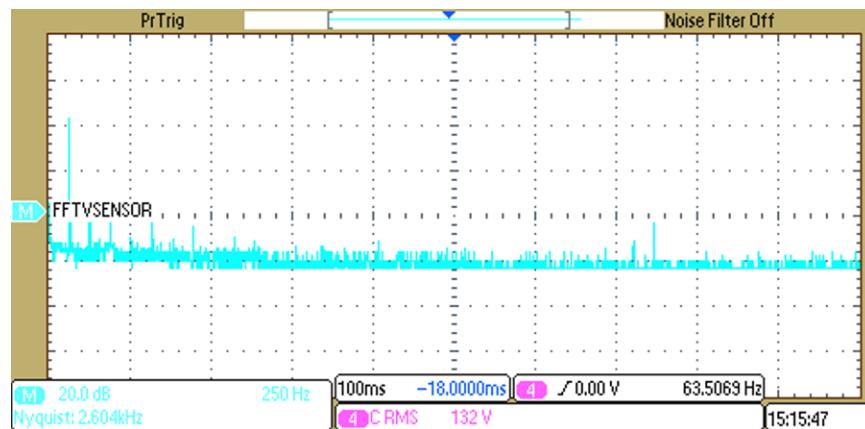
### 3.2.4 Sensor Output

Sensor output is measured at a 24-V input, and the FFT plot is taken to verify harmonic content (see Figure 36).



**Figure 36. Sensor Output**

As seen from Figure 37, the peak is at 63 Hz with a 42-dB magnitude and harmonics with magnitudes of 7 dB, -18 dB, -12 dB, and -5 dB. The THD computed for an observed output is 1.8%.



**Figure 37. FFT Plot Sensor Output**

## 4 Design Files

### 4.1 Schematics

To download the schematics, see the design files at [TIDA-01426](#).

### 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01426](#).

### 4.3 PCB Layout Recommendations

#### 4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01426](#).

### 4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01426](#).

### 4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01426](#).

### 4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01426](#).

## 5 Software Files

To download the software files, see the design files at [TIDA-01426](#).

## 6 Related Documentation

1. Texas Instruments, [Designing Switching Voltage Regulators With the TL494](#), TL494 Application Report (SLVA001)

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.

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## 7 About the Authors

**SRINIVASAN IYER** is a systems engineer at Texas Instruments India, where he is responsible for developing reference design solutions for the industrial segment. Srinivasan has six years of experience in power supply and analog circuit designs for field transmitter and signal chain. Srinivasan received his BE from the University of Pune, India.

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