DelSig_I2CM Example Project
1.00

Features

- 8-channel sequenced Delta Sigma ADC
- I2C Master
- Easy debugging using Character LCD
- Exception Handling

General Description

This example project is also a PSoC Creator starter design. This design shows a 16-bit differential ADC, hardware multiplexed into 8 channels, and transported over I2C. To test this design, an I2C Slave project (DelSig_I2CM_Test) is available as a separate example project.

This starter design also includes advanced debugging techniques to detect and handle system level faults and conditions, such as a missing wire or missing device on the bus. The PSoC 0.1% internal voltage reference shows the additional BOM integration.

This design makes it easy to get started and utilize precision analog capability of PSoC.

Development kit configuration

The following configuration instructions provide a guideline to test this design with the DelSig_I2CM_Test example project. For simplicity, the instructions describe the stepwise process to follow when testing this design with 2 PSoC Development Kits (CY8CKIT-001), but can be generalized for the PSoC 3 Development Kit (CY8CKIT-030) and PSoC 5 Development Kit (CY8CKIT-050) as well.

1. Set LCD power jumper J12 to ON position and position jumpers for Vdd, Vdda and Vddd to be at 5V for both the main and test board.
2. In order to generate different voltages to test the Example Project, set up a resistor ladder on the breadboard available on the CY8CKIT-001 (See Figure 2). Use 7 resistors of 10k ohm in series, followed by a 0 ohm resistor or jumper wire to ground. Starting from the top of the first 10k resistor tap each point of the resistor ladder to P0[0] to P0[6]. The zero-ohm resistor tap is sent to P1[4], and P2[7] is also connected to ground. Finally, connect the current output of the IDAC – from P0[7] to the top of the resistor ladder – P0[0].
3. For I2C communication, connect P12[0] to SCL, P12[1] to SDA. Use 2 external 2.67k resistors to pull-up SCL and SDA to 5V (Figure 1). Note that Figure 1 is a depiction for the

purpose of understanding the external connections and not the actual PSoC Creator schematic (Figure 2).

4. Externally connect the corresponding pins (SCL and SDA) on I2C Master board to the Slave (SCL and SDA) as depicted in Figure 1.

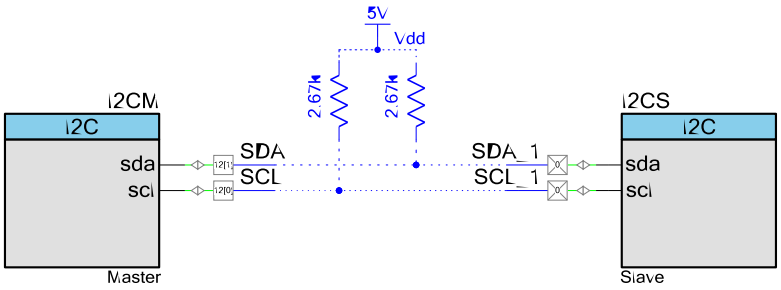

Figure 1. Connection of SDA and SCL to pull-up resistors

5. Connect the Character LCD to P2[6:0] on both boards.
6. Ensure that the grounds of the two boards are tied together.
7. Build the DelSig_I2CM project and then program the hex file onto the master board, and repeat this for the DelSig_I2CM_Test project with its corresponding board. After programming is complete, disconnect the MiniProg3.
8. Power cycle the master device and reset the slave device.

Project configuration

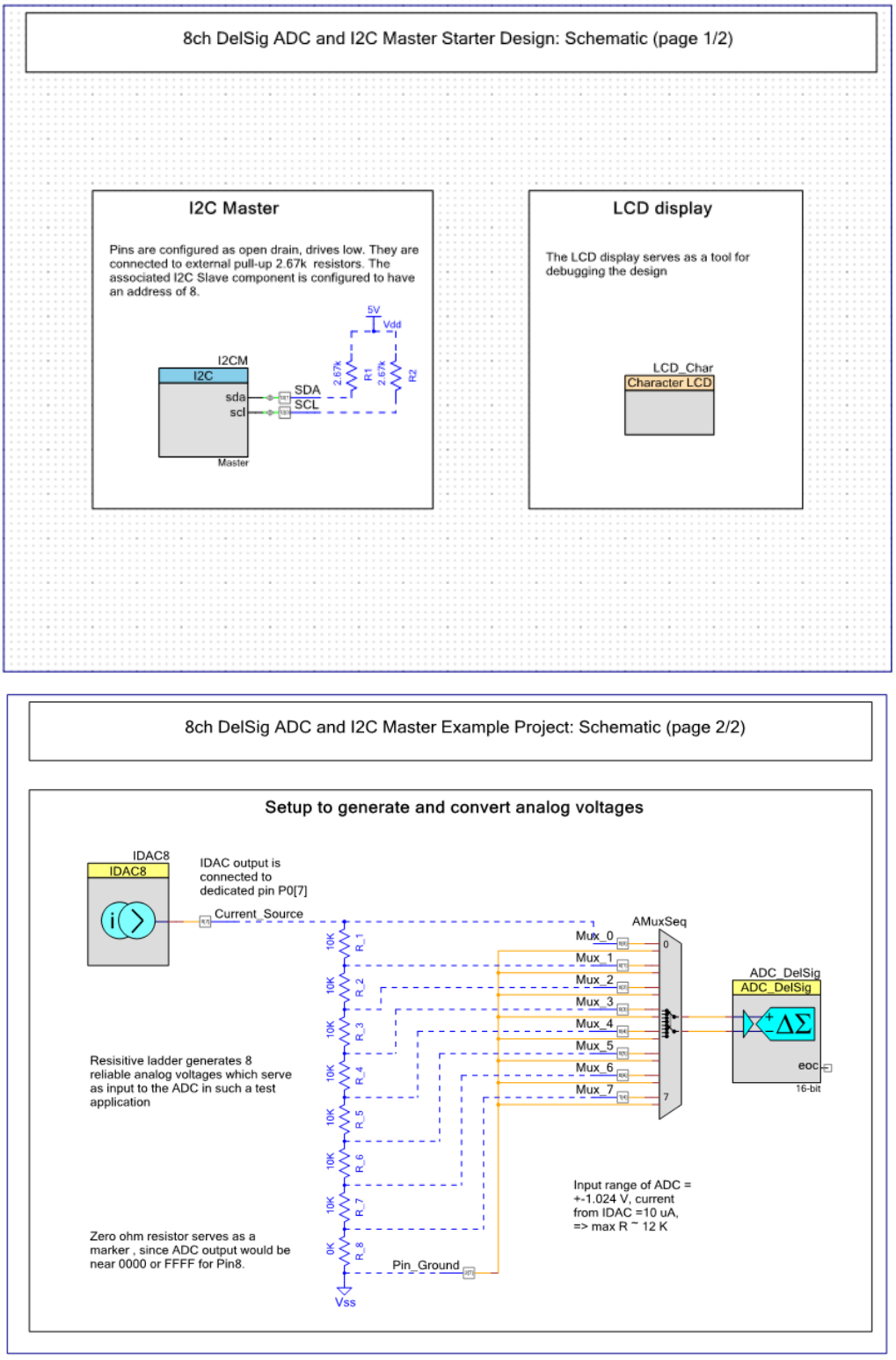

Figure 2. Schematic for the I2C Master Example Project

The top design schematic is shown in Figure 2 above. As shown in Figure 3, a Fixed Function I2C block is used, with a data rate of 100 kbps.

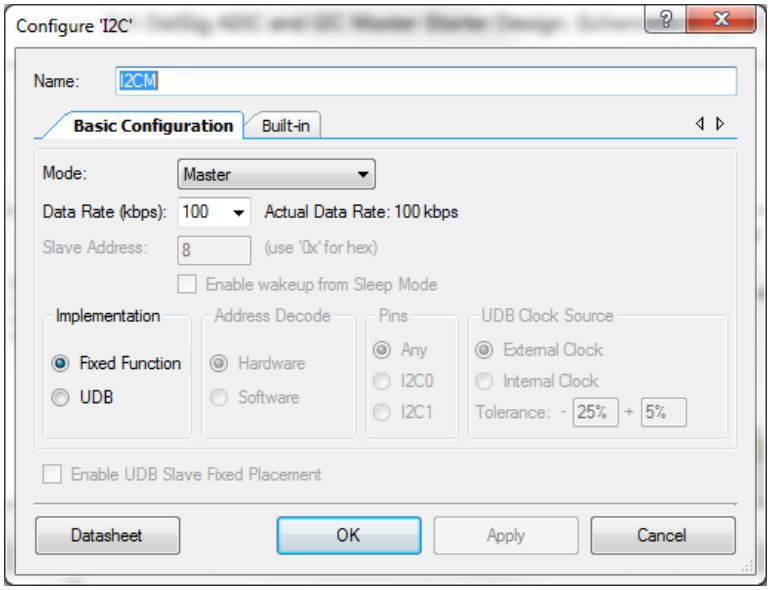

Figure 3. I2C Master Configuration

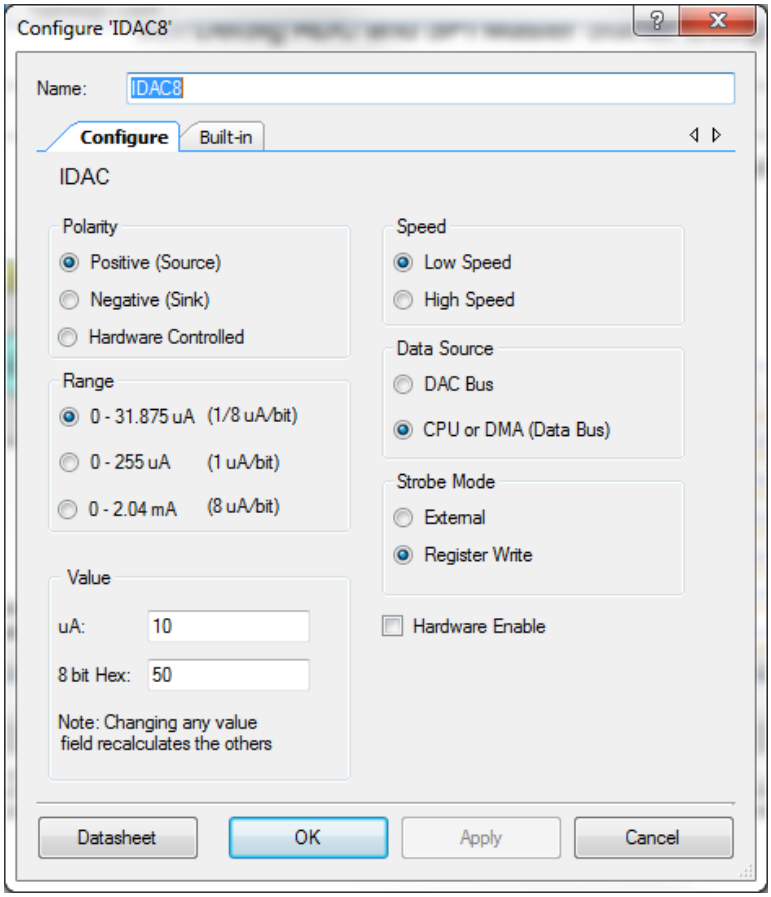

Figure 4. IDAC configuration

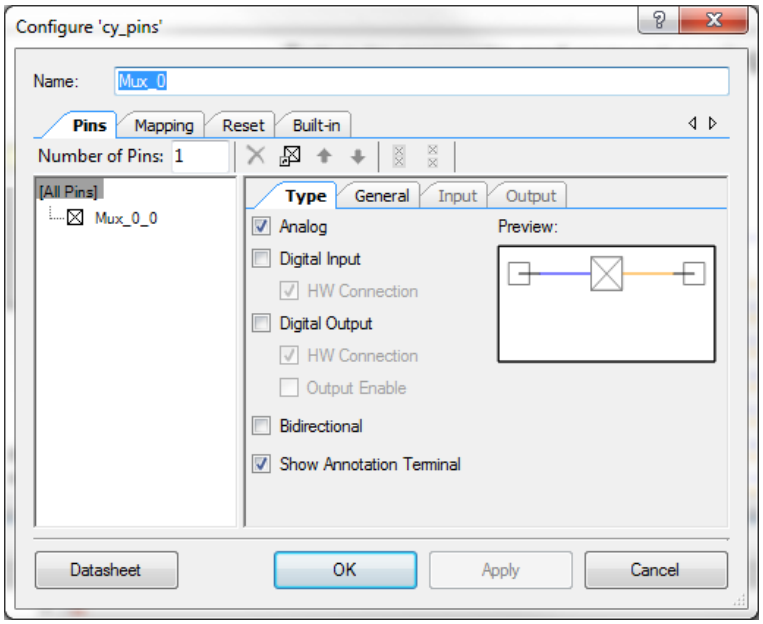

Figure 5. Configuration for the pins

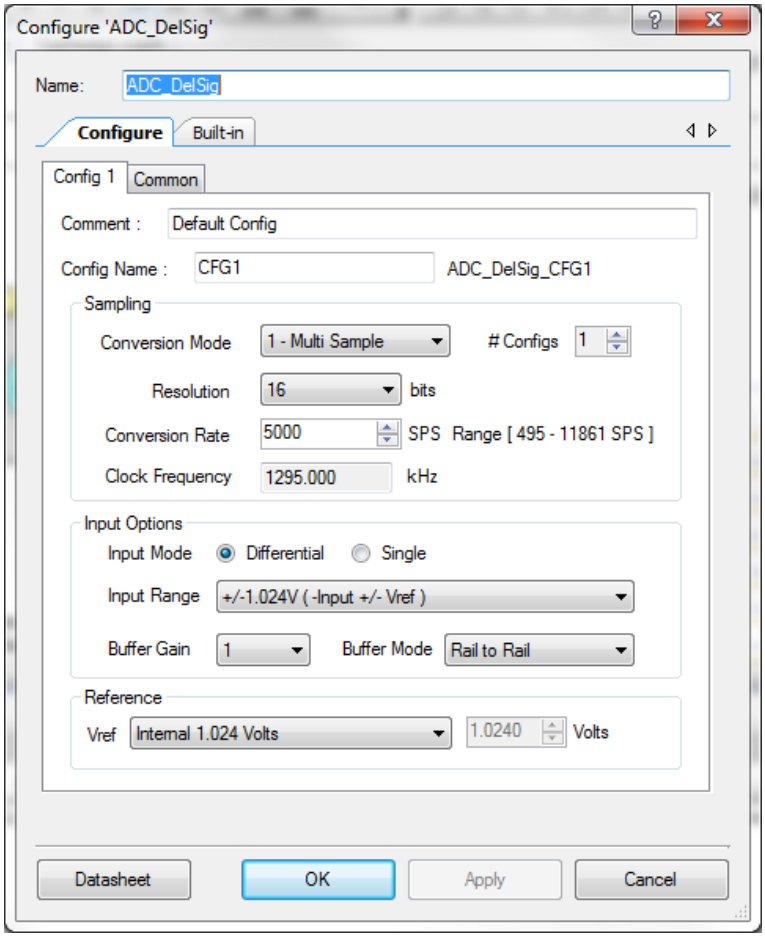

Figure 6. Delta Sigma ADC configuration

The character LCD is configured with its default settings. The IDAC is set to source current in the 0-31.875 µA range and an initial value of 10µA. This value can be adjusted according to the input range of the ADC and the value of the resistors in the resistor ladder.

The Analog Sequencing Mux is configured for 8 differential inputs, and all the analog pins are used with their default settings (Figure 5). Figure 6 shows the configuration for the Delta Sigma ADC. The test project configuration is simple – as shown in Figure 7 and Figure 8.

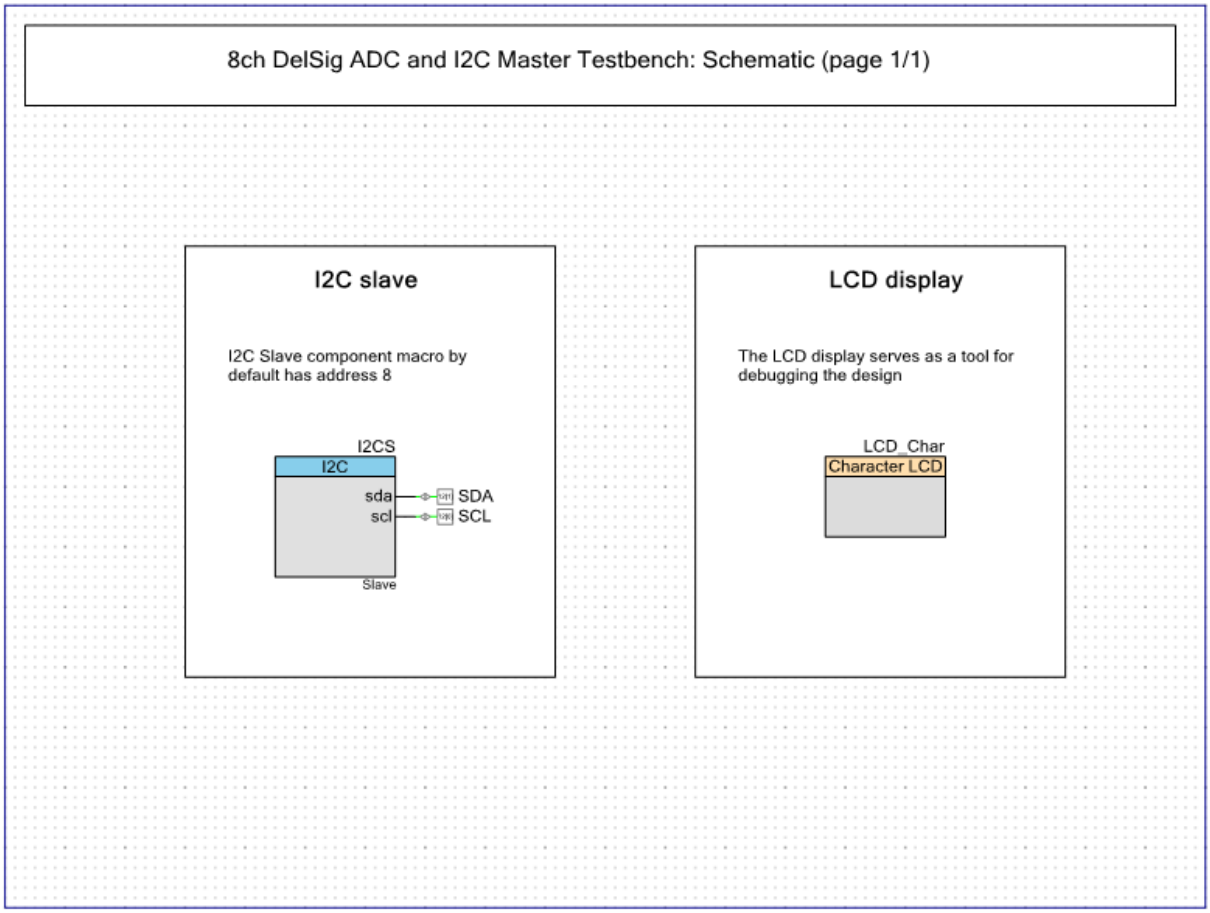

Figure 7 . I2C Slave top design schematic

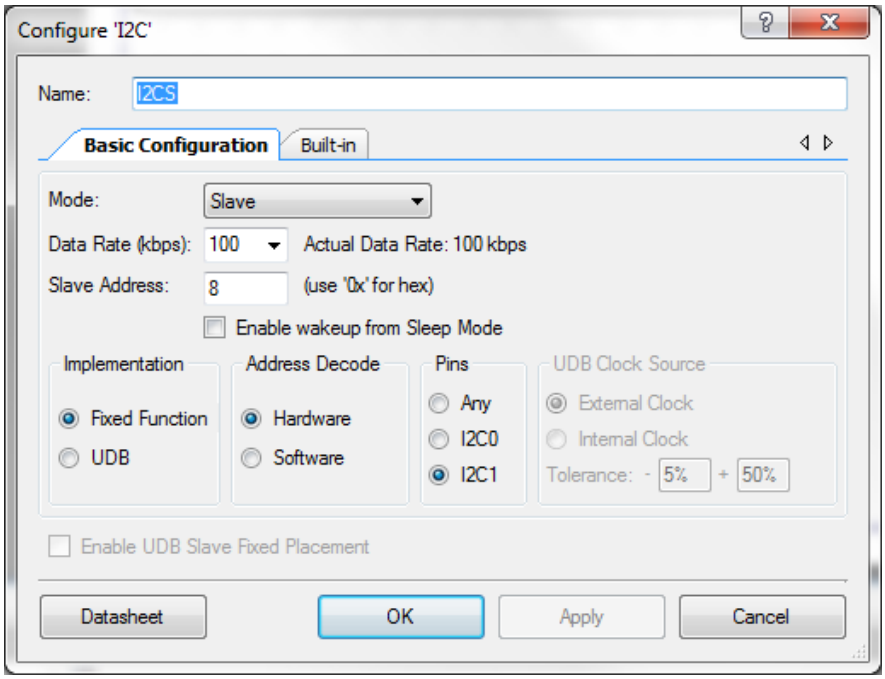

Figure 8. I2C Slave configuration

Project description

The analog voltages input to the Analog Sequencing Mux are selected in succession, one every 2 seconds (to facilitate reading of LCD). Each selected analog voltage is converted by the ADC, and transmitted over I2C using the I2C master. This digital value is also displayed in hexadecimal format on the Character LCD on the development kit. In order to make the design more robust, exception handling is built into the code.

The receiver (test) board has a pre-configured I2C slave which waits for data from the I2C master. When data arrives, this is displayed in hex using the Character LCD. The functionality is verified by checking the data displayed on the main and test board LCDs (at the same time).

Expected Results

The character LCD on the master board as well as the slave board should display the same hexadecimal representation of the analog inputs fed from the resistor ladder. The subsequent analog voltage value should appear every 2 seconds, while cycling through all 8 voltages continuously.

Related Material

Example Projects

- ADC_16Channel
- DelSig_I2CS
- DelSig_SPIM
- SAR_SPIM_USB
- ADC_DMA_VDAC

Component Datasheets

- Delta Sigma Analog to Digital Converter (ADC_DelSig) 2.20

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