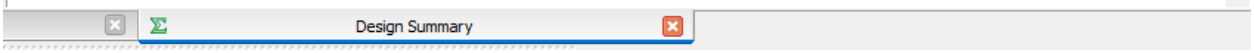
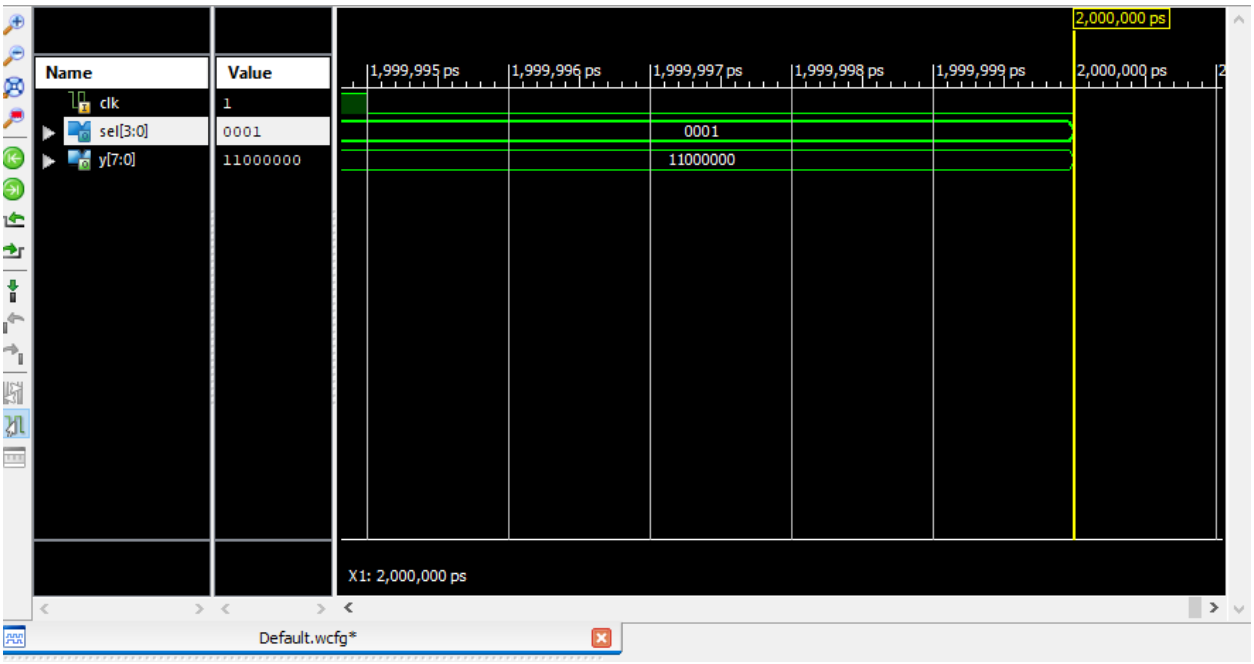
new_code Project Status			
Project File:	RTC.xise	**Parser Errors:**	No Errors
Module Name:	new_code	**Implementation State:**	Placed and Routed
Target Device:	xc3s250e-4cp132	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	2 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	183	4,896	3%	
Number of 4 input LUTs	386	4,896	7%	
Number of occupied Slices	268	2,448	10%	
Number of Slices containing only related logic	268	268	100%	
Number of Slices containing unrelated logic	0	268	0%	
Total Number of 4 input LUTs	511	4,896	10%	
Number used as logic	386			
Number used as a route-thru	125			
Number of bonded IOBs	13	92	14%	
Number of BUFGMUXs	1	24	4%	

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Sep 26 16:07:32 2023	0	2 Warnings (0 new)	1 Info (0 new)
Translation Report	Current	Tue Sep 26 16:07:54 2023	0	0	0
Map Report	Current	Tue Sep 26 16:08:13 2023	0	0	2 Infos (0 new)
Place and Route Report	Current	Tue Sep 26 16:08:57 2023	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Tue Sep 26 16:09:02 2023	0	0	6 Infos (0 new)
Bitgen Report					

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0001
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X1: 2,000,000 ps
Default.wcfg*