PALAQUE SHARMA
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EXPERIMENT NO. 1

AIM

To study and verify the Truth Tables of AND, OR, NOT, NAND, NOR, EXOR logic gates for positive logic.

REQUIREMENTS

- Prototyping board (breadboard)
- DC Power Supply 5V Battery.
- Light Emitting Diode (LED)
- Digital ICs : 7404 : Hex Inverter
  7408 : Quad 2 input AND
  7432 : Quad 2 input OR
  7400 : Quad 2 input NAND
  7402 : Quad 2 input NOR
  7486 : Quad 2 input EXOR
- Connecting Wires

THEORY

A digital logic gate is an electronic device that makes logical decisions based on the different combinations of digital signals present on its inputs. Logic gates are the building blocks of digital circuits. Combinations of logic gates form circuits designed with specific tasks in mind. They are fundamental to the design of computers. Digital logic using transistors is often referred as Transistor-Transistor logic or TTL gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates.

OBSERVATIONS

LED ON (Red light) : Logic 1
LED OFF (No light) : Logic 0
Input Variables : A, B
Output Variable : Y

S.NO.	INPUT (A)	INPUT (B)	$Y = A + B$ (OR)	$Y = A \cdot B$ (AND)	$Y = \overline{AB}$ (NAND)	$Y = \overline{A+B}$ (NOR)	$Y = A \oplus B$ (XOR)	$Y = A \odot B$ (XNOR)
1.	0	0	0	0	1	1	0	1
2.	0	1	1	0	1	0	1	0
3.	1	0	1	0	1	0	1	0
4.	1	1	1	1	0	0	0	1

➤ AND Gate

A multi-input circuit in which the output is 1 only if all inputs are 1. The symbolic representation of the AND gate is as shown.
The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B.

➤ OR Gate

A multi-input circuit in which the output is 1 when any input is 1. The symbolic representation of the OR gate is as shown.
The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.

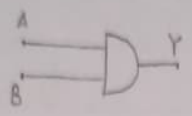
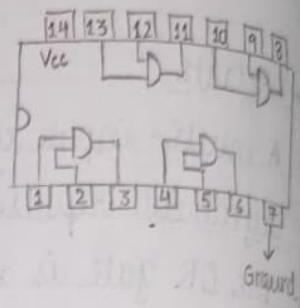
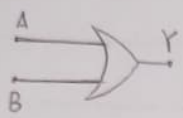
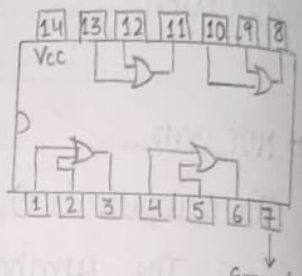
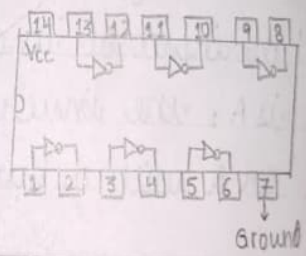
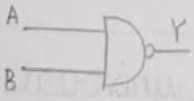
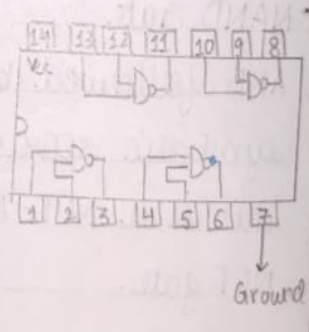
➤ NOT Gate

The output is 0 when the input is 1, and the output is 1 when the input is 0. The symbolic representation of an inverter is as shown.
The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as inverter. If the input variable is A, the inverted output is known as NOT A. This is also known as A', or A with a bar over the top, as shown at the outputs.

➤ NAND Gate

AND followed by INVERT. It is also known as universal gate. The symbolic representation of the NAND gate is as shown.
This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate.

SUMMARY OF LOGIC GATES

GATE	LOGIC DIAGRAM	FUNCTION	TRUTH TABLE	IC DIAGRAM
AND (IC 74C08)		Y = A AND B Y = A·B Y = AB	A B | Y 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1	
OR (IC 74C32)		Y = A OR B Y = A + B	A B | Y 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1	
NOT (IC 74C04)		Y = NOT A Y = $\overline{A}$	A | Y 0 | 1 1 | 0	
NAND (IC 74C00)		Y = A NOT AND B Y = A NAND B Y = $\overline{A \cdot B}$ Y = $\overline{AB}$	A B | Y 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0	

▶ NOR Gate

OR followed by inverter. It is also known as universal gate. The symbolic representation is as shown.
This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

▶ EXOR Gate

The output of the Exclusive-OR gate, is 0 when its two inputs are the same and its output is 1 when its two inputs are different. It is also known as Anti-coincidence gate.
The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both, of its two inputs are high. An encircled plus (⊕) is used to show the EXOR operation.

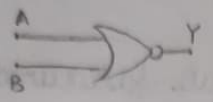
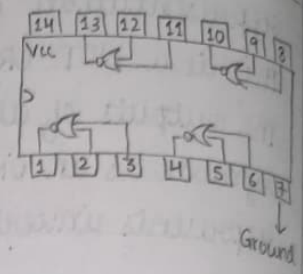
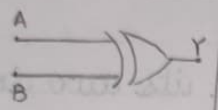
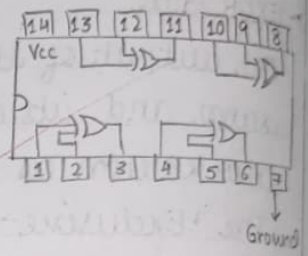
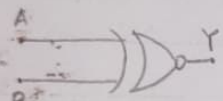
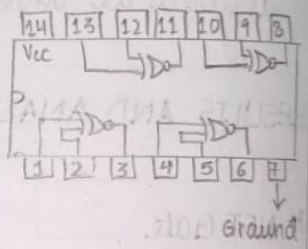
RESULTS AND ANALYSIS

▶ NOT Gate

When logic 1 is applied to one of NOT gate of 7404 IC, then output becomes zero. When input LED is ON (RED), the output LED becomes OFF (Green) and vice versa.

▶ OR Gate

The output of an OR gate is a 1 if one or the other or both the inputs are 1, but a 0 if both inputs are 0. When one or the other or both the input LEDs are ON (Red) then the output LED is ON (Red) otherwise the output LED is OFF (Green).

GATE	LOGIC DIAGRAM	FUNCTION	TRUTH TABLE	IC DIAGRAM
NOR (IC 74C02)		Y = A NOT OR B Y = A NOR B $Y = \overline{A+B}$	A B Y 0 0 1 0 1 0 1 0 0 1 1 0	
EX-OR (IC 74C86)		Y = A X-OR B $Y = A \oplus B$ $Y = A\overline{B} + \overline{A}B$	A B Y 0 0 0 0 1 1 1 0 1 1 1 0	
EX-NOR (IC 74C266)		$Y = \overline{A \text{ XOR } B}$ Y = A XNOR B $Y = A \odot B$ $Y = \overline{A}\,\overline{B} + AB$	A B Y 0 0 1 0 1 0 1 0 0 1 1 1	

▶ AND Gate

The output of an AND gate is only 1 if both the inputs are 1. For all the other possible inputs the output is 0. When both the LEDs are ON, then the output LED is ON (Red), otherwise it is OFF (Green).

▶ NOR Gate

The output of the NOR gate is a 1 if both inputs are 0 but a 0 if one or the other or both inputs are 1.

▶ NAND Gate

The output of the NAND gate is a 0 if both inputs are 1 but a 1 if one or the other or both inputs are 0.

▶ EXOR Gate

The output of the XOR gate is a 1 if either but not both inputs are 1 and a 0 if the inputs are either 0 or both 1

■ CONCLUSION

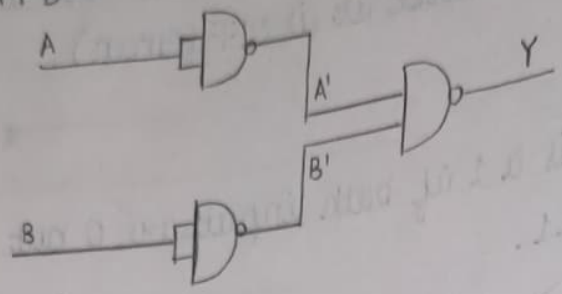
Any Boolean expression can be realised using NOT, AND, OR, NAND, NOR, EXOR gates.

13/08/19

DESIGN OF GATES USING N

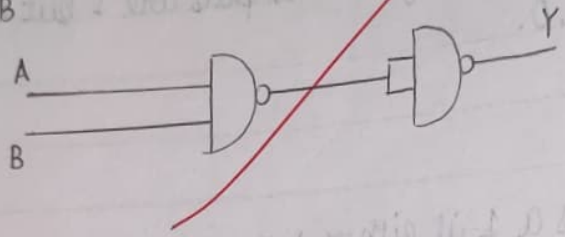
(i) OR GATE

$Y = A + B$



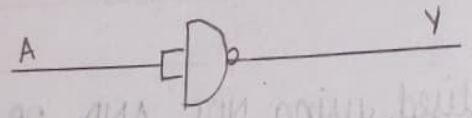
(ii) AND GATE

$Y = A \cdot B$



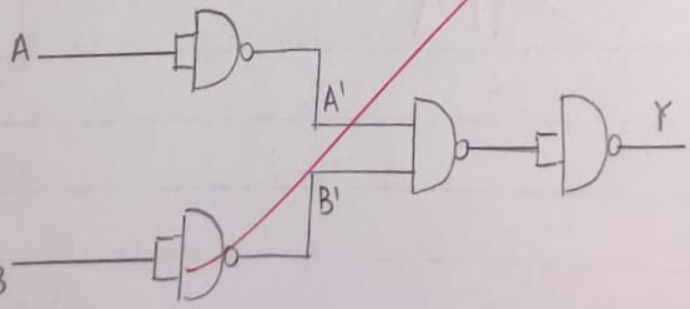
(iii) NOT GATE

$Y = A'$



(iv) NOR GATE

$Y = (A+B)'$



EXPERIMENT NO·2

AIM

To design AND, OR, NOT, XOR, XNOR, NAND, NOR gates using Universal Gates.

APPARATUS REQUIRED

IC (No·7400 and 7402), connecting wires, breadboard, LED

THEORY

It is possible to design all the logic gates using NAND and NOR gates. Hence, these two gates are called Universal Gates.

Using NAND Gate

(i) OR Gate

OR Gate can be designed using 3 NAND gates. For OR gate with A and B as inputs and Y as the output then

$$Y = A + B$$

$$Y = ((A+B)')'$$

Using Demorgan's Law,

$$Y = (A'.B')'$$

$$Y = (A \text{ NAND } A) \text{ NAND } (B \text{ NAND } B)$$

(ii) AND Gate

AND gate can be designed using 2 NAND gates.

Here,

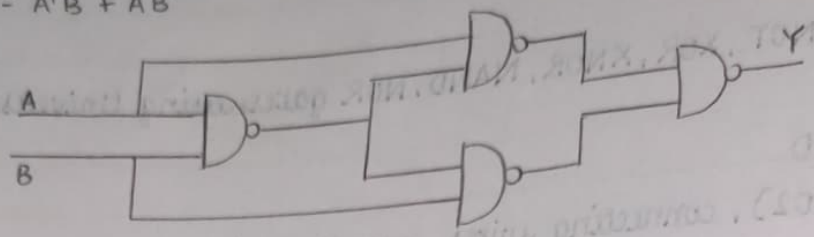
$$Y = AB$$

$$Y = ((AB)')'$$

$$Y = (A \text{ NAND } B) \text{ NAND } (A \text{ NAND } B)$$

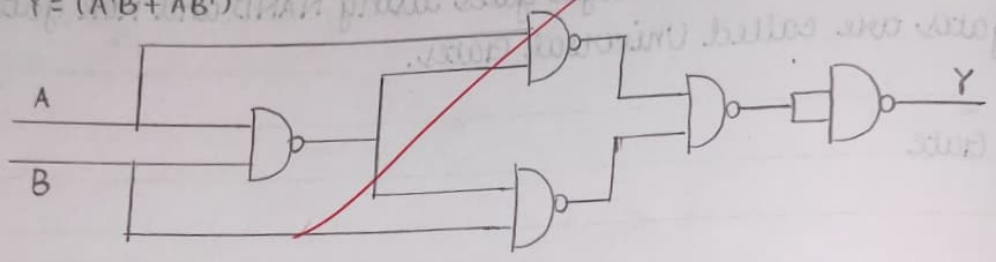
(v) XOR GATE

$Y = A'B + AB'$



(vi) XNOR GATE

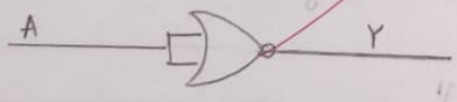
$Y = (A'B + AB')'$



DESIGN OF GATES USING NOR GATES

(i) NOT GATE

$Y = A'$



(iii) NOT Gate

NOT gate can be designed using only 1 NAND gate. For a NOT gate,

$$Y = A'$$

$$Y = ((A)')' = (A \cdot A)'$$

$$Y = A \text{ NAND } A$$

(iv) NOR Gate

NOR gate can be designed using 4 NAND gates. For NOR gate,

$$Y = A + B$$

$$Y = [(A \text{ NAND } A) \text{ NAND } (B \text{ NAND } B)] \text{ NAND } [(A \text{ NAND } A) \text{ NAND } (B \text{ NAND } B)]$$

(v) XOR Gate

XOR gate can be designed using 4 NAND gates. For XOR gates,

$$Y = A'B + AB'$$

$$Y = [(A \text{ NAND } (A \text{ NAND } B)) \text{ NAND } (B \text{ NAND } (A \text{ NAND } B))]$$

(vi) XNOR Gate

XNOR gate can be designed using 5 NAND gates. Here for an XNOR gate,

$$Y = [(A \text{ NAND } (A \text{ NAND } B)) \text{ NAND } (B \text{ NAND } (A \text{ NAND } B))] \text{ NAND } [(A \text{ NAND } (A \text{ NAND } B)) \text{ NAND } (B \text{ NAND } (A \text{ NAND } B))]$$

➤ Using NOR Gate

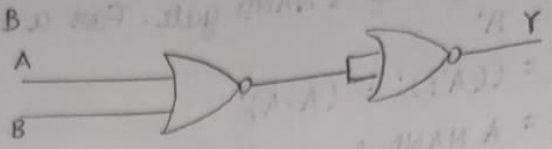
(i) OR Gate

OR gate can be designed using 2 NOR gates. Here,

$$Y = (A \text{ NOR } B) \text{ NOR } (A \text{ NOR } B)$$

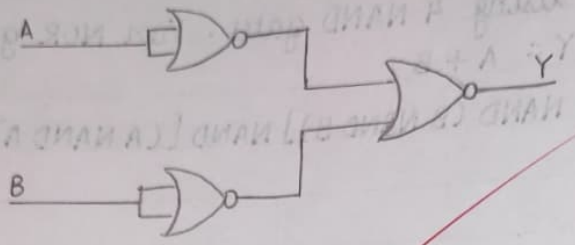
(ii) OR GATE

$Y = A + B$



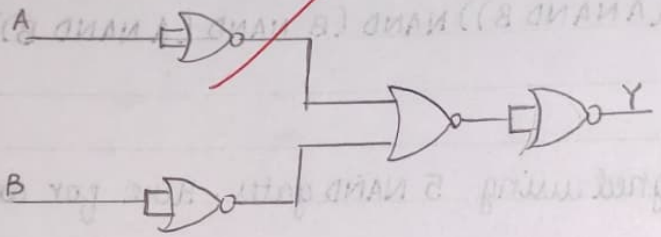
(iii) AND GATE

$Y = A \cdot B$



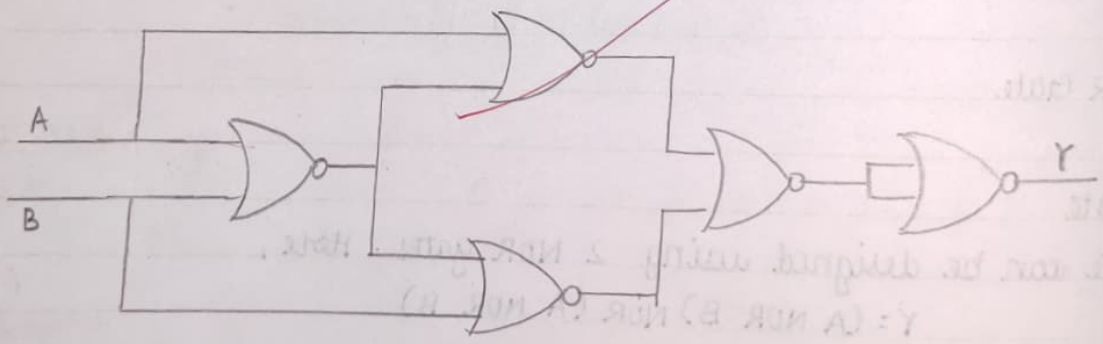
(iv) NAND GATE

$Y = (AB)'$



(v) XOR GATE

$Y = A'B + AB'$



(ii) AND Gate

AND gate can be designed using 3 NOR gates. Here, we have,

Y = (A NOR A) NOR (A NOR B)

(iii) NOT Gate

NOT Gate can be designed using just one NOR gate. Here,

Y = A NOR A

(iv) NAND Gate

NAND Gate can be designed using 4 NOR gates. Here we have,

Y = [(A NOR A) NOR (B NOR B)] NOR [(A NOR A) NOR (B NOR B)]

(v) XOR Gate

XOR gate can be designed using 5 NOR gates. Here we have,

Y = [(A NOR (A NOR B)) NOR (B NOR (A NOR B))] NOR
[(A NOR (A NOR B)) NOR (B NOR (A NOR B))]

(vi) XNOR Gate

XNOR gate can be designed using 4 NOR gates. Here, we have,

Y = [(A NOR (A NOR B)) NOR (B NOR (A NOR B))]

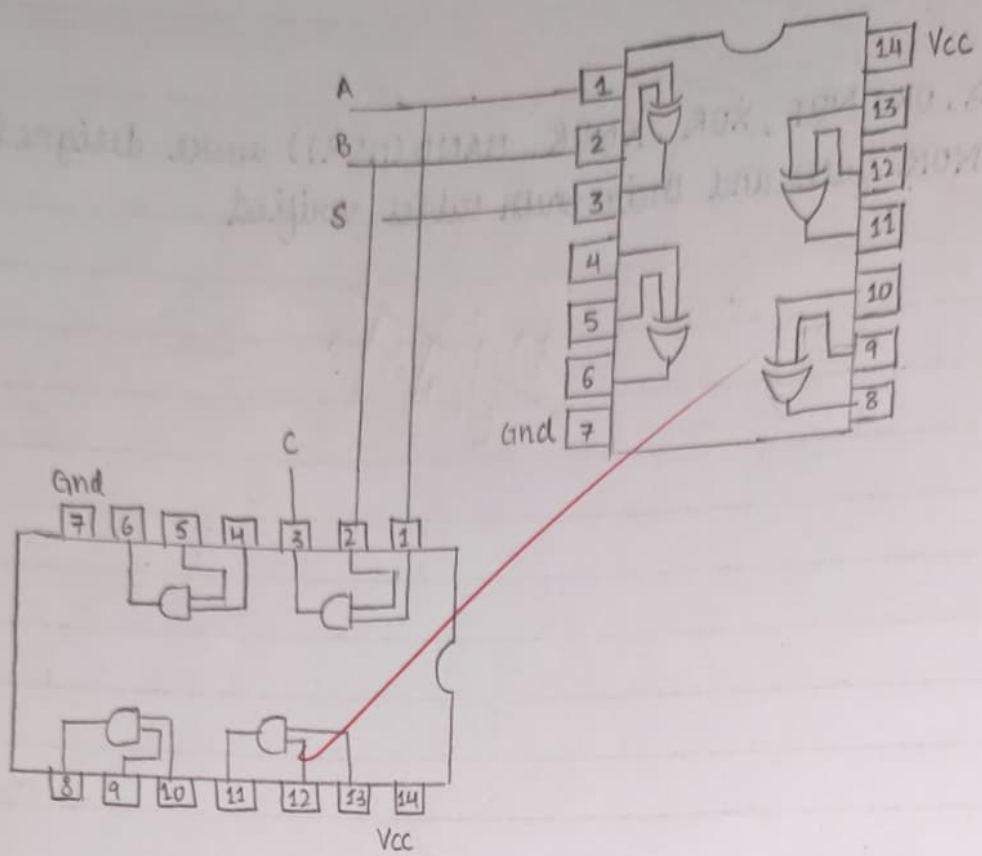
PROCEDURE

- For designing the required gate from NAND or NOR gates, connect the reqd. IC.
- Connect the gate in the required manner with the help of connecting wires and make proper connections for ground (pin 7) and supply (pin 14).
- Connect the inputs and outputs to the required LED. Switch on the supply.
- Note the output for various combinations of input, note the observations and compare them with the observations of original gate.
- Repeat the above steps for all the gates and note the observations.

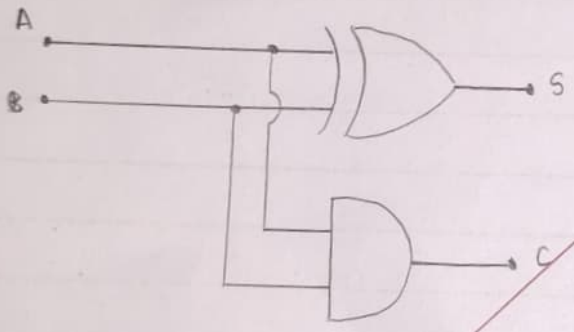
RESULT

All the gates (AND, OR, NOT, XOR, XNOR, NAND (NOR)) were designed using NAND and NOR gates and their truth tables verified

27/08/19



PIN DIAGRAM OF HALF ADDER



CIRCUIT DIAGRAM OF HALF-ADDER

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

TRUTH - TABLE

EXPERIMENT NO. 3(i)

AIM

Design and verify the logic circuit of Half Adder using logic gates.

APPARATUS REQUIRED

Breadboard, DC Power Supply 5V Battery, Light Emitting Diode (LED), Digital ICs (7408, 7486, 7432), connecting wires

THEORY

A Half-Adder is a logical circuit that performs an addition operation on two binary digits. The half-adder produces a sum and a carry value which are both binary digits.

BOOLEAN EXPRESSION: $S = A \oplus B$

$C = AB$

PROCEDURE

- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips. PIN 7 = Ground and PIN 14 = +15V.
- According to the pin diagram of each IC mentioned above, make the connections according to circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn on the power switch of breadboard.
- Operate the switches and fill in the truth table (1 for ON and 0 for OFF). Apply the various combinations of inputs acc. to the truth table and observe the condition of output LEDs.

OBSERVATION TABLE

Input Variables : A, B

Output Variables : S, C

LED ON : Red light (1)

LED OFF : No Light (0)

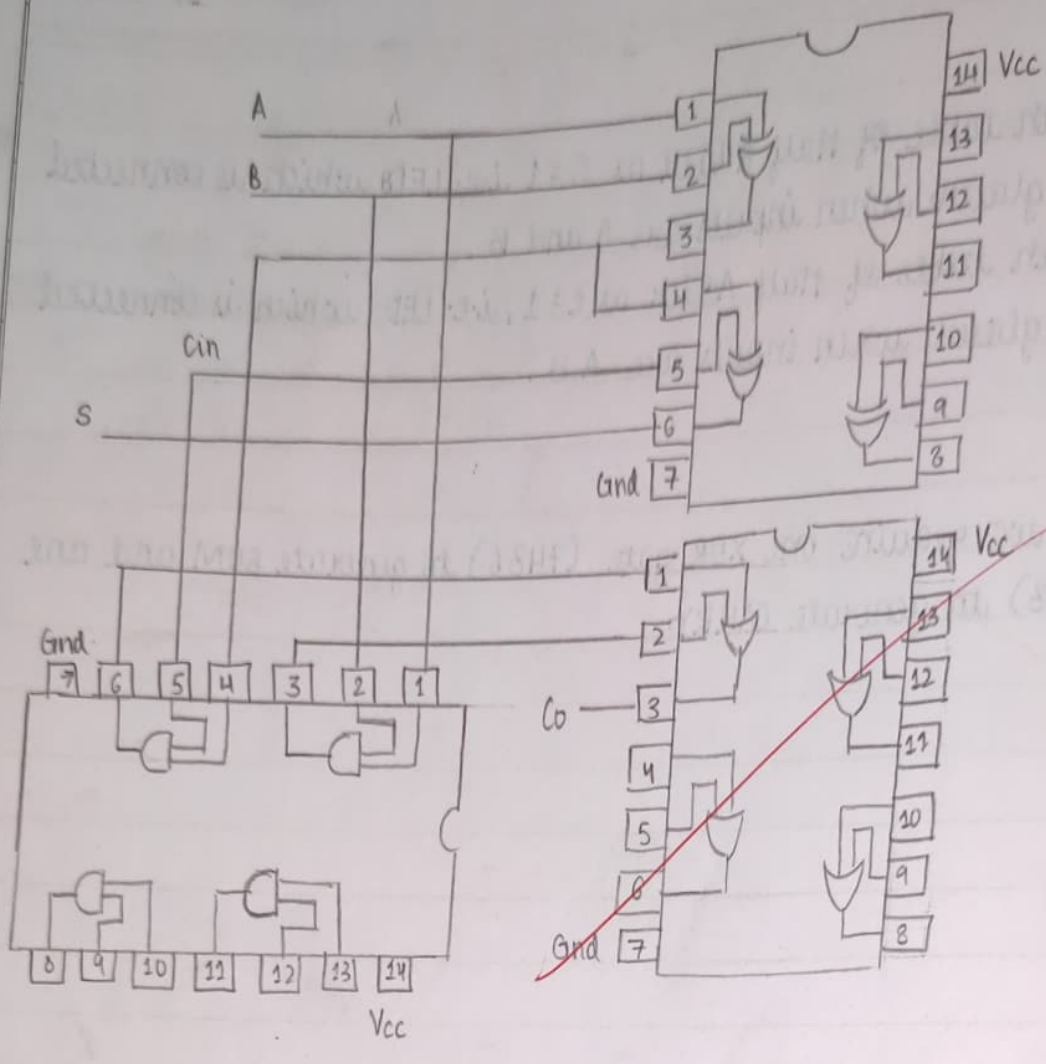
INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

RESULT

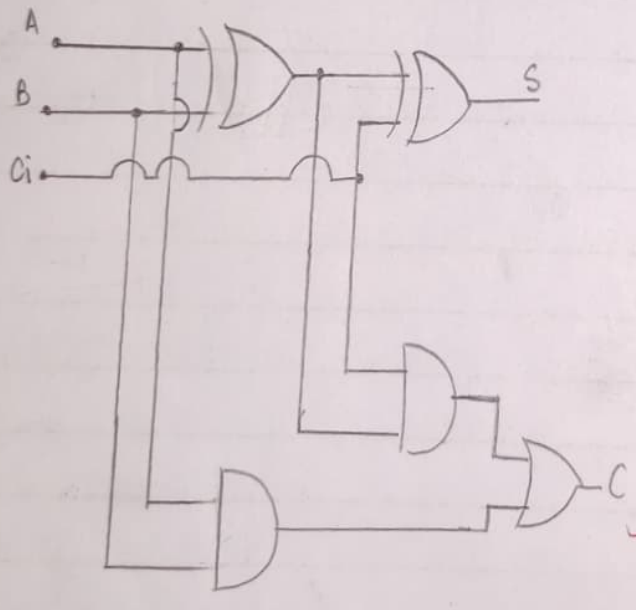
Verified the truth table of Half Adder as S=1 i.e. LED which is connected to S terminal glows when inputs are A and B.
Verified the truth table of Half Adder as C=1, i.e. LED which is connected to C terminal glows when inputs are A B.

CONCLUSION

To add two bits we require one XOR gate (7486) to generate SUM and one AND gate (7408) to generate CARRY.



PIN DIAGRAM FOR FULL ADDER



CIRCUIT DIAGRAM FOR FULL-ADDER

INPUT			OUTPUT	
A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TRUTH TABLE

EXPERIMENT NO. 3(ii)

AIM

Design and verify the logic circuit Full Adder using a Half Adder.

APPARATUS REQUIRED

Breadboard, DC Power Supply 5V Battery, light Emitting Diode (LED), Digital ICs (7408, 7486, 7432), connecting wires.

THEORY

Full adder is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, which are both binary digits. It can be combined with other full adders or work on its own.

BOOLEAN EXPRESSION: $S = A \oplus B \oplus C_i$

$C_o = AB + C_i(A \oplus B)$

PROCEDURE

- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips. PIN 7 = Ground and PIN 14 = +5V.
- According to the pin diagram of each IC mentioned above, make the connections according to the circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all the connections have been done, turn on the power switch of breadb.
- Operate the switches and fill in truth table (1 for LED ON and 0 for LED OFF)

OBSERVATIONS

Input Variables : A, B, Ci

Output Variables : S, Co (sum and carry)

LED ON : RED light (1)

LED OFF : NO light (0)

INPUT			OUTPUT	
A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

RESULT

Verified the truth table of Full Adder as S=1, i.e. LED which is connected to S terminal glows when inputs are A, B, Ci.
Verified the truth table of Full Adder as Co=1, i.e. LED which is connected to Co terminal glows when inputs are A, B, Co.

CONCLUSION:

To add three bits we require two half adders.

Megha 03/07/19

TRUTH TABLE

INPUTS		OUTPUTS	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-MAP

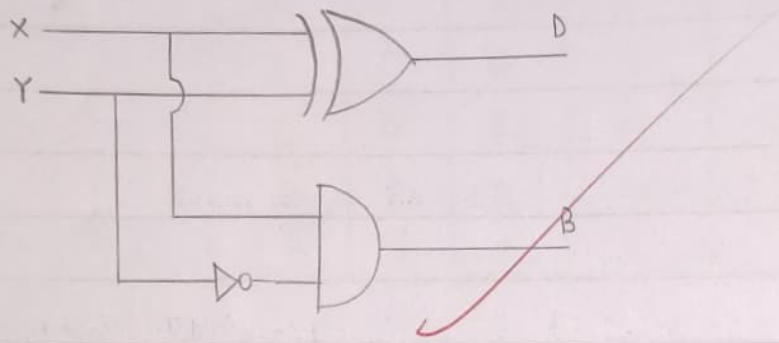
X \ Y	0	1
0		1
1	1	

$D = A \oplus B$

X \ Y	0	1
0		1
1		

$B = \bar{A}B$

CIRCUIT DIAGRAM



EXPERIMENT NO. 04.(i)

AIM

Design and verify the logic circuit of a half subtractor using logic gates.

APPARATUS REQUIRED

Breadboard, DC Power supply 5V battery, Light Emitting Diode (LEDs), Digital ICs (7404, 7486, 7408), connecting wires.

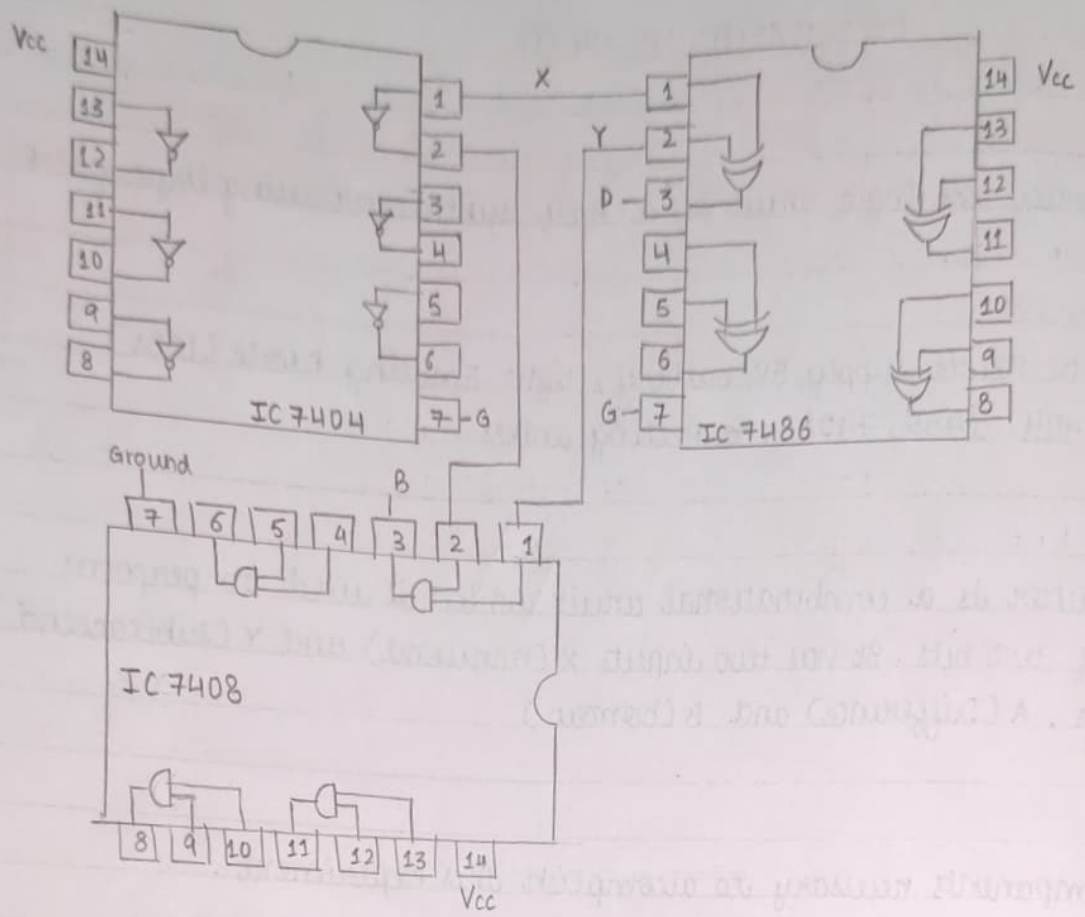
THEORY

A half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs X (minuend) and Y (subtractend) and 2 outputs, A (Difference) and B (borrow)

PROCEDURE

- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips. PIN 7 → Ground and PIN 14 → 5V.
- According to the pin diagram of each IC mentioned above. Make the connections according to circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn on the power switch of the breadboard.
- Operate the switches and fill in the truth table.

PIN DIAGRAM



OBSERVATION TABLE

Input Variables : X, Y

Output Variables : D, B

LED ON : Red light (1)

LED OFF : No light (0)

INPUT		OUTPUT	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

RESULT AND ANALYSIS

Verified the truth table of half subtractor as D=1, i.e. LED which is connected to D terminal glows when inputs are x, y. Verified the truth table of half subtractor as B=1, i.e. LED which is connected to B terminal glows when inputs are x and y.

CONCLUSION

- To add two bits we require one EXOR gate (7486) to generate difference and one AND (7408) and NOT gate (7432) to generate Borrow.
- To add three bits, we require full subtractor.

TRUTH TABLE

A	B	Bor in	D	Bor out
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-MAP

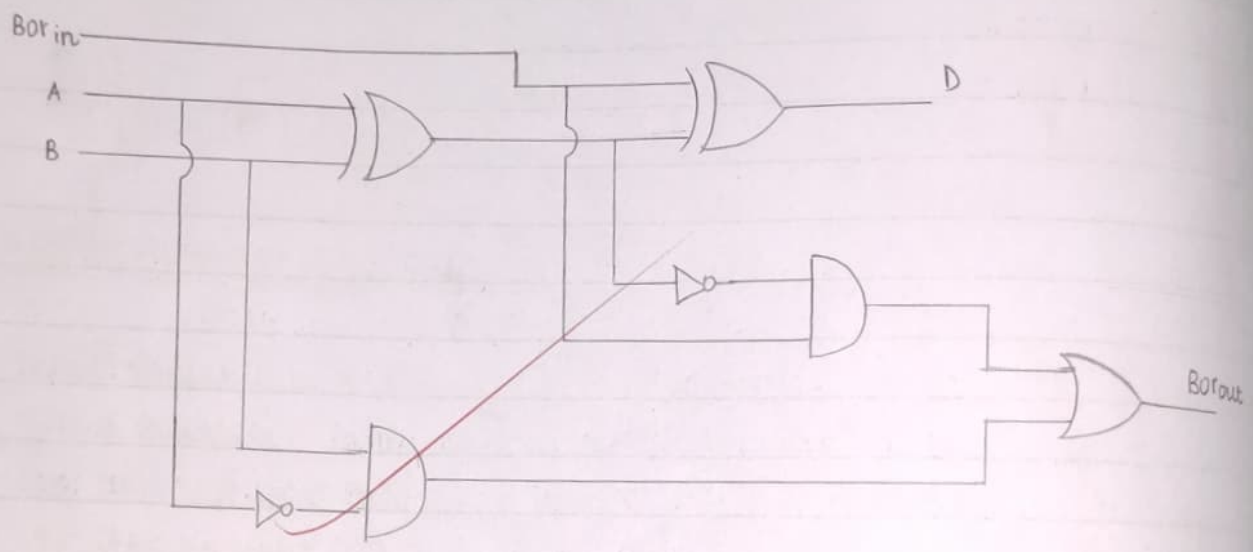
A \ B Borin	00	01	11	10
0		1		1
1	1		1	

$D = A \oplus B \oplus Bor\,in$

A \ B Borin	00	01	11	10
0		1	1	1
1			1	

$B = \bar{A}B + \bar{A}Bor\,in + BBor\,in$

CIRCUIT DIAGRAM



EXPERIMENT NO. 4(ii)

AIM

Design and verify the logic circuit of full subtractor using half subtractor.

APPARATUS REQUIRED

Breadboard, DC Power Supply 5V battery, Light Emitting Diodes (LEDs), Digital ICs (7408, 7486, 7432, 7404), connecting wires.

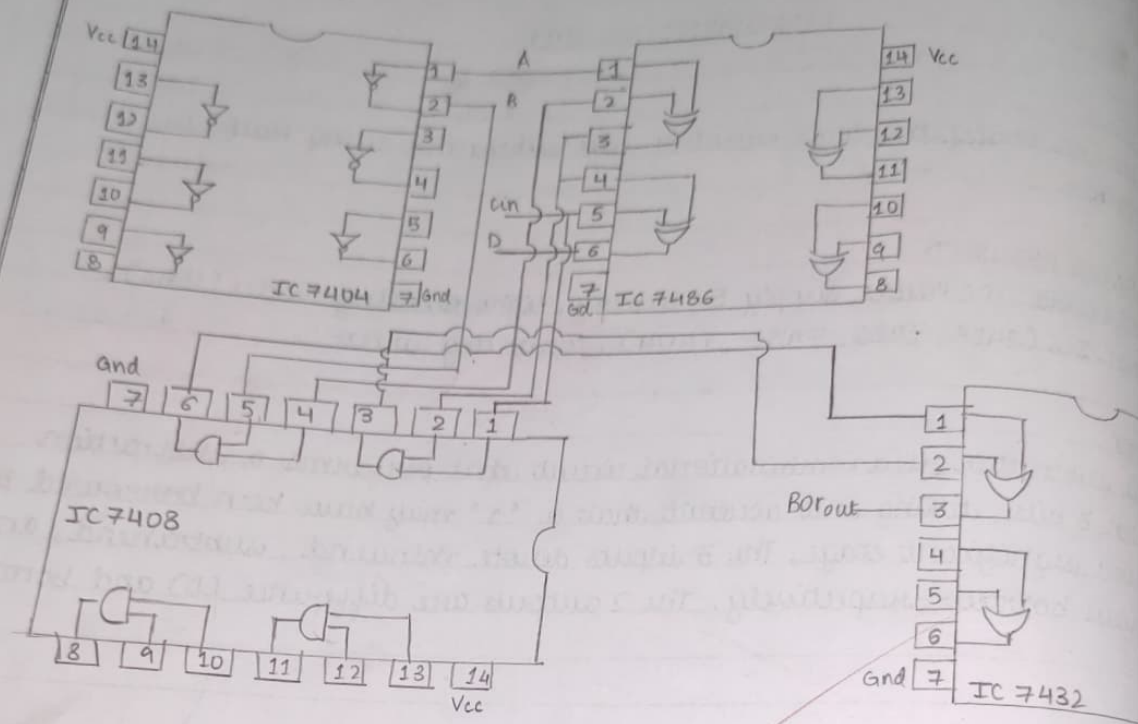
THEORY

A full subtractor is a combinational circuit that performs a subtraction between 3 bits, taking into account that a '1' may have been borrowed by a lower significant stage. The 3 inputs denote minuend, subtrahend, and previous borrow, respectively. The 2 outputs are difference (D) and borrow (B).

PROCEDURE

- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the Breadboard.
- Connect the supply voltage and ground lines to the chips.
- According to the pin diagram of each IC mentioned here above. Make the connections according to circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn on the power switch of breadboard.
- Operate the switches and fill in the truth table.

PIN- DIAGRAM



OBSERVATION TABLE

Input Variables: A, B, Borin

Output Variables: D, Borout

LED ON: Red light (1)

LED OFF: No light (0)

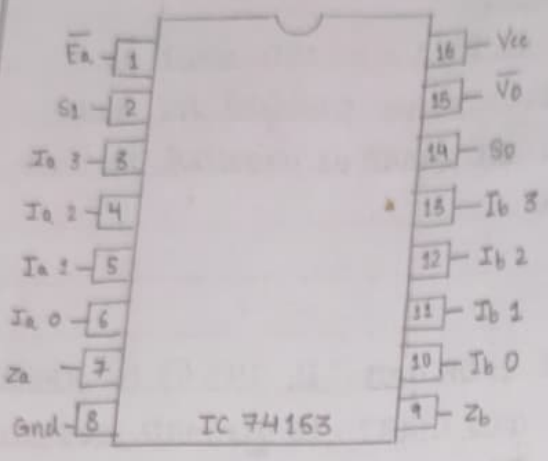
A	B	Borin	D	Borout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

RESULT AND ANALYSIS

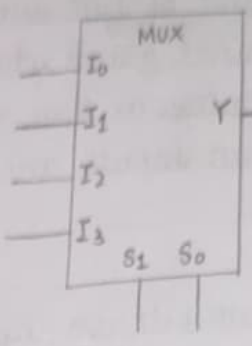
Verified the truth table of full subtractor as D = 1 i.e., LED which is connected to D terminal glows when inputs X, Y, Bin. Verified the truth table of full subtractor as Bout = 1, i.e. LED which is connected to Bout terminal glows when inputs are X, Y, Bin.

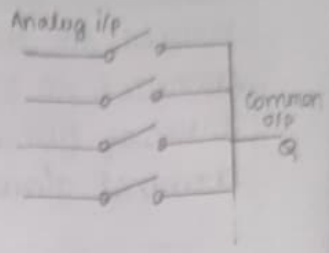
CONCLUSION

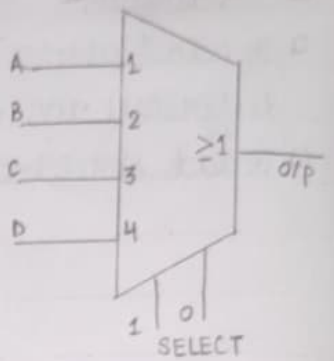
- To add (subtract) two bits we require one EXOR gate (IC 7486) to generate difference and one AND (7408) and NOT gate (7432) to generate borrow.
- To add three bits, we require ha full subtractor.



PIN DIAGRAM OF DUAL 4:1 MUX



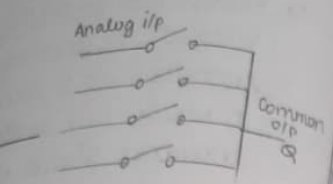


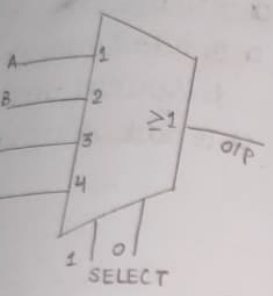


E	SELECT LINES		Zo OUTPUT
	S0	S1	
0	0	0	(I0) 1
0	0	1	(I1) 0
0	1	0	(I2) 1
0	1	1	(I3) 0
1	X	X	0

[Zo was given]

TRUTH TABLE OF 4:1 MUX (IC 74153) [CHANNEL A] WITH O/P ON LOW MODE





EXPERIMENT NO. 5(i)

AIM

(a) To verify the truth table of 4:1 multiplexer using IC 74153.
(b) To verify the truth table of 1:4 demultiplexer using IC 74139

APPARATUS REQUIRED

Breadboard, DC Power Supply 5V battery, Light Emitting Diode, Digital ICs: 74153 dual 4:1 MUX and 74139 dual 1:4 DEMUX, wires

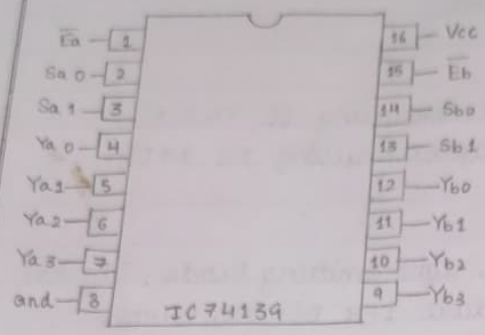
THEORY

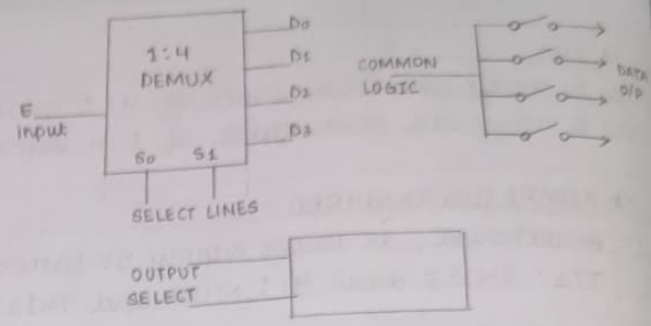
▸ Multiplexer

A data selector, more commonly called a multiplexer, shortened to "MUX" or "MPX" is a combinational logic switching device that operates like a very fast-acting multiple rotary switch. It connects or controls multiple input lines called "channels" consisting of either 2, 4, 8 or 16 individual inputs, on at a time, to an output. Then job of a MUX is to allow multiple signals to share a signal comm output. For example, a single 8 channel MUX would connect one o its 8 inputs to the single data output.

▸ Demultiplexer

The data distributer, known more commonly as a demultiplexer or "DEMUX", is the exact opposite of multiplexer. The DEMUX ta single input data line and then switches it to any one of a no individual output lines one at a time. The MUX converts a seri signal at the input to a parallel data at its output lines.

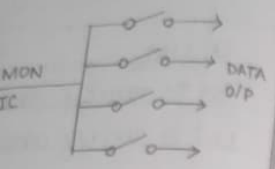




PIN DIAGRAM OF DUAL 1:4 DEMUX

E	INPUT		OUTPUT			
	S_0	S_1	D_0	D_1	D_2	D_3
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

TRUTH TABLE OF 1:4 DEMUX (IC 74139) WITH ACTIVE LOW E MODE



The Boolean expression for this 1-to-4 DEMUX above with the inputs outputs D0 to D3 and data select line S0 to S1 is given as

$$E = S_0S_1D_0 + S_0S_1D_1 + S_0S_1D_2 + S_0S_1D_3$$

The function of the DEMUX is to switch one common data input line to any of the 4 output data lines. Some standard DEMUX IC's also have an "enable output" input pin which disables or prevents the input from being passed to the selected output. Also some have latches built into their outputs to maintain the output logic level after the address inputs will determine which single data output will have the same value as the data input with all other data outputs having the value of logic '0'.

PROCEDURE

- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips:
- Make the connections as shown in the respective circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output of the ~~led~~ LED.
- Once all the connections have been done, turn on the power switch of the breadboard.
- Operate the switches and fill in the truth table.

RESULT AND DISCUSSIONS

Multiplexer and Demultiplexer help in reducing the cost of transmissio of digital signals. Logic Design is simple and boolean expression nee not be simplified. MUX and DEMUX act as rotary switches. Multi

-plexers are used as one method of reducing the no. of logic gates required in a circuit or when a single data line is required to carry two or more different digital signals i.e. it converts parallel data into serial data and is also used for data selection. The demultiplexer converts a serial data signal at the input to a parallel data at its output lines and is used for data distribution. Both are available as ICs.

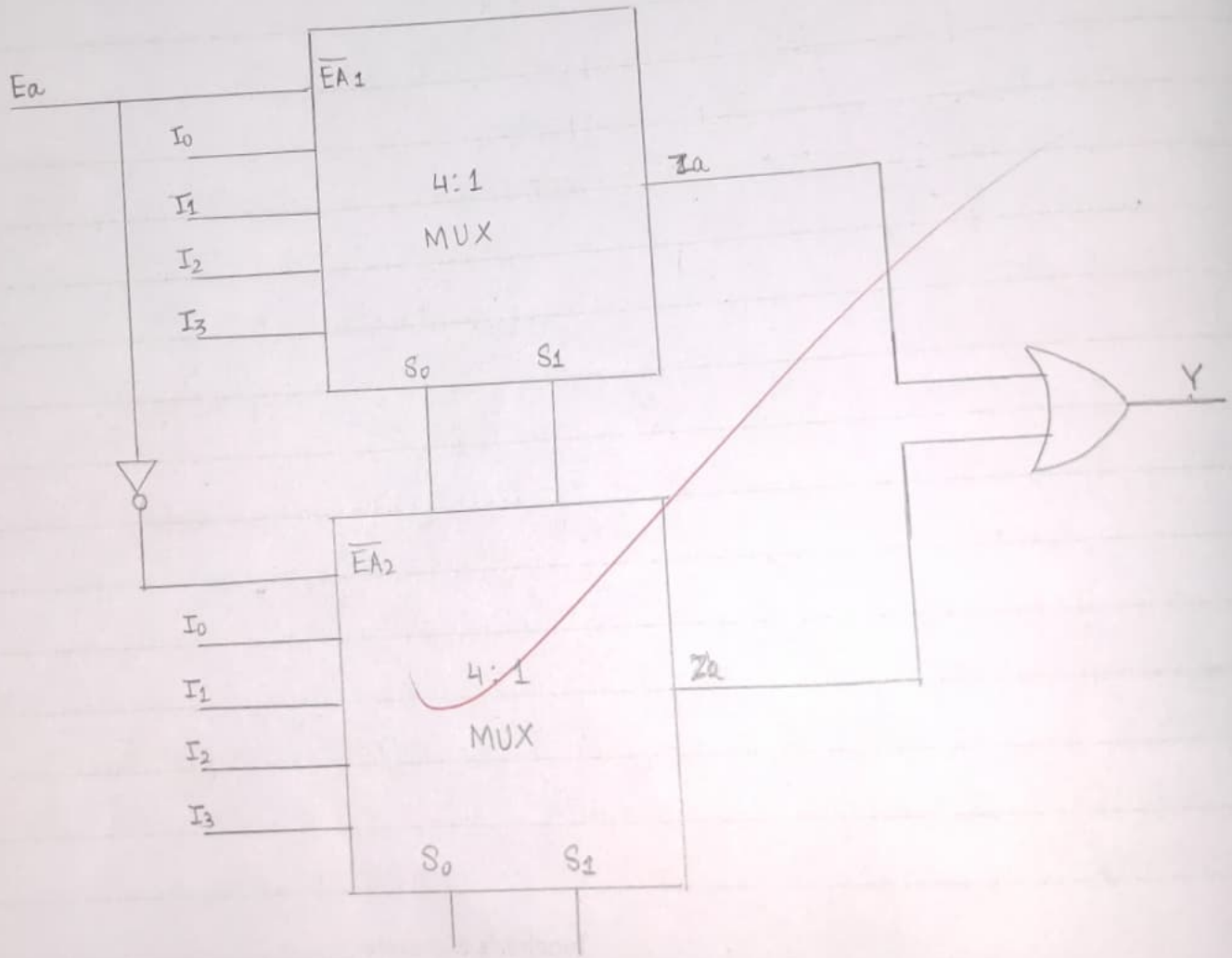
CONCLUSION

The Truth Tables of 4:1 MUX using IC 74153 and 1:4 DEMUX using IC 74139 have been verified.

TRUTH TABLE

SELECT LINES			OUTPUTS		
E_0	S_1	S_0	Z_a	Z_b	Y
0	0	0	1	0	1
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	1	1
1	1	1	0	1	1

CIRCUIT DIAGRAM



EXPERIMENT NO. 5(ii)

AIM

To design the 8:1 MUX using two 4:1 MUX using f(0,2,6,7).

APPARATUS REQUIRED

Breadboard, DC Power supply, Light Emitting Diode, digital ICs 74153 (Dual 4:1 MUX), 7432 (OR), 7404 (Hex Inverter), connecting wires.

THEORY

MULTIPLEXER

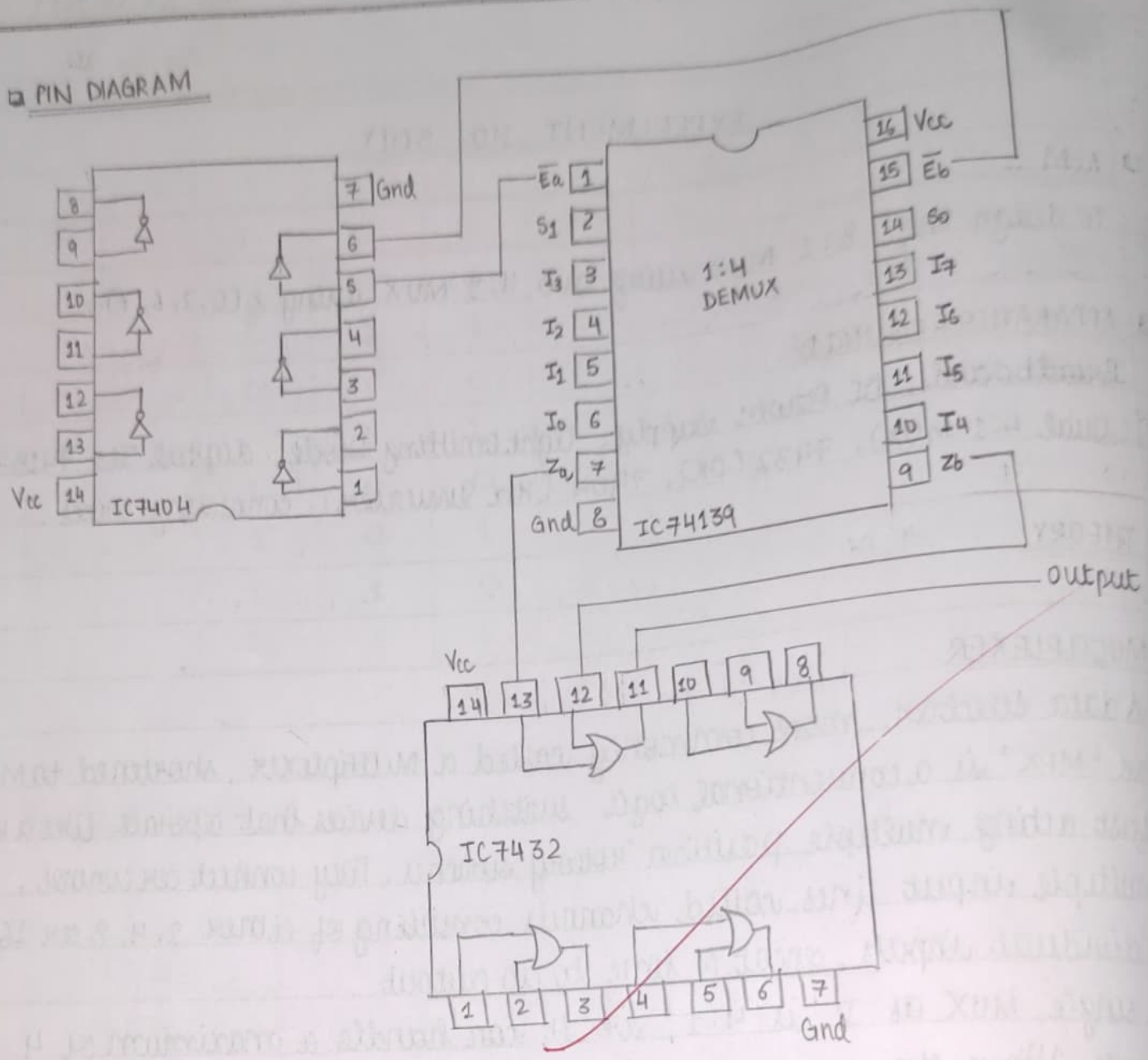
A data selector, more commonly called a Multiplexer, shortened to MUX or 'MPX' is a conventional logic switching devices that operate like a very fast acting multiple position rotary switches. They connect or control, multiple input lines called channels consisting of either 2, 4, 8 or 16 individual inputs, one at a time to an output.

A single MUX as IC is 4:1, i.e. it can handle a maximum of 4 inputs. When the no. of inputs is more than 4, a multiplexer tree can be used that is also known as multiplexer stack.

PROCEDURE

- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and Ground lines to the chips.
- Make connections as shown.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn ON the powerswitch of breadbo

PIN DIAGRAM


Gnd
Vcc
IC7404
Ea
S1
I3
I2
I1
I0
Z0
Gnd
1:4
DEMUX
IC74139
Vcc
Eb
S0
I7
I6
I5
I4
Z6
output
Vcc
IC7432
Gnd

- Operate the switches and fill in the truth table.

RESULT

Multiplexers help in reducing the cost of transmission of signals. Logic design is simple and boolean expression need not be simplified. MUX acts as a rotary switch. Multiplexers are used as one method of reducing the numbers of logic gates required in a circuit or when a single data line is required.

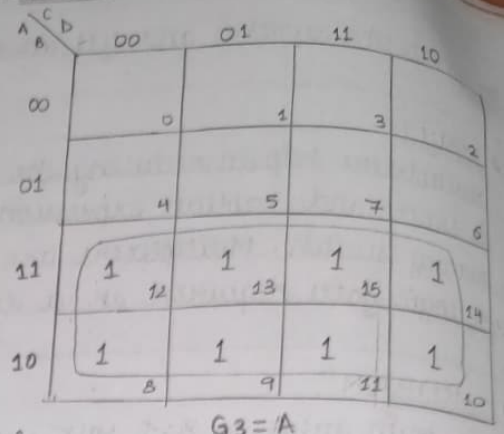
CONCLUSION

The truth table of 8:1 MUX using IC 74153 has been verified.

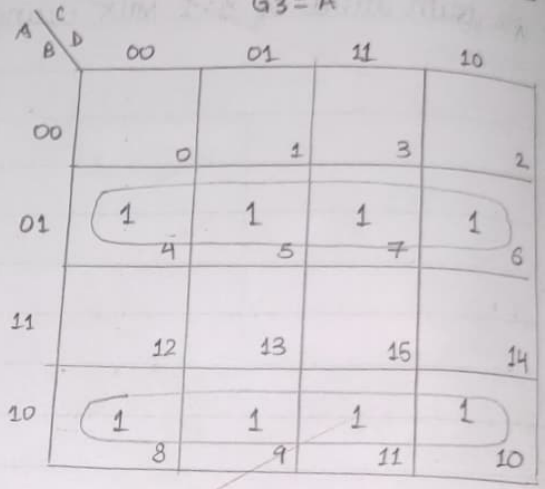
TRUTH TABLE

INPUTS				OUTPUTS			
A	B	C	D	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

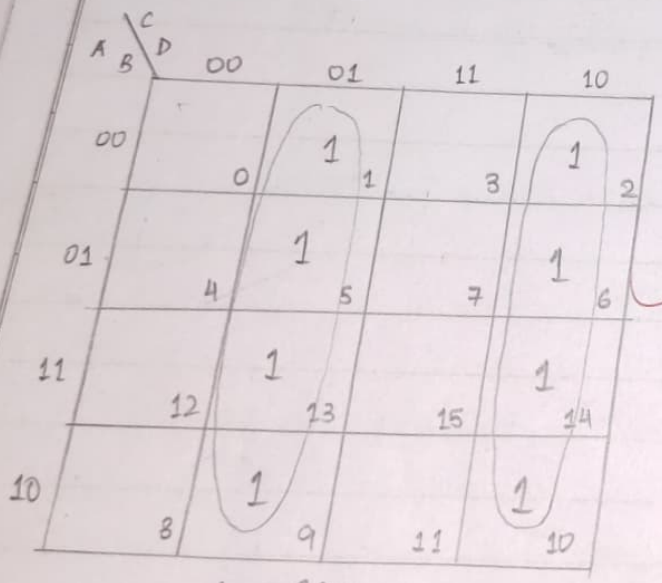
K-MAP



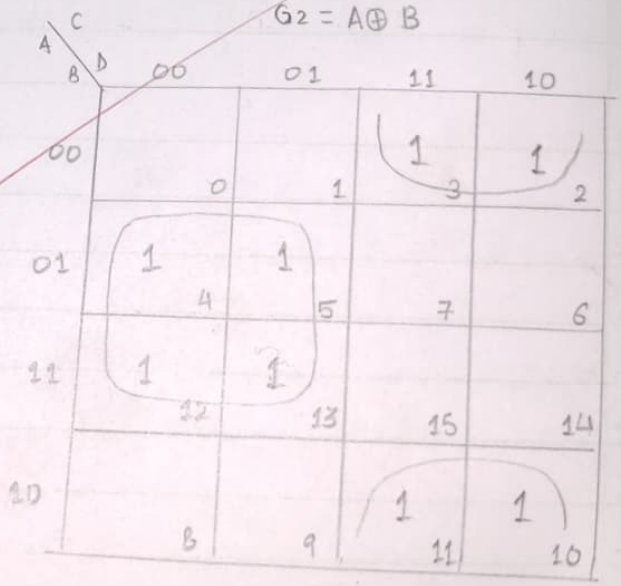
$G_3 = A$



$G_2 = A \oplus B$



$G_0 = C \oplus D$



$G_1 = B \oplus C$

EXPERIMENT NO. 6(i)

AIM

To design and verify the truth table of code conversion from binary to gray code conversion (4-bit) using basic logic gates.

OBJECTIVE

- Design a different combinational circuits and their applications using basic logic gates.
- Creation and observation of the four-bit Gray code number representation sequence
- Exercising the design of code conversion logic circuits.
- Creating the truth table of conversion functions from Binary to Gray Code.
- Developing skills in simplification of specified logical functions.

APPARATUS REQUIRED

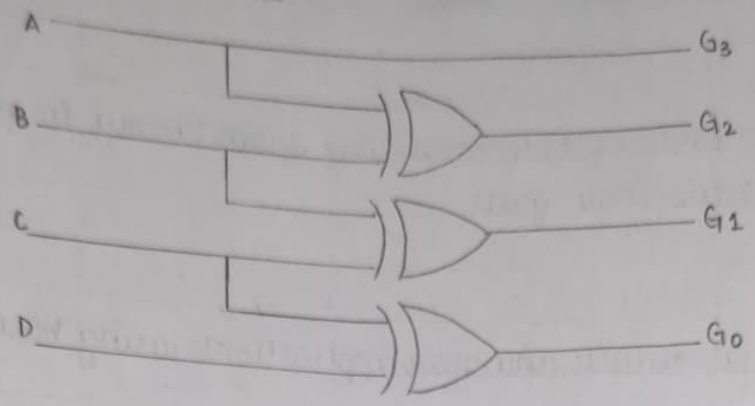
- Prototyping board (Breadboard), DC Power Supply (5v battery), Light Emitting Diode (LED), Digital ICs (7486), connecting wires.

THEORY

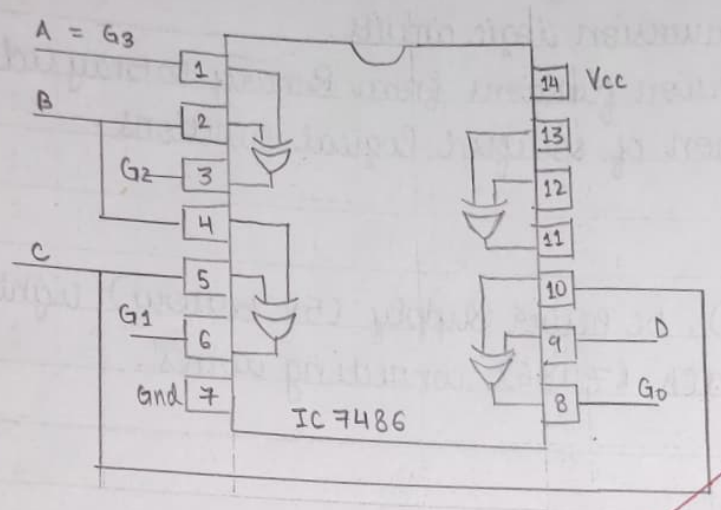
CODE CONVERTER

A code converter is a circuit that makes two digital systems using different codes for the same information. It means that a code conv is a code translator from one code to the other. The code converter used since two systems using two different codes but they need to u same information so the code converts is the solution.

CIRCUIT DIAGRAM



PIN-DIAGRAM



BINARY TO GRAY CONVERTER

An interesting application for the XOR gate is a logical circuit to change a binary no. to its equivalent in gray code. The logic circuit can be used to convert a 4-bit binary number ABCD into its gray code equivalent $G_1G_2G_3G_4$.

APPLICATION

Some sensors send information in Gray Code. These must be converted to binary in order to do arithmetic with it. Occasionally, it is necessary to convert back.

ADVANTAGES

Higher speed or smaller code.

RESULT AND DISCUSSION

The Binary to Gray Code converter is used since two systems using two diff. codes but they need to use the same information. Binary to Gray code converter converts correctly Binary 0000 to 1111 into Gray codes. The circuit diagram is very simple and only uses an 7486 IC i.e. XOR gate. Unless the K-Map is used many gates may be used. But result of K-Map minimalization it can work only using XOR gate. Gray code is a weighted, cyclic and reflective code are used in instrumentation and acquisition system where linear or angular displacement is measured, shaft encoder, I/O devices, A/D converter and other peripheral devices.

CONCLUSION

Binary to Gray code converter has been designed using XOR gate and its truth table is verified.

TRUTH TABLE

INPUTS				OUTPUTS			
A	B	C	D	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

K-MAP

A B \ C D	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	1 (12)	1 (13)	1 (15)	1 (14)
10	1 (8)	1 (9)	1 (11)	1 (10)

$B_3 = A$

A B \ C D	00	01	11	10
00	0	1	3	2
01	1 (4)	1 (5)	1 (7)	1 (6)
11	12	13	15	14
10	1 (8)	1 (9)	1 (11)	1 (10)

$B_2 = A \oplus B$

A B \ C D	00	01	11	10
00	0	1	1 (3)	1 (2)
01	1 (4)	1 (5)	7	6
11	12	13	1 (15)	1 (14)
10	1 (8)	1 (9)	11	10

$B_1 = A \oplus B \oplus C$

A B \ C D	00	01	11	10
00	0	1 (1)	3	1 (2)
01	1 (4)	5	1 (7)	6
11	12	1 (13)	15	1 (14)
10	1 (8)	9	1 (11)	10

$B_0 = A \oplus B \oplus C \oplus D$

EXPERIMENT NO. 6(ii)

AIM

To design and verify the truth table of code conversion from gray to binary code (4-bit) using basic logic gates.

OBJECTIVE

- Design of different combinational circuits and their applications using basic logic gates.
- Creation and observation of 4-bit binary code no. representation sequence.
- Exercising the design of code conversion logic circuits.
- Creating the truth table of conversion from gray to binary code.
- Developing skills in simplification of specified logical functions.

APPARATUS REQUIRED

Prototyping Board (Breadboard), DC Power Supply (5V battery), Light Emitting Diode (LEDs), digital ICs 7486, connecting wires.

THEORY

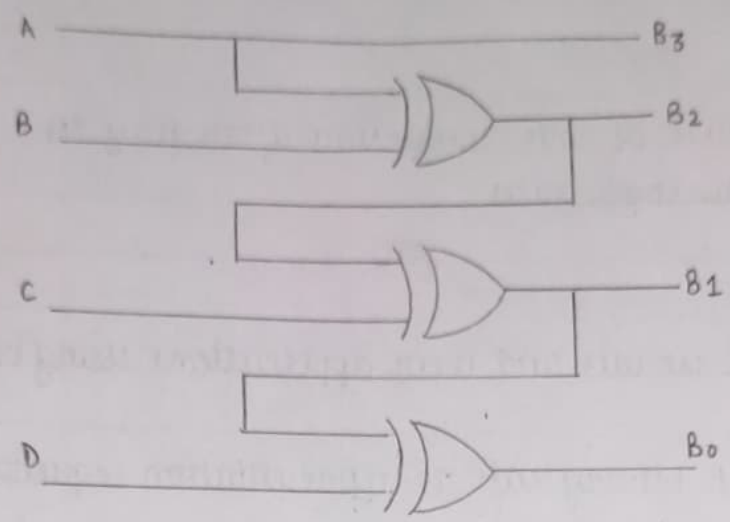
CODE CONVERTER

A code converter is a circuit that makes two digital systems using diff. codes for the same information. It means that a code converter is a code translator from one code to the other. The code converter is used since two systems using two different codes but they need to use the same info. So, the code converter is the solution.

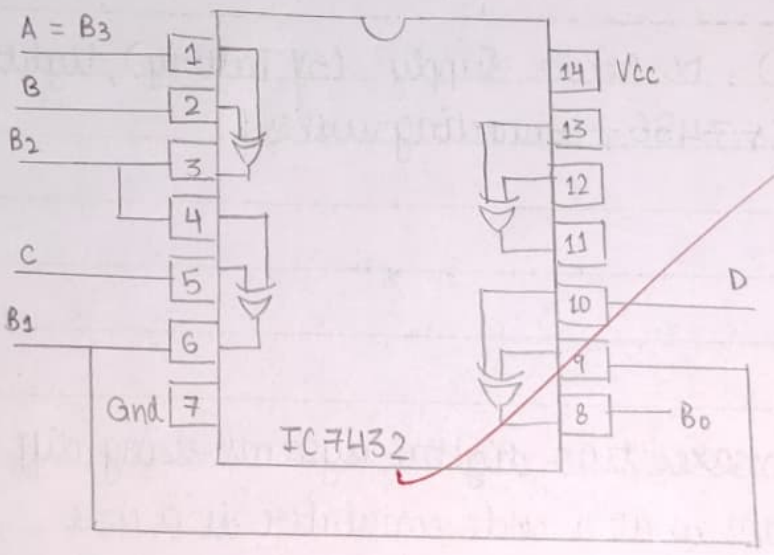
GRAY TO BINARY CODE CONVERTER

An interesting application for the XOR gate is a logical gate to convert a gray

CIRCUIT DIAGRAM



PIN DIAGRAM



code to its equivalent in binary code. The logic circuit can be used to convert a 4-bit gray no. ABCD to its Binary Code equivalent $B_3B_2B_1B_0$.

APPLICATION

Some sensors send information in Gray code. These must be converted to binary in order to do arithmetic with it. Occasionally its necessary to convert it back.

ADVANTAGES

Higher Speed or Smaller Code.

RESULT AND DISCUSSION

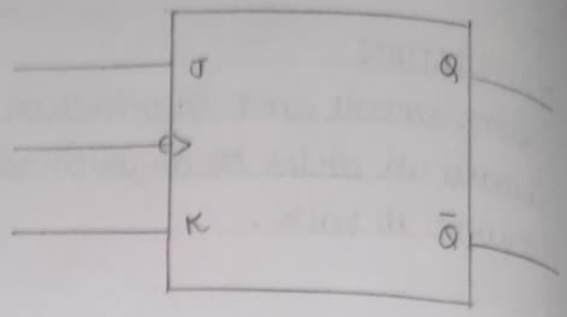
The Gray to Binary Code converter is used since two systems using two diff. codes but they need to use the same info. Gray to Binary code converter converts correctly gray 0000 to 1111 into Binary codes. The circuit diagram is very simple and only uses a 7486 IC (XOR gate). Unless the K-Map is used is used many gates may be used but result of K-Map minimization, it can work only using XOR gates. Gray code is a weighted, cyclic and reflexive code are used in instrumentation and acquisition system where linear or angular displacement is measured, shaft encoders, I/O devices, A/D converters and other peripheral devices.

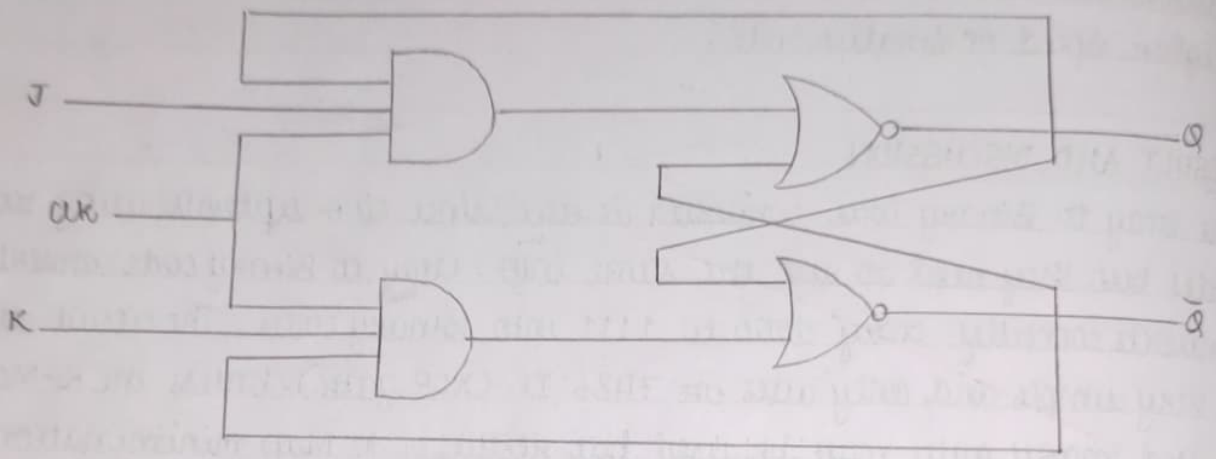
CONCLUSION

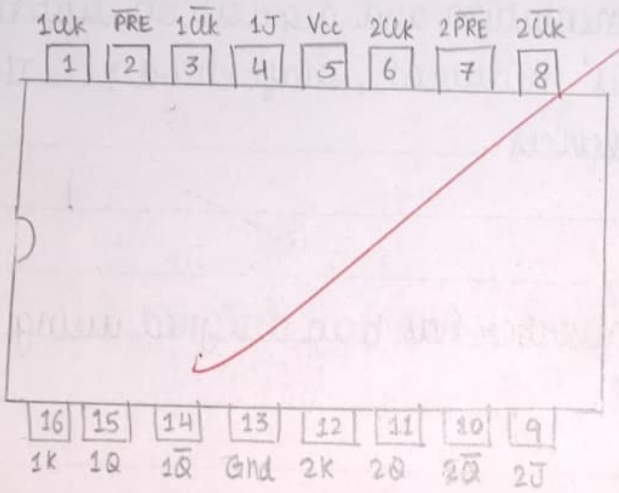
Gray to Binary code converter has been designed using XOR gates and its truth table is verified.

J-K FLIP FLOP

J	K	Qn+1
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$







EXPERIMENT NO. 7

AIM

To realize and implement JK and D flipflops using ICs and a breadboard.

APPARATUS REQUIRED

Breadboard, DC Power supply, Light Emitting Diode, Digital ICs 7476 and 7474, connecting wires.

THEORY

Logic circuits for digital circuits are either combinational or sequential. The output of combinational circuits depends only on the current inputs. In contrast, sequential circuits depends upon not only the current value of input but also upon the initial state of the circuit. Basic building blocks (memory elements) of a sequential circuit are the flipflops.

The flip-flops change their interval of time synchronized with some clock pulse applied to it. Usually any flip flop has normal inputs, present state (Q_t) as circuit inputs and two outputs, next state Q_{t+1} and its complementary value $Q:1$.

▶ JK Flip Flop.

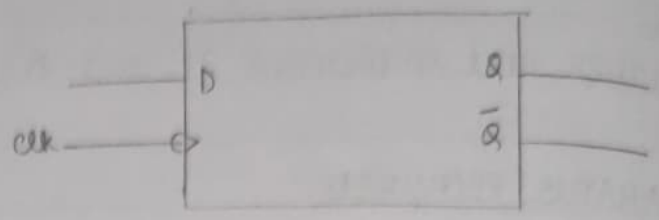
The JK Flip Flop is the modified version of SR flip-flop with no invalid states, that is, the state of JK = 1 is not forbidden, It works such that J serves as SET input and K serves as RESET. The only difference is that for all combinations J = K = 1. This flip-flop now performs an action - it inverts its state.

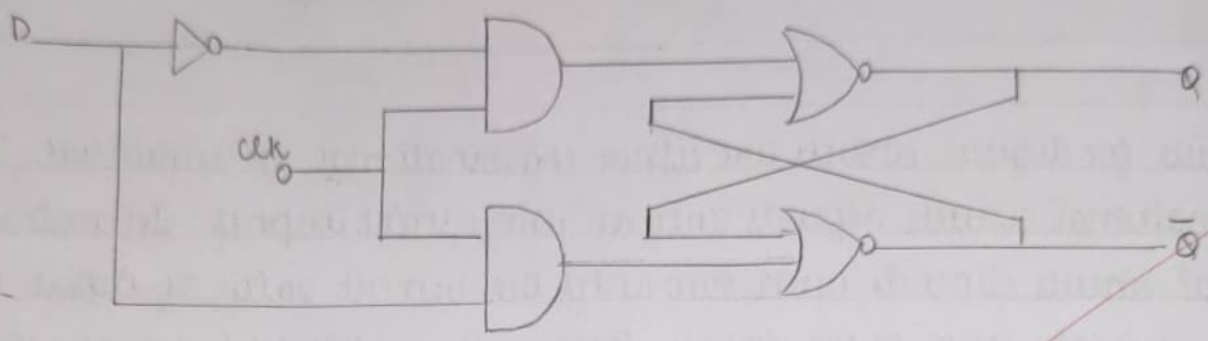
▶ D Flip Flop

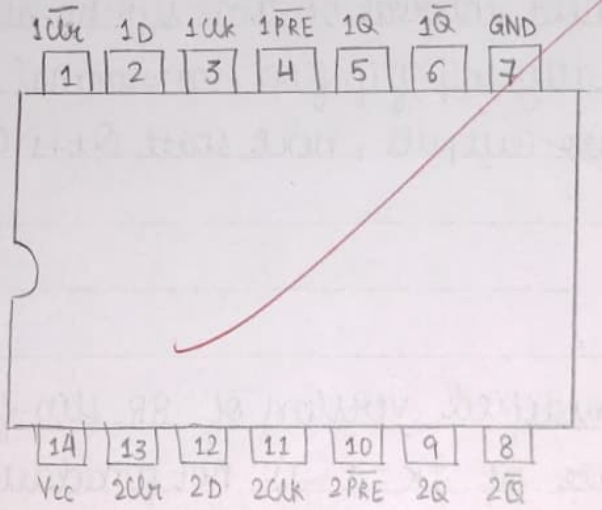
A D Flip Flop has a single data input. This input type of FF is obtained from

D FLIP-FLOP

D	Qn
0	0
1	1







the SR-FF by connecting the input through an inverter and the S input is connected directly to data input. The modified clocked SR FF is known as D Flip Flop.

PROCEDURE

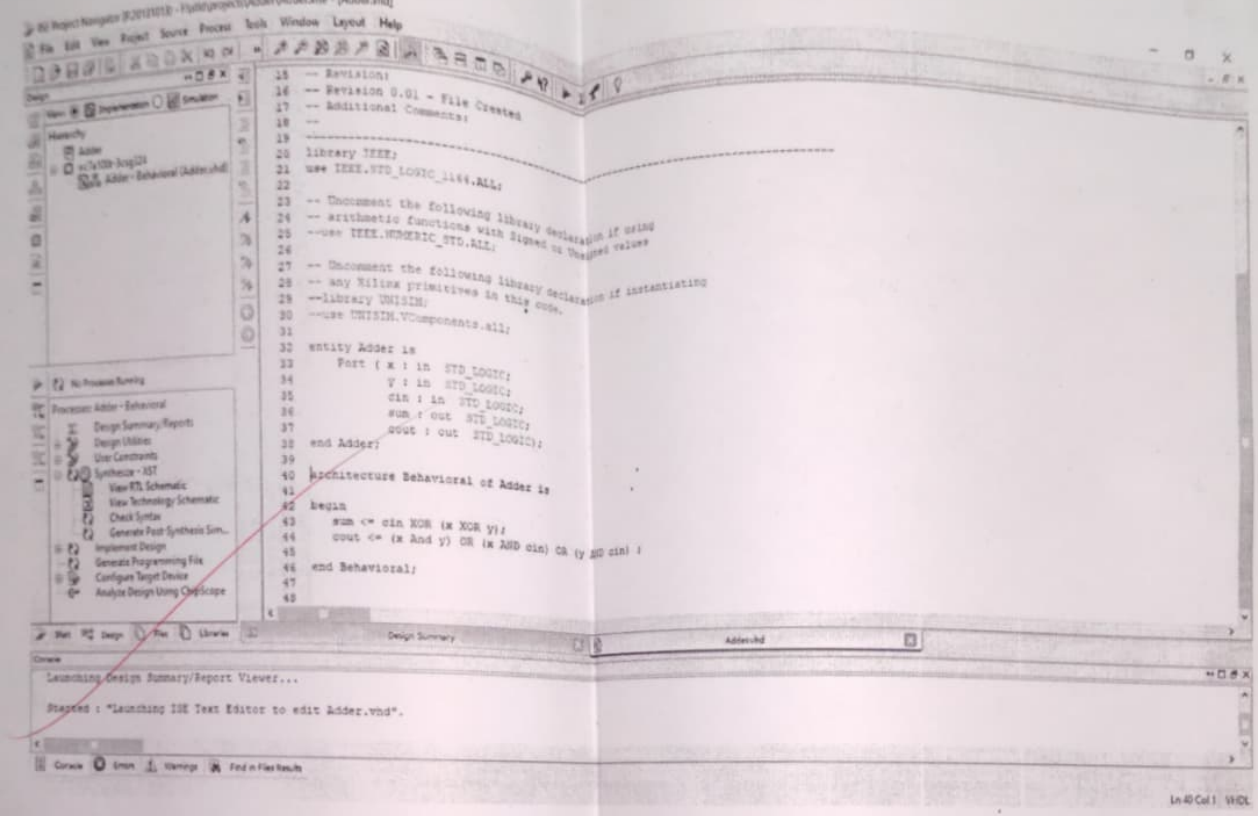
- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect all the wires according to the diagram.
- After all the connections have been made, switch ON the supply.

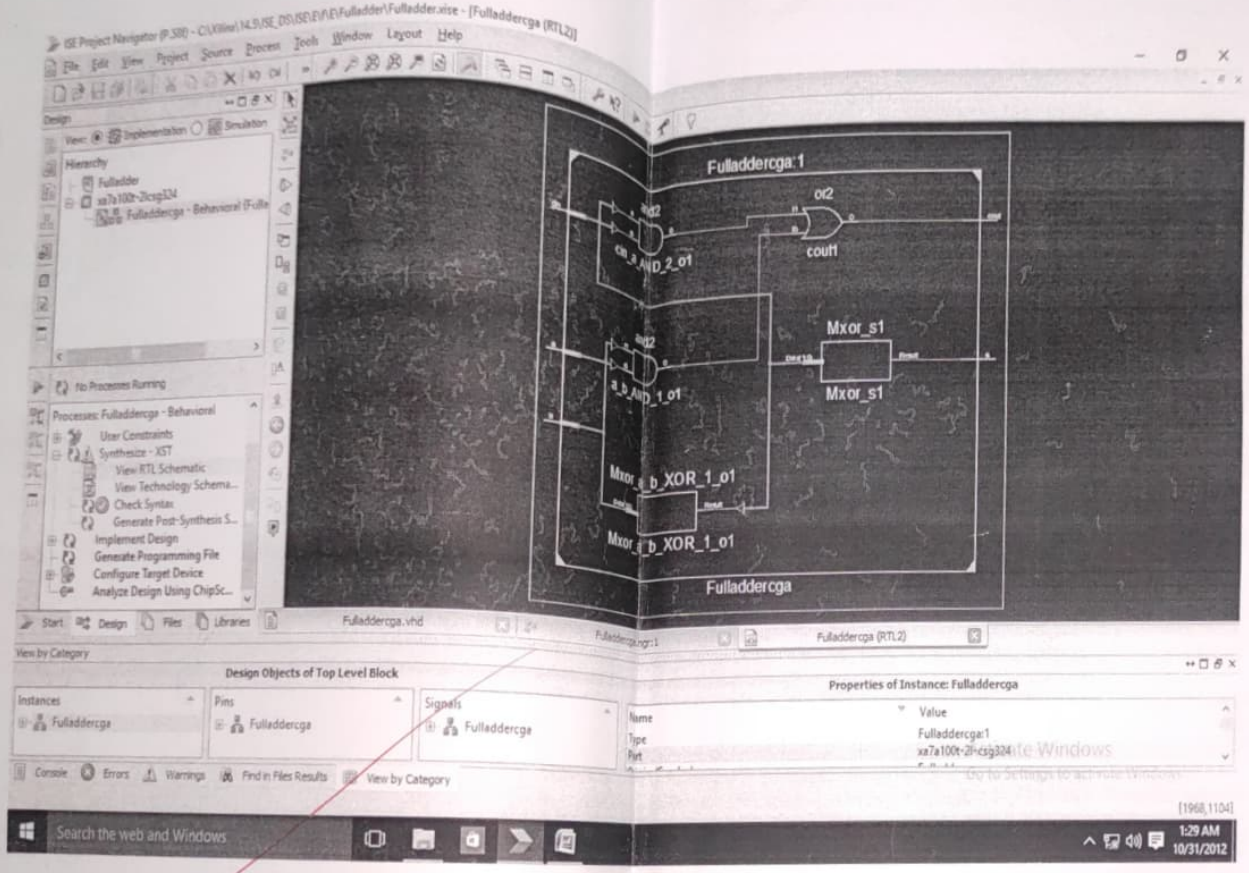
CONCLUSION

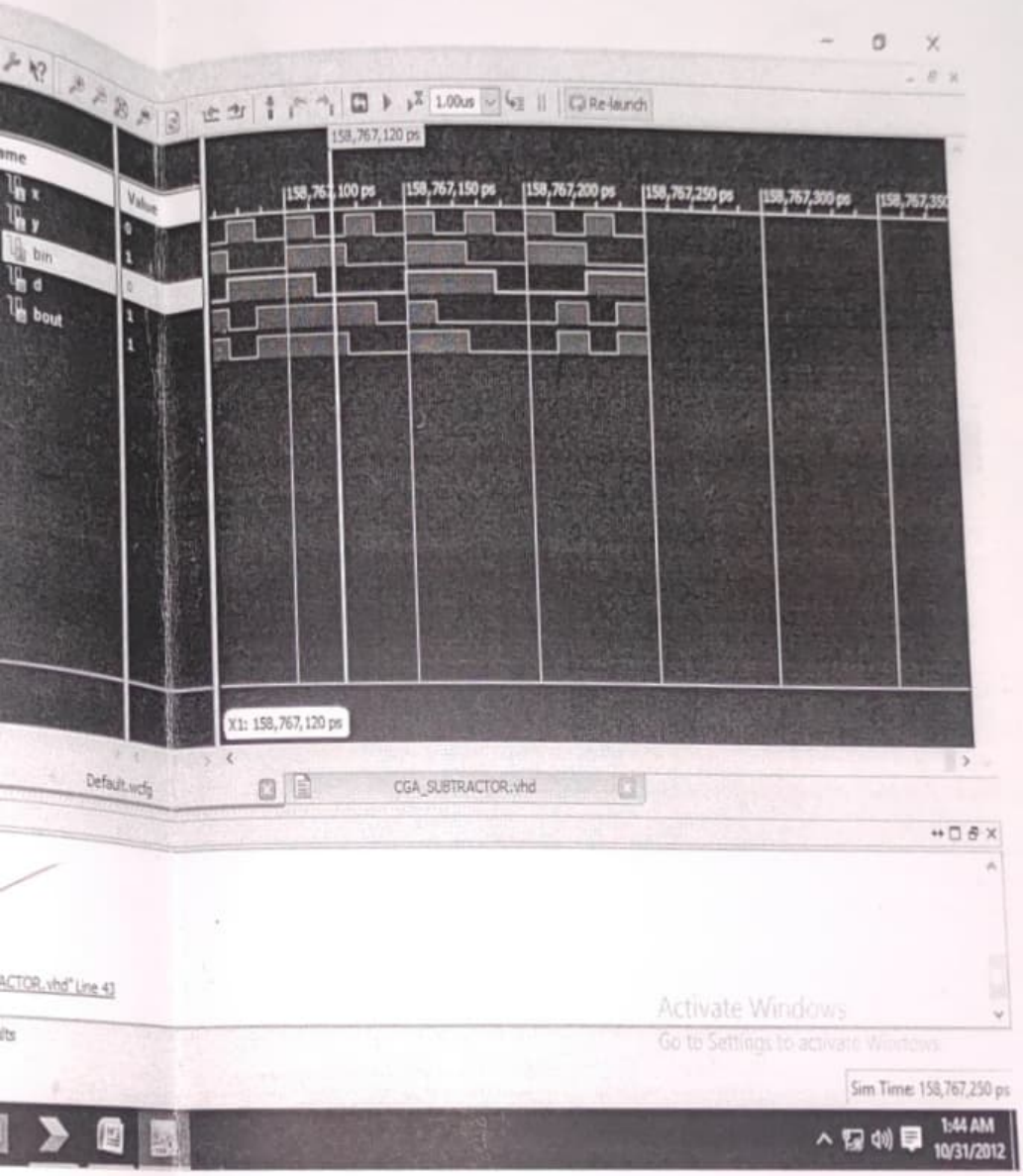
Basic memory elements are implemented and verified.

Experiment-8

To make a digital full adder using ISE.

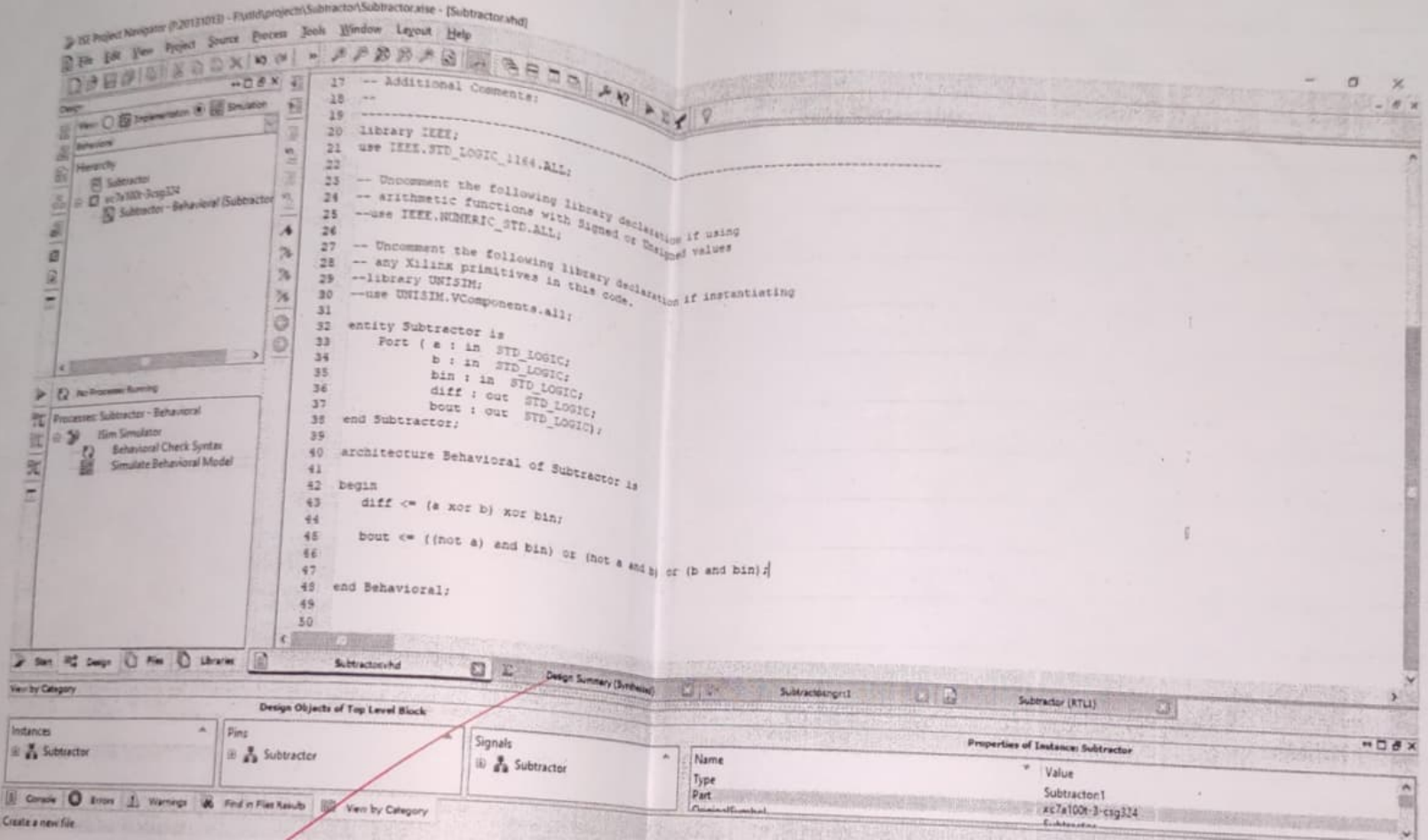



Fulladdercga:1
or2
coutl
Mxor_s1
Mxor_s1
Fulladdercga
Fulladdercga.vhd
Fulladdercga (RTL2)
Design Objects of Top Level Block
Properties of Instance: Fulladdercga
Name
Value
Type
Fulladdercga:1
Part
Console
Errors
Warnings
Find in Files Results
View by Category
Search the web and Windows
1:29 AM
10/31/2012


Re-launch
158,767,120 ps
158,767,100 ps
158,767,150 ps
158,767,200 ps
158,767,250 ps
158,767,300 ps
Value
x
y
bin
d
bout
X1: 158,767,120 ps
Default.wcfg
CGA_SUBTRACTOR.vhd
Activate Windows
Go to Settings to activate Windows.
Sim Time: 158,767,250 ps
1:44 AM
10/31/2012

Experiment 9

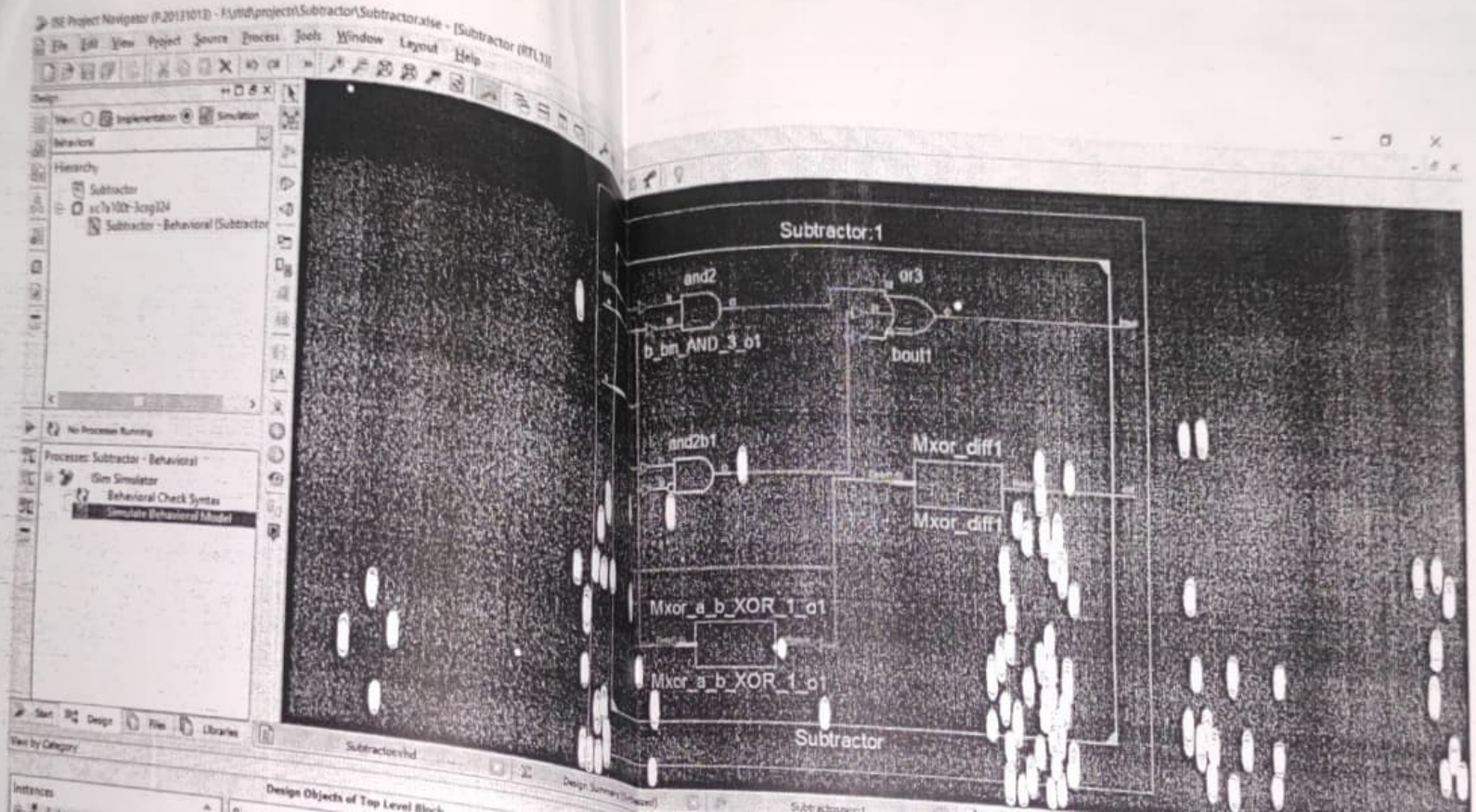
To make a digital full subtractor using ISE.

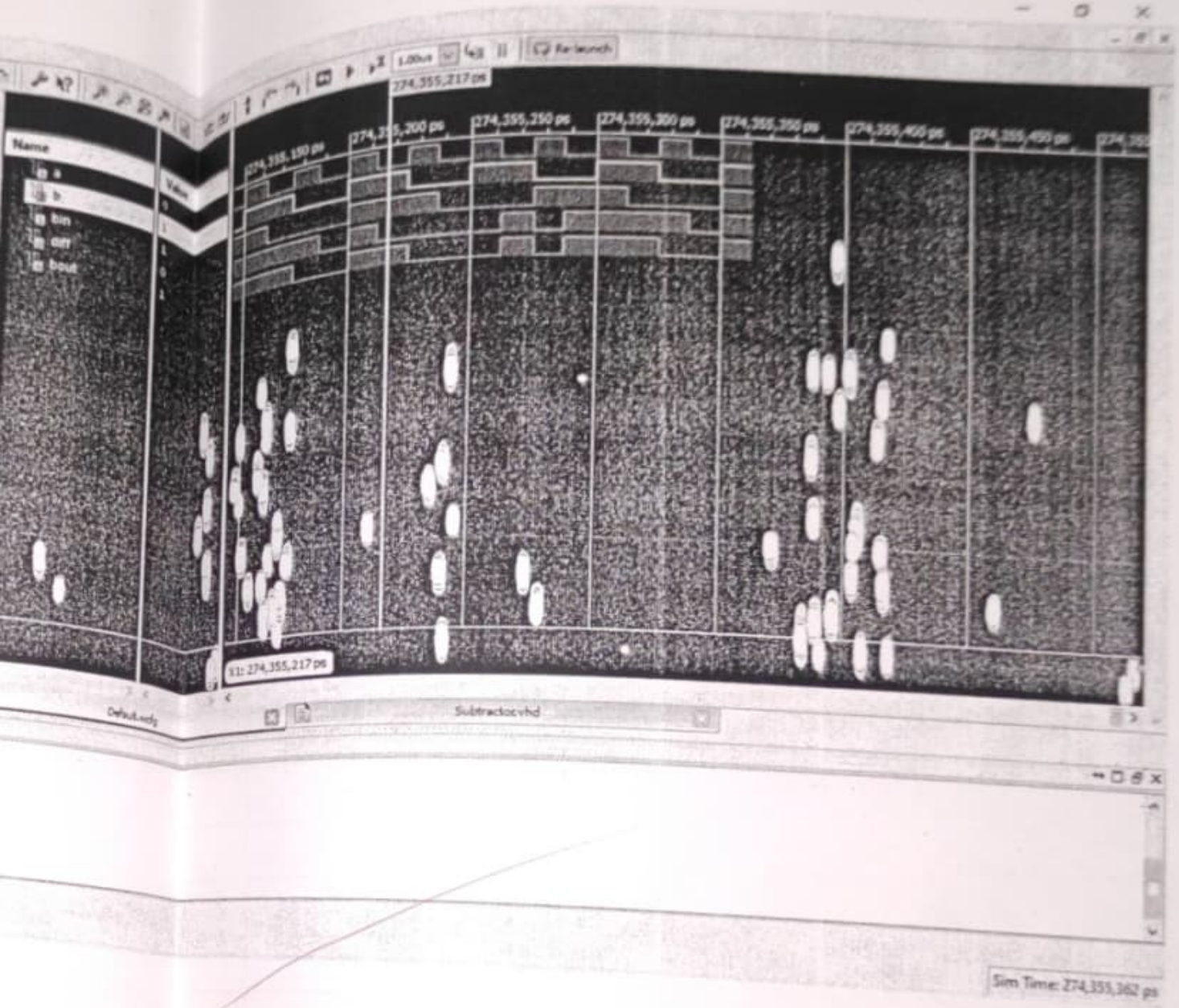


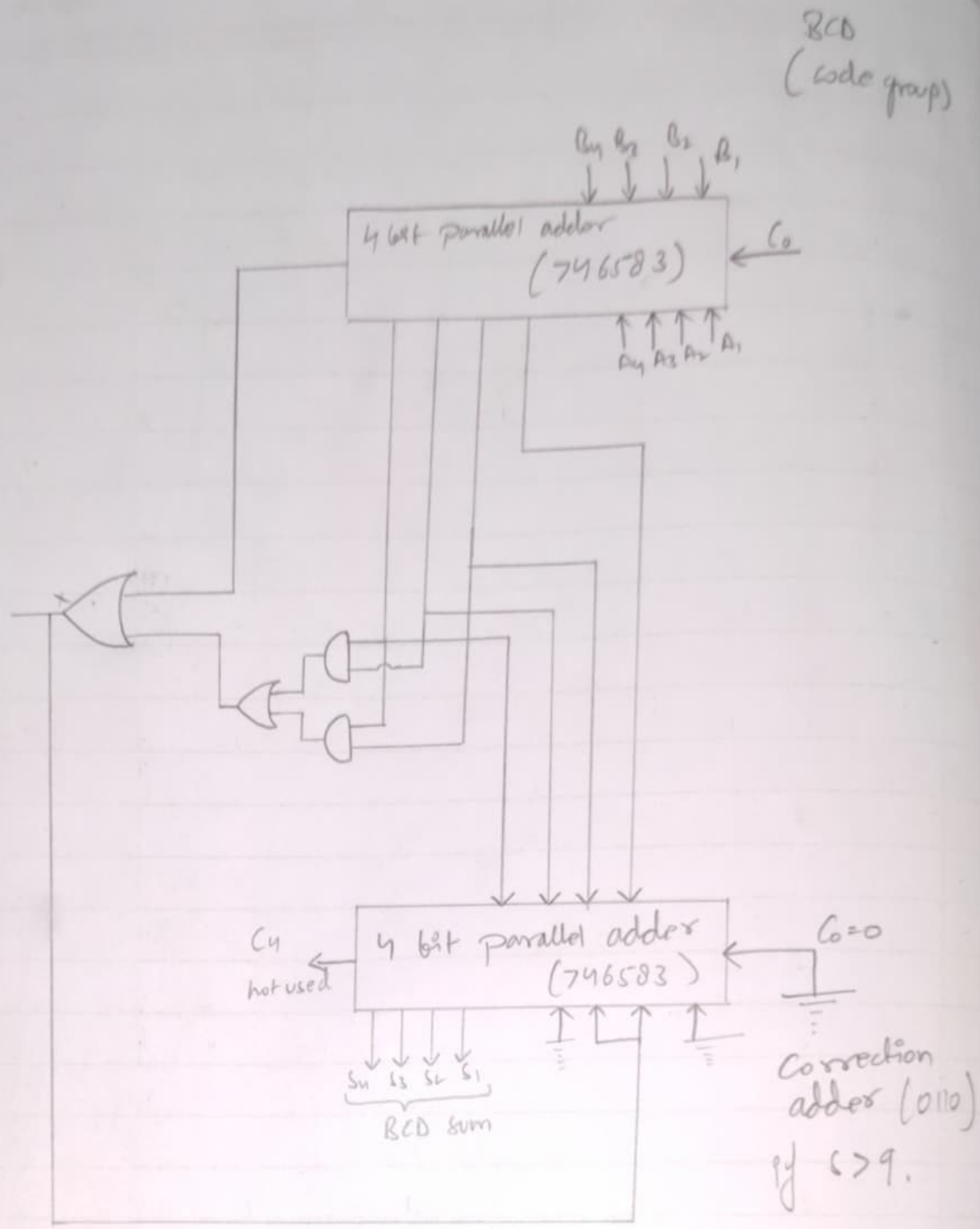

```
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Subtractor is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           bin : in  STD_LOGIC;
           diff : out  STD_LOGIC;
           bout : out  STD_LOGIC);
end Subtractor;

architecture Behavioral of Subtractor is

begin
   diff <= (a xor b) xor bin;

   bout <= ((not a) and bin) or (not a and b) or (b and bin);

end Behavioral;
```

Date

Expt. No.


Subtractor:1
and2
or3
b_bn_AND_3_o1
bout1
and2b1
Mxor_diff1
Mxor_diff1
Mxor_a_b_XOR_1_o1
Mxor_a_b_XOR_1_o1
Subtractor


Re-launch
274,355,217 ps
Name
Value
a
b
bin
cin
cout
274,355,150 ps
274,355,200 ps
274,355,250 ps
274,355,300 ps
274,355,350 ps
274,355,400 ps
274,355,450 ps
X1: 274,355,217 ps
Subtractor.vhd
Sim Time: 274,355,362 ps



Logic diag. of a BCD adder using two 4 bit adders & a correction detector circuit.

$$X = C_4 + S_4 S_3 + S_4 S_2 = C_4 + S_4 (S_3 + S_2)$$

EXPERIMENT- 10

AIM

To design and verify the logic circuit of BCD Adder using logic gates

APPARATUS REQUIRED

Breadboard, DC Power supply, LEDs, Digital ICs (Quad 2 Input AND 7408, Quad 2 Input OR 7432, 4 Bit Parallel Adder 7483)

THEORY

A BCD Adder is a logical circuit that is used for the condition process. It has 9 inputs, 4 of them augend and other addend and one is carry in. As the name suggests, BCD Adder is generally used for addition process based on the binary coded decimal codes.
During the process of addition using BCD technique. If sum is greater than 9 or carry out is 1, then add 6 to the sum to make it the accurate process of addition.

PROCEDURE

- Collect the components necessary to accomplish the experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips.
- Connect the supply voltage and ground lines to the chips and the switches of LED.

CONCLUSION

To add multiple bits in BCD form the logic circuit makes the simplest way to do this process. It is close of IC 7483 which is a 4-bit parallel adder.

Decimal digit	Uncorrected BCD sum					Corrected BCD sum				
	C_4	S_4	S_3	S_2	S_1	C_4	S_4	S_3	S_2	S_1
0		0	0	0	0	0	0	0	0	0
1		0	0	0	1		0	0	0	1
2		0	0	1	0		0	0	1	0
3		0	0	1	1		0	0	1	1
4		0	1	0	0		0	1	0	0
5		0	1	0	1		0	1	0	1
6		0	1	1	0		0	1	1	0
7		0	1	1	1		0	1	1	1
8		1	0	0	0		1	0	0	0
9		1	0	0	1		1	0	0	1
10		1	0	1	0	1	1	0	1	0
11		1	0	1	1	1	1	0	1	1
12		1	1	0	0	1	1	1	0	0
13		1	1	0	1	1	1	1	0	1
14		1	1	1	0	1	1	1	1	0
15		1	1	1	1	1	1	1	1	1
16	1	0	0	0	0	1	0	0	0	0
17	1	0	0	0	1	1	0	0	0	1
18	1	0	0	1	0	1	0	0	1	0
19	1	0	0	1	1	1	0	0	1	1

BCD Sum

S_3	S_2	S_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0
0	0	1

1	0
1	1
0	0
0	1
1	0
1	1
0	0
1	
0	
1	

RESULT

The logic circuit of BCD adder using logic gates has been designed and hence verified.