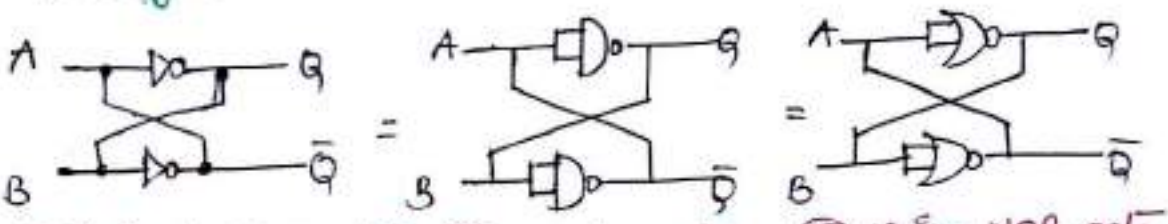
Binary Cell



(a) Using basic Inverter (b) NAND gate (c) Using NOR gate

⇒ Binary Cell is a basic bistable element used in latches and flipflops

⇒ Flip flops are basic building blocks of Sequential CKts.

→ A flip-flop is known as bistable multivibrator has two stable states.

→ It may remain in either of the state i;e ON state or OFF state. Two possible states — logic 0 – OFF
logic 1 – ON

→ Flipflop is also called as binary or one-bit memory.

→ when $A = 0 \Rightarrow Q = \bar{A} = 1 \Rightarrow B = \bar{A} = 1$

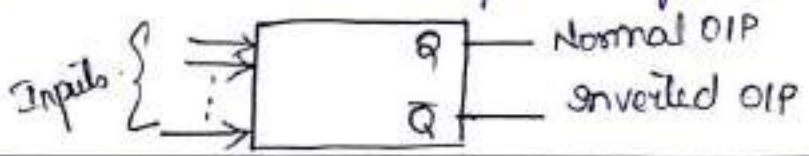
$$\bar{Q} = \bar{B} = \bar{1} = 0$$

when $A = 1 \Rightarrow Q = \bar{A} = 0 \Rightarrow B = \bar{A} = 0$

$$\bar{Q} = \bar{B} = \bar{0} = 1$$

⇒ Here the state flip flop always refers to the state of normal output Q and the inverted output $\bar{Q}$ is the opposite state.

⇒ ∴ Q and $\bar{Q}$ are two complementary outputs.



LATCHES

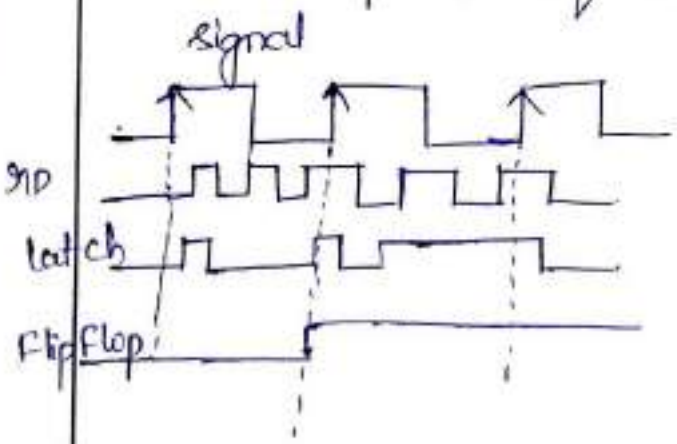
→ A latch is a sequential device that checks all its inputs continuously and changes its outputs accordingly at any time independent of a clock signal.

→ Latch is a non-clocked flipflop, upon 'latch on' to a 1 or 0 immediately upon receiving the input signal called SET (or) RESET.

→ A latch can be an active-HIGH input latch or an active-LOW input latch.

→ Active High → SET and RESET = LOW state
Active Low → SET and RESET = High state.

Difference between Latch and FlipFlop

Latch	FlipFlop
Latch is level sensitive ↓ positive level ↓ negative level.	Flip flop is Edge triggered ↓ +ve edge ↓ −ve edge
→ It is independent of clock signal	→ It is dependent on clock signal.
	Applications → Data storage → transfering of data → Counting → Frequency division → Parallel to serial & serial to parallel data conversions.

Case 2: $S = 1$ & $R = 0$

In this case $\bar{S} = 0$, $\bar{R} = 1$

→ For NAND1 → I/Ps $\bar{S} = 0$ from NAND logic if any I/P is 0. O/P = 1

So $Q = 1$

For NAND2 ⇒ I/Ps are $R = 1$ & $Q = 1$ so O/P $\bar{Q} = 0$

For inputs $S = 1$ & $R = 0$, $Q = 1$ i.e set state.

Case 3 $S = 0$ & $R = 1$

In this case $\bar{S} = 1$, $\bar{R} = 0$

For NAND2 ⇒ I/Ps are $\bar{R} = 0$ ⇒ O/P $\bar{S} = 1$

For NAND1 ⇒ I/Ps are $\bar{S} = 1$ $\bar{Q} = 1$ ⇒ O/P $Q = 0$

For inputs $S = 0, R = 1$ makes $Q = 0$ ⇒ Reset State

Case 4 $S = 1$ & $R = 1$

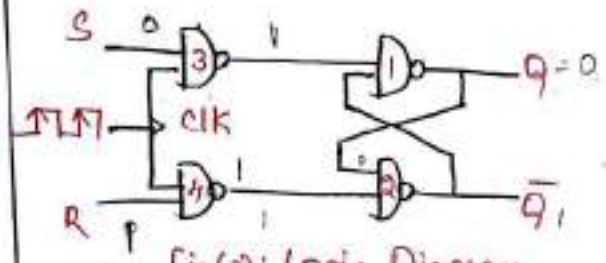
when $S = R = 1$, both the O/P's Q & $\bar{Q}$ try to become 1 which is not allowed, therefore $S = R = 1$ condition is prohibited

⇒ The S-R latch is also called R-S latch or S-C (Set-clear) latch.

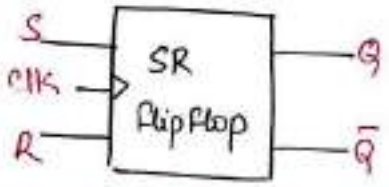
→ If Enable I/P is considered, it is called Gated SR latch instead of enable, a clock input is considered.

Clk	S	R	Q_n	Q_{n+1} (next state)	
1	0	0	0	0	} No change
1	0	0	1	1	
1	0	1	0	0	} Reset state
1	0	1	1	0	
1	1	0	0	1	} Set state
1	1	0	1	1	
1	1	1	0	x	} Unused state
1	1	1	1	x	Undetermined state
0	x	x	0	0	} No change.
0	x	x	1	1	

S-R Flip Flop



Fig(a): Logic Diagram



Fig(b): Logic Symbol

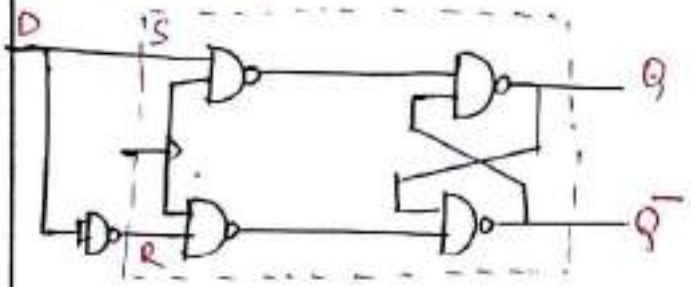
→ S and R Inputs ~~will~~ control the state of the flipflop only when the ~~clock~~ enable is high ~~or~~.

⇒ These types of flipflops are called level triggered flipflops. when the clock is high - edge triggered.

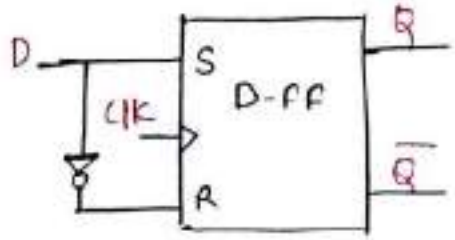
⇒ The Sequential ckts controlled by clock are called Synchronous sequential circuits

CP	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	} No change
↑	0	0	1	1	
↑	0	1	0	0	} Reset state
↑	0	1	1	0	
↑	1	0	0	1	} Set state
↑	1	0	1	1	
↑	1	1	0	x	} Indeterminate
↑	1	1	1	x	

D-FlipFlop



fig(a): Logic Diagram



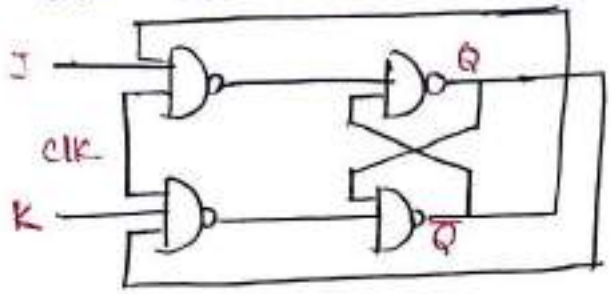
fig(b): Logic Symbol

CLK	D	Q_{n+1}
↑	0	0
↑	1	1
0	x	Q_n

fig(c): Truth table.

→ The O/P Q_{n+1} is delayed by one clk period, thus D-FF is called Delay flip flop.

JK FlipFlop



→ Here O/P is not available instantly because of 2 level NAND gates propagation delay

→ For single NAND gate propagation delay = 10ns

* Propagation Delay is always calculated interms of levels but not no of gates involved in the circuit.

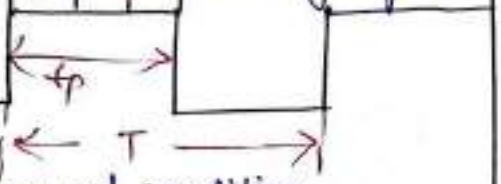
→ Here 2 levels of NAND gate so,

propagation delay = 2 × 10 = 20nsec.

* In J.K flipflop, when J=1, K=1 → O/P oscillates between 0 & 1, at the end of the clock pulse we don't know the O/P. This condition is called Race Around condition.

→ The problem in Race around is the O/P is changing many times during clock pulse

→ If we make the change const only one value, we can avoid this race around condition

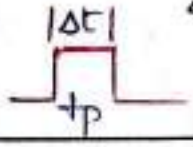


→ To avoid this less clock pulse (or) pulse width is required.

t_p → pulse width

Δt → propagation Delay

$t_p < \Delta t$ To avoid race around cond



J	K	Q_n	S	R	Q_{n+1}	
0	0	0	0	0	0	Q_n
0	0	1	0	0	1	
0	1	0	0	0	0	0
0	1	1	0	1	0	
1	0	0	1	0	1	1
1	0	1	0	0	1	
1	1	0	1	0	1	$\bar{Q}_n$
1	1	1	0	1	0	

fig(c): Truth table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

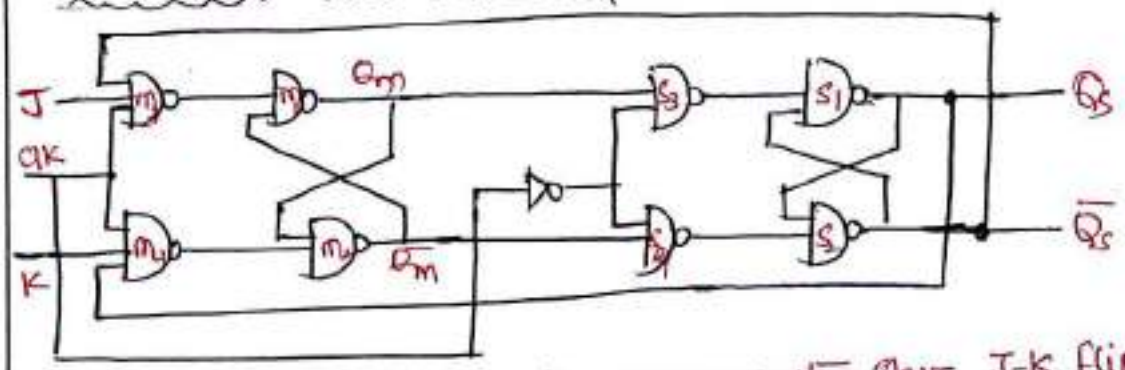
* Here the flipflop are edge triggered, so there ~~are~~ is positive edge triggering & Negative edge triggering.

→ A negative edge triggered JK flip flop is positive (J-K) FF operates in same way except that the change of state takes place only at the ~~clock~~ edge of the clock pulse. In J-K flip-flop, the excitations J=K=1 If the width of the clock pulse tp is too long, the state of the flip-flop will keep on changing from 0 to 1, 1 to 0, 0 to 1 and so on and at the end of clock pulse, its state will be uncertain. This phenomenon is called Race around condition.

$t_p < \Delta t < T$ → To avoid race around condition

→ It is only a theoritical approach but in practical not possible (∵ Δt is small (ns), we can't put t_p very small (ps) in practical).

Master Slave J-K Flip Flop



fig(a): Logic diagram of master Slave J-K flip flop

→ when clock = positive edge = Master – enable
Slave – disable

when J=K=1, Assume Q_s (present state) = 0, $\bar{Q}_s = 1$

Master → works when clk = ⎍

(i) For NAND m_3 ⇒ I/P's are ⇒ J = 1, $\bar{Q}_s = 1$
O/P is Q = 0

· for NAND m_1 ⇒ I/P is zero O/P = 1

So, $Q_m = 1$

ii) for NAND4 as $Q_s = 0 \Rightarrow$ o/p = 1

for NAND $m_2 \Rightarrow$ i/ps $Q_m = 1 \Rightarrow \overline{Q_m} = 0$

Slave works when clk = ⎍ clk = 0

$Q_m = S = 1$
$\overline{Q_m} = R = 0$ $\Rightarrow$ we know for SR flipflop when $S=1, R=0 \Rightarrow Q_s = 0$, $\overline{Q_s} = 1$

Slave simply Transfers (obeys) the master o/ps so called as master slave flipflop (Slave is followed by master)

→ So Race around condition is removed, because it is not oscillating.

COUNTERS

⇒ A counter is a register which counts the number of clock pulses arriving at clock input.

⇒ The counter is incremented by one with arrival of each clock pulse

⇒ The n-bit binary counter has n-flip-flops and it has 2^n distinct states of output.

→ For example · 2 bit binary counter

→ no of flip-flops = 2

No. of states $= 2^n = 4$ distinct state

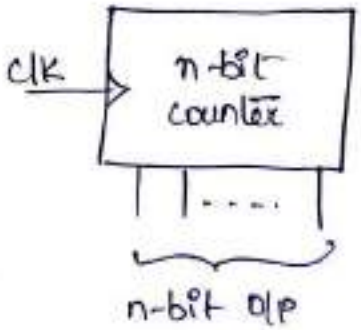
i;e 00, 01, 10, 11

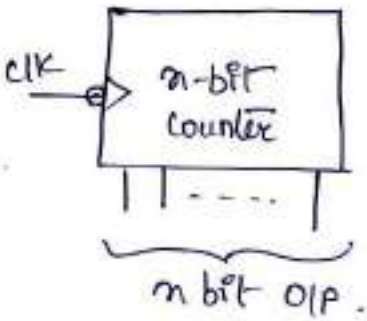
→

n-bit counter

positive edge triggered n-bit counter

Negative edge triggered n-bit counter.





The binary counter can count upto a maximum of 2^{n-1}

Characteristics of counters.

① Single or multi-mode operation

→ A counter is said to be single mode if only external inputs are clock and clear and the outputs are the states of flip flop outputs.

ex: Binary up counter and Binary down counter.

Multi mode: A single-mode counter with some external input control added to it is multimode counters.

ex: Up/down Counter —

② Number of Output bits

③ modulus of Counter.

Differences between Synchronous and Asynchronous Sequential ckts.

Synchronous Sequential ckt	Asynchronous Sequential ckt
⇒ Memory elements are clocked flipflops	⇒ Memory elements are either unclocked FFs or time delay elements
⇒ The change in input signals can affect memory elements upon activation of clock signal	⇒ change in input signal can affect memory elements at any instant of time.
⇒ The maximum operating speed of the clock depends on time delay	⇒ Operates faster than synchronous circuits ~~because~~ due to absence of clock.
⇒ Easier to design	⇒ More difficult to design.

Shift Registers

Register:- A group of flip-flops can be used to store a word, which is called register.

Need for Register:-

(i) Registers are used to store the binary information temporarily in digital system.

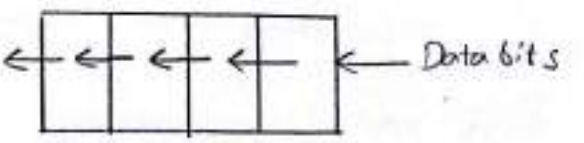
(ii) They helps in understanding the operation of digital computers and microprocessors.

(iii) They build an important link between main digital systems and inputs, output channels and microprocessors

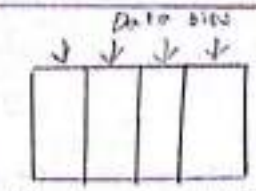
Shift Registers:-

- The binary information (data) in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called "shift register".
- They are very important in applications involving the storage and transfer of data in a digital system.
- Symbolic Representation of data movement in shift register operations:-

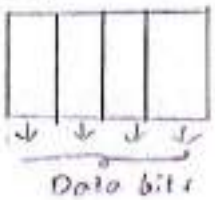
(a) Serial shift right, then out



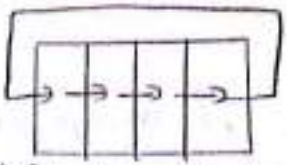
(b) Serial shift left, then out



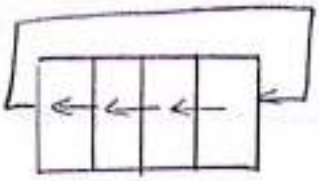
(c) parallel shift in



(d) Parallel shift out



(e) Rotate right



(f) Rotate right

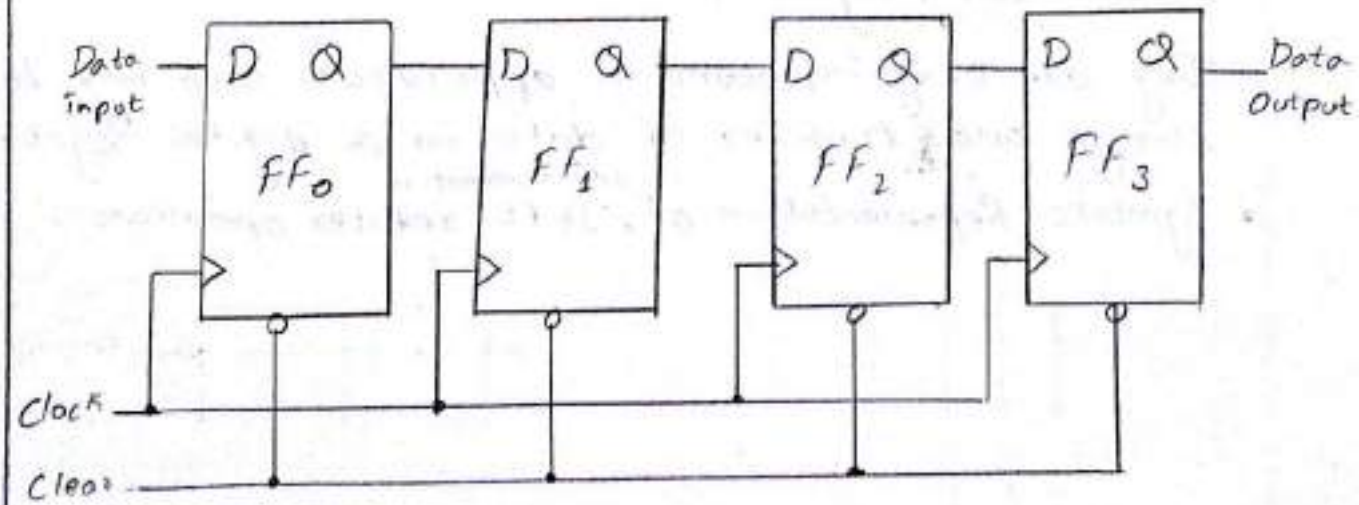
Types of Shift Registers:-

Shift Registers are of four types. They are:

1. Serial-in serial-out shift register
2. Serial-in parallel-out shift register
3. Parallel-in serial-out shift register
4. Parallel-in parallel-out shift register

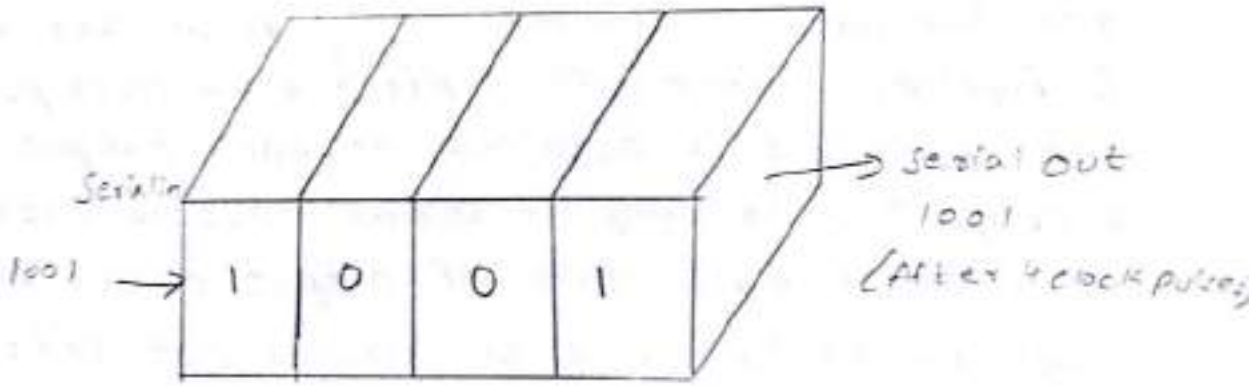
Serial-In Serial-Out Shift Register (SISO):-

The following figure shows the construction of serial-in serial-out shift register with four D-flipflops.



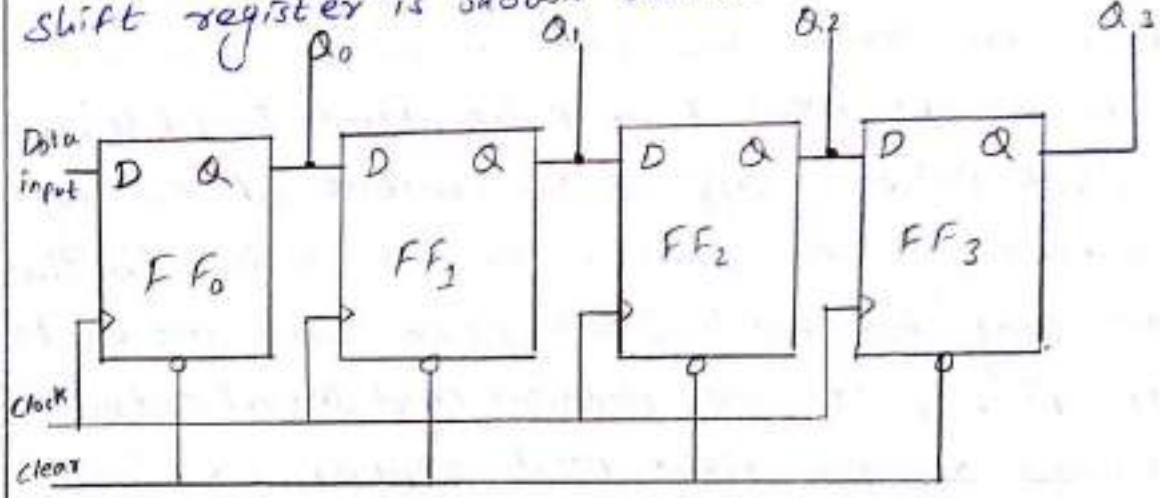
In the above figure four D-type flipflops namely D-FF1, D-FF2, D-FF3 and D-FF4 are used form a 4-bit serial-in-serial-out shift register. Initially, all flipflops are cleared and data is entered serially bit by bit from left most flipflop i.e., from D-FF4. When the clock pulse is applied, the content of the register is shifted by one position to the right. In the same way for each clock pulse data moves to the next flipflop by one position and serial output is obtained at the right most flipflop i.e., D-FF after four clock pulses.

The serial-in-serial-out operations for data input "1001" is illustrated in the below figure.

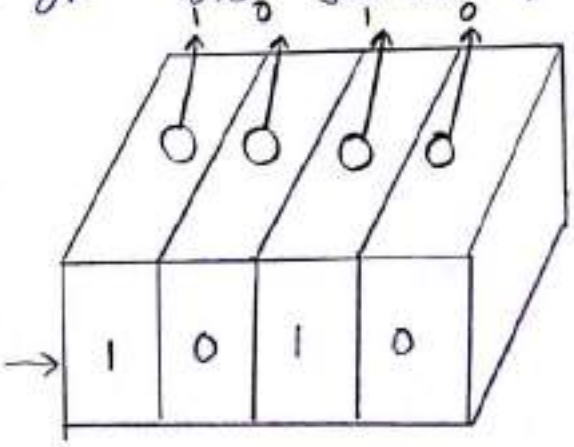


Serial-in-Parallel-out (SIPO) shift Register:

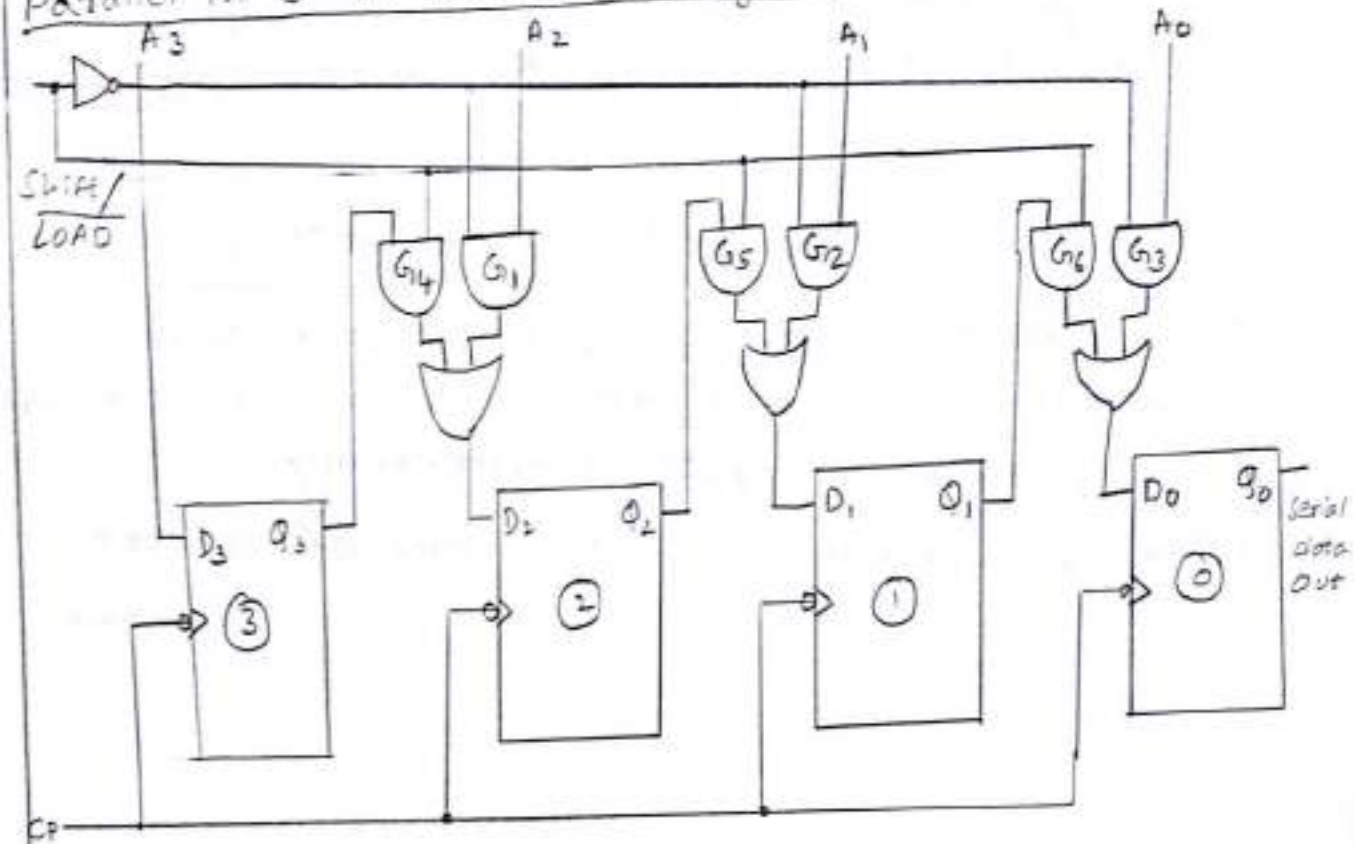
The circuit diagram of a 4-bit serial-in-parallel-out shift register is shown below.



In the above figure, 4-D flipflops namely D-FF1, D-FF2, D-FF3 and D-FF4 are used to form a 4-bit Serial-in, parallel-out register. Initially, all the flipflops are cleared by applying active low signal on clear. Once, the flip-flops are cleared, clock signal is applied and the data is entered serially from left most D-flipflop (i.e., from D-FF1). After each clock pulse, one data bit is obtained at each output of the flipflop. Thus, the complete serial input is obtained parallely at each stage of output after four clock pulses. The serial-in-parallel-out shift register operation of "1010" serial-input is illustrated below.



Parallel in Series out (PISO) Register

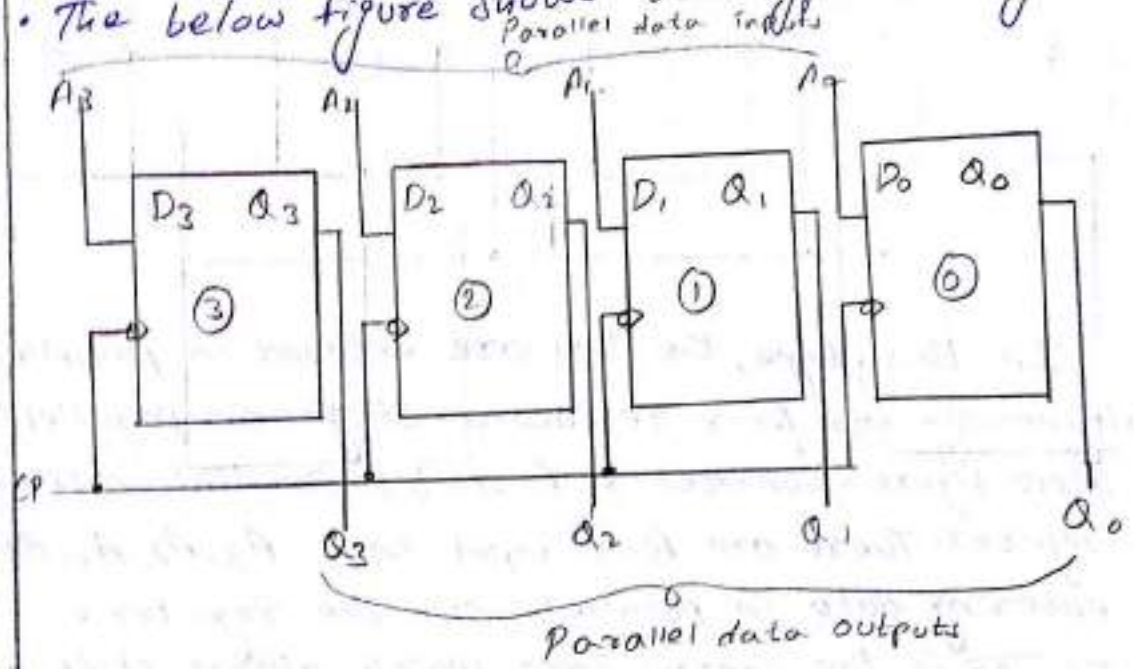


In this type, the bits are entered in parallel i.e, simultaneously into their respective stages on parallel lines. The above figure illustrates a four-bit parallel in serial out register. There are four input lines A_3, A_2, A_1, A_0 for entering data in parallel into the register. SHIFT/$\overline{LOAD}$ is the control input which allows shift or loading data operation of the register. When SHIFT/$\overline{LOAD}$ is low, gates G_1, G_2, G_3 are enabled, allowing each input data but to be applied to D input of its respective flip flop. When a clock pulse is applied, the flip-flops with D = 1 will SET and those with D = 0 will RESET. All four bits are stored simultaneously. When SHIFT/$\overline{LOAD}$ is high, gates G_1, G_2, G_3 are disabled and gates G_4, G_5, G_6 are enabled. This allows the data bits to shift right from one stage to the next. The OR gates at the D-inputs of the flip-flops allow either the parallel data entry operation or

Shift operation, depending on which AND gater are enabled by the level on the SHIFT/$\overline{LOAD}$ input.

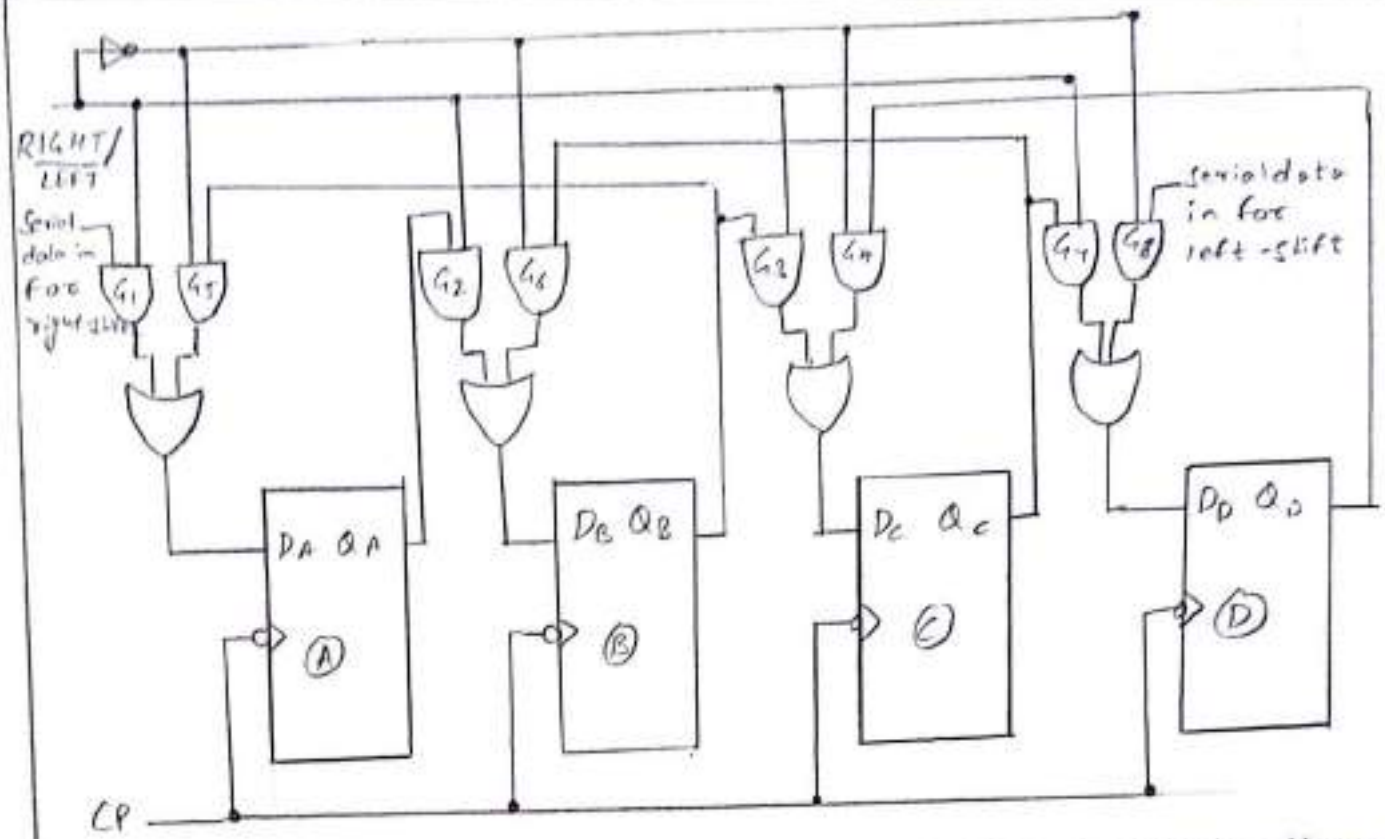
Parallel In Parallel Out (PIPO) Shift Register

- In parallel in parallel out register, there is simultaneous entry of data bits and the bits appear on parallel output simultaneously.
- The below figure shows this type of register.



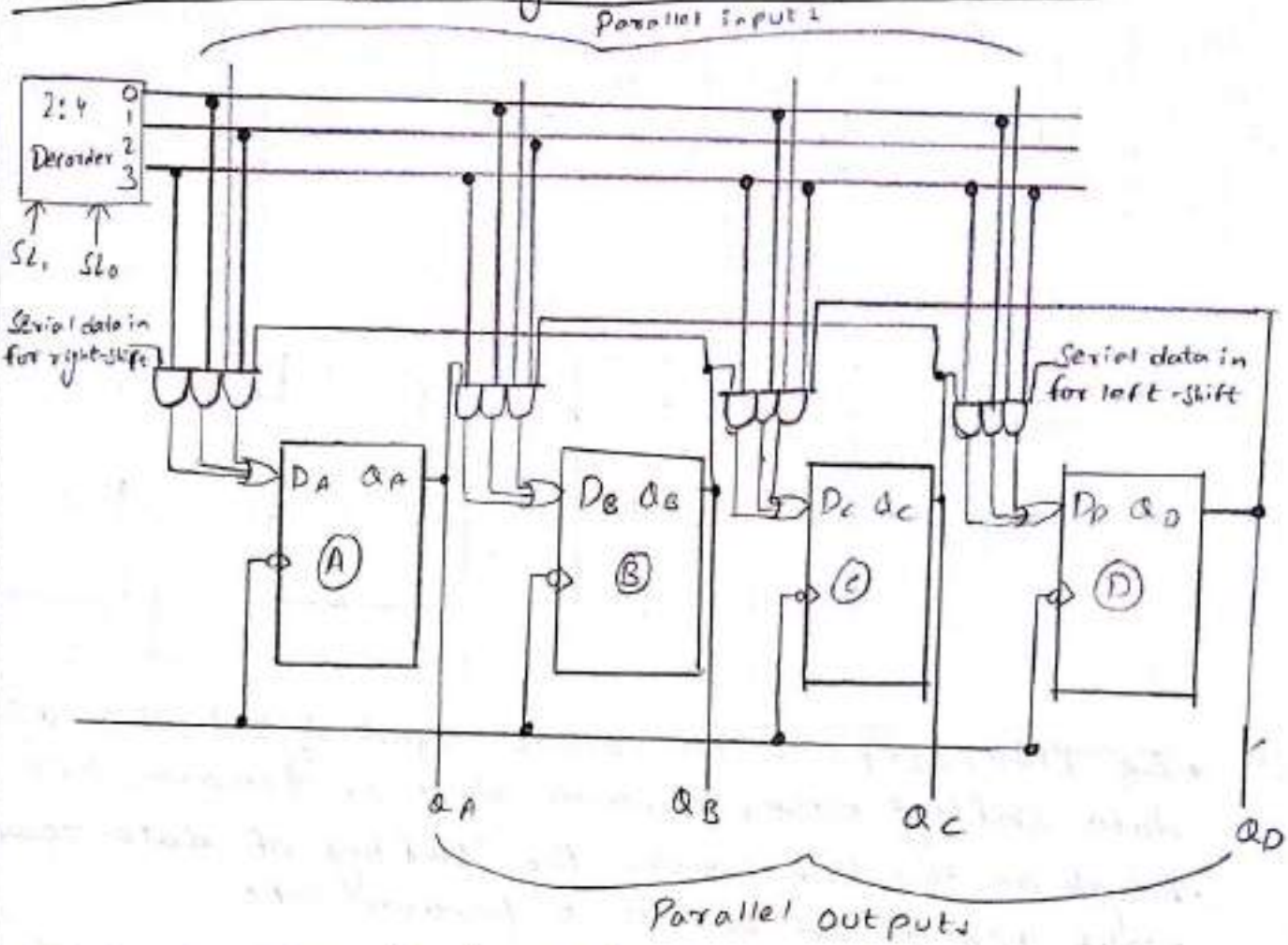
Bi-directional Shift Register:-

- This type of ~~shift~~ register allow shifting of data either to the left or to the right side. It can be implemented by using logic gate circuitry that enables the transfer of data from one stage to the next stage to the right or to the left, depending on the level of a control line.



- The RIGHT/$\overline{\text{LEFT}}$ is the control input signal which allows data shifting either towards right or towards left.
- A high on this line enables the shifting of data towards right and a low enables it towards left
- When RIGHT/$\overline{\text{LEFT}}$ signal is high, gates G_1, G_2, G_3, G_4 are enabled.
- The state of the Q output of each flip-flop is passed through the D input of the following flip-flop.
- When a clock pulse arrives, the data are shifted one place to the right.
- When the RIGHT/$\overline{\text{LEFT}}$ signal is low, gates G_5, G_6, G_7, G_8 are enabled.
- The Q output of each flip-flop is passed through the D input of the preceding flip-flop.
- When clock pulse arrives, the data are shifted one place to the left.

Bidirectional Shift Register with Parallel load:-



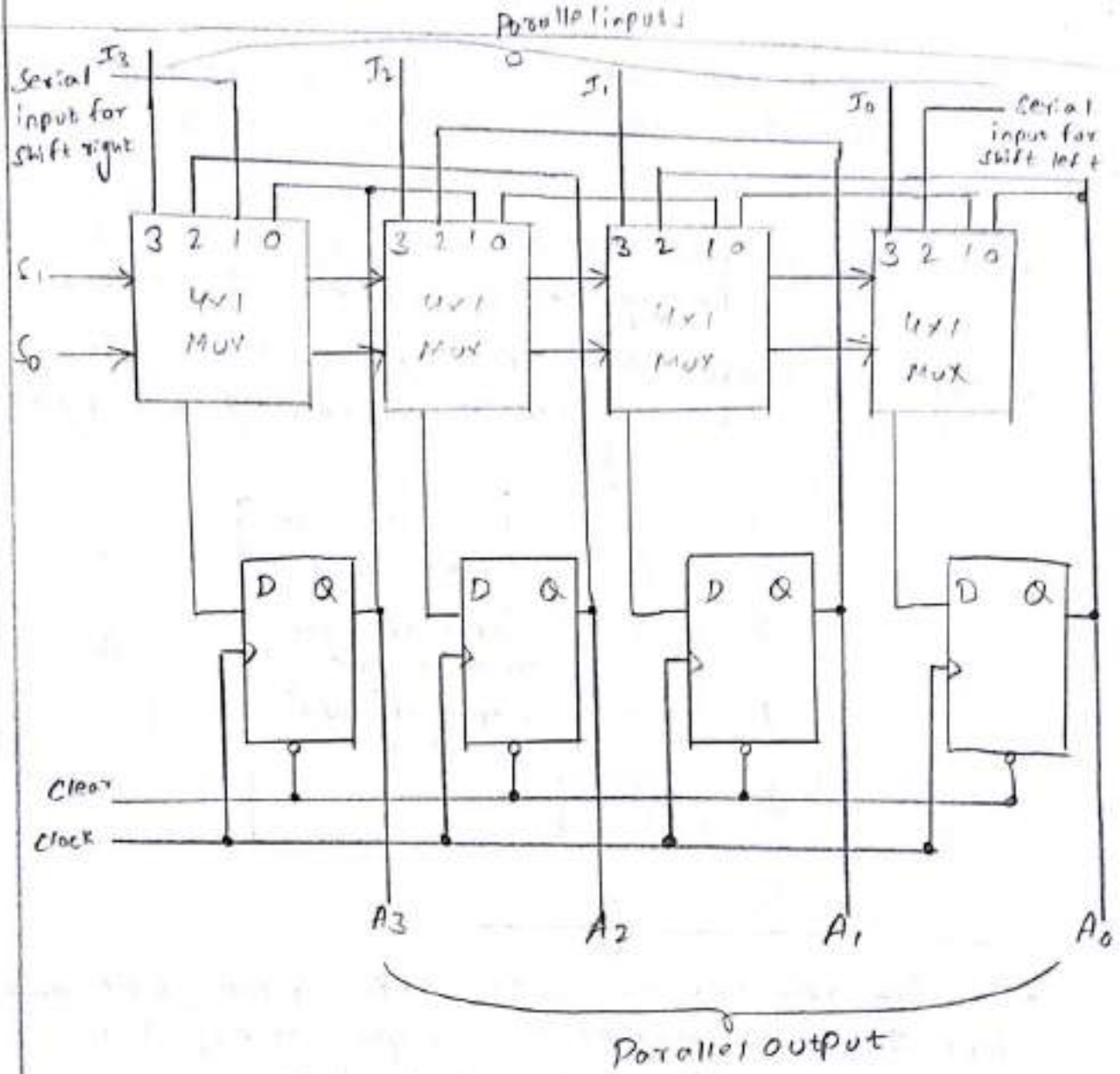
- When parallel load capability is added to the shift register, the data entered in parallel can be taken out in serial fashion by shifting the data stored in the register. Such a register is called bidirectional shift register with parallel load.
- As shown in the figure, the D input of each flip-flop has three sources: Output of left adjacent flip-flop, output of right adjacent flip-flop, and parallel input. Out of these three sources one source is selected at a time and it is done with the help of decoder. The decoder seled lines (S_1 and S_0) select the one source out of three as shown in Table.

- When select lines are 00 (i.e., $SL_1 = 0$ and $SL_0 = 0$) data from the parallel inputs is loaded into 4-bit register.
- When select lines are 01 (i.e., $SL_1 = 0$ and $SL_0 = 1$) data within the register is shifted 1-bit left.
- When select lines are 10 (i.e., $SL_1 = 1$ and $SL_0 = 0$) data within the register is shifted 1-bit right.

SL_1	SL_0	Selected Source
0	0	parallel input
0	1	output of right adjacent FF
1	0	output of left adjacent FF
1	1	—

Universal Shift Register:-

- If the register has both shifts (right shift and left shift) and parallel load capabilities, it is referred as Universal shift register.
- It consists of four flip-flops and four multiplexers.
- The four multiplexers have two common selection inputs S_1 and S_0 and they select appropiate input for D flip-flop.



- The table shows the register operation depending on the selection inputs of multiplexers.

Mode control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

- When $S_1 S_0 = 00$, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in the register value.
- When $S_1 S_0 = 01$, input 1 is selected and circuit connections are such that it operates as a right shift register.
- When $S_1 S_0 = 10$, input 2 is selected and circuit connections are such that it operates as a left shift register.
- Finally, when $S_1 S_0 = 11$, the binary information on the parallel input lines is transferred into the register simultaneously and it is parallel load operation.

COUNTERS

Introduction :-

A counter is a sequential machine that produces a specified count sequence. The count changes when ever the input clock is asserted.

Design of Counters :-

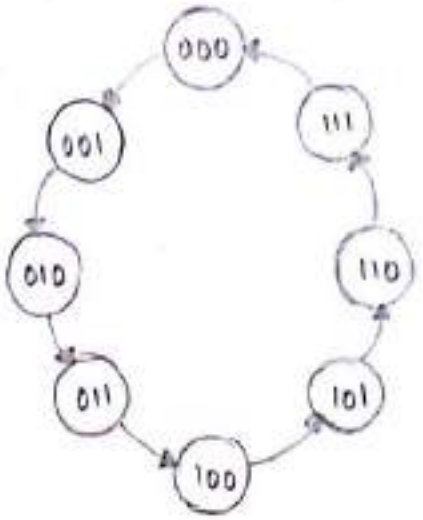
A sequential circuit that goes through a prescribed sequence of states upon the application of input pulses is called a counter. The input pulses, called count pulses, may be clock pulses. Counters are found in almost all equipment containing digital logic.

* They are used for counting the number of occurences of an even and are useful for generating timing sequences to control operation in a digital system.

* A counter that follows the binary sequence is called a binary counter. An n-bit binary countains of n-flip-flops and can count in binary form 0 to $2^n - 1$.

Ex :-

* A counter is first described by a state digram, which is shown for the sequence of states through which the counter advances when it is clocked. The above diagram shows the 3-bit binary counter.



State diagram of a 3-bit binary counter.

The circuit has no inputs other than the clock pulse and no outputs other than its internal state (outputs are taken off each flip-flop in the count

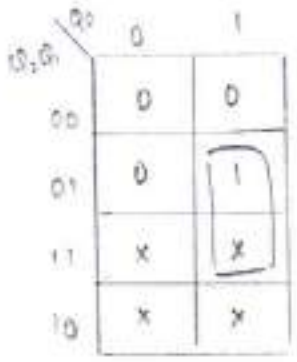
The next state of the counter depends entirely on its present state, an the state transition occurs every time the clock pulse occurs.

Present state			Next state		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

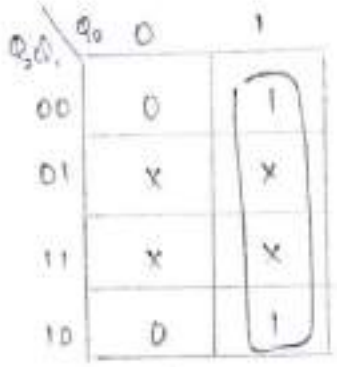
Since there are eight states, the number of flip-flops required would be three. Now we want to implement the counter diagram using JK flip-flops. Next step is to develop an excitation table from the stable table.

Output State Transitions						Flip-flop inputs		
Present state			Next state					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2K_2	J_1K_1	J_0K_0
0	0	0	0	0	1	0x	0x	1x
0	0	1	0	1	0	0x	1x	x1
0	1	0	0	1	1	0x	x0	1x
0	1	1	1	0	0	1x	x1	x1
1	0	0	1	0	1	x0	0x	1x
1	0	1	1	1	0	x0	1x	x1
1	1	0	1	1	1	x0	x0	1x
1	1	1	0	0	0	x1	x1	x1

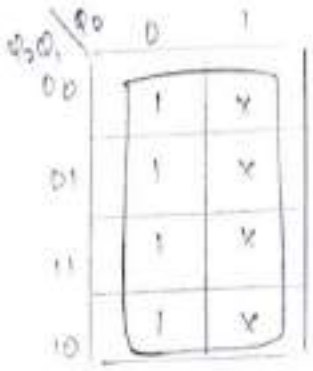
Now transfer the JK states of the flip-flop inputs from the excitation table to karnaugh maps to derive a simplified boolean expression for each flip-flop input. This is shown below.



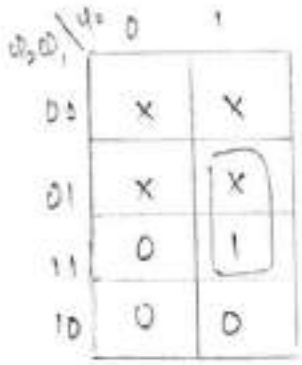
J_2 map



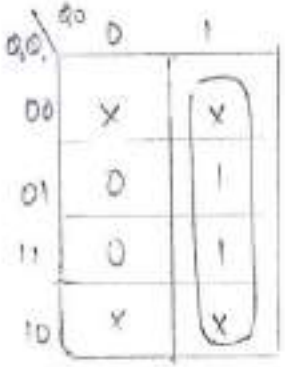
J_1 map



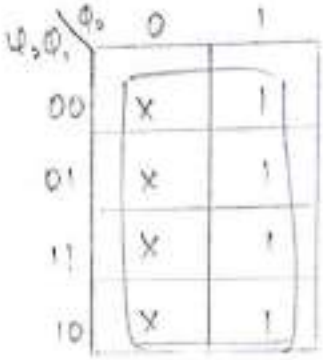
J_0 map



K_2 map



K_1 map



K_0 map

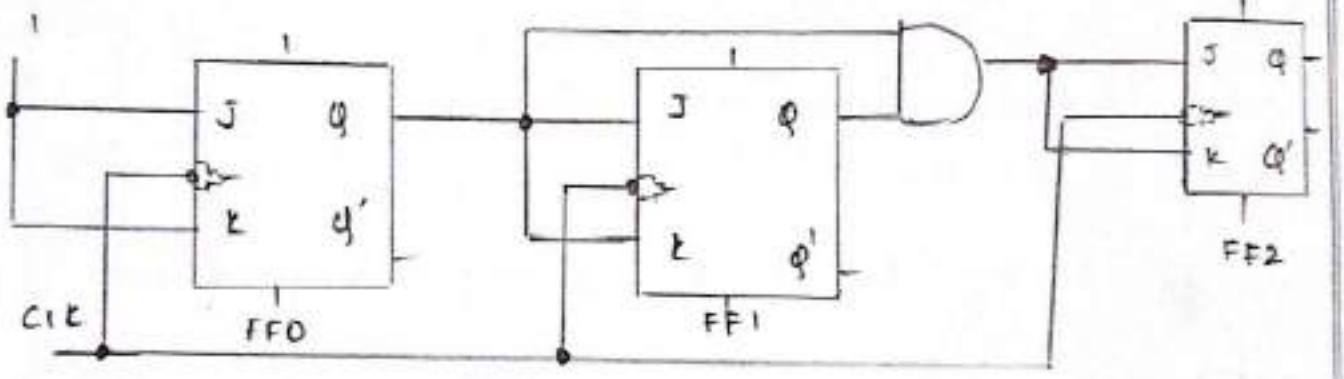
The 1s in the karnaugh maps are grouped with "don't cares" and the following expressions for the J and K inputs of each flip-flop are obtained.

$$J_0 = K_0 = 1$$

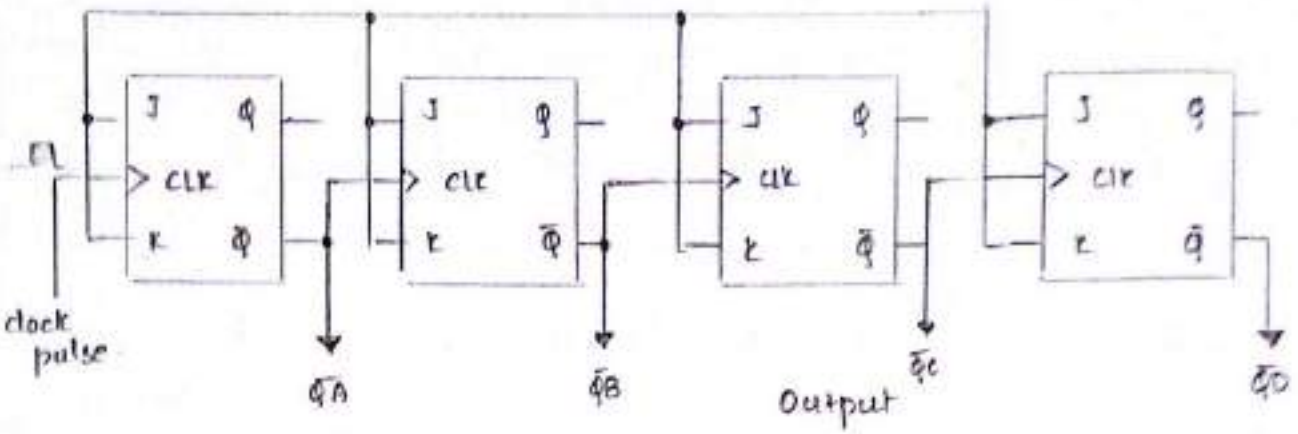
$$J_1 = K_1 = Q_0$$

$$J_2 = K_2 = Q_1 * Q_0$$

The final step is to implement the combinational logic from the equations and connect the flip-flops to form the sequential circuit. The complete logic of a 3-bit binary counter is shown below.



Bidirectional Counters (or) Up Down Counters

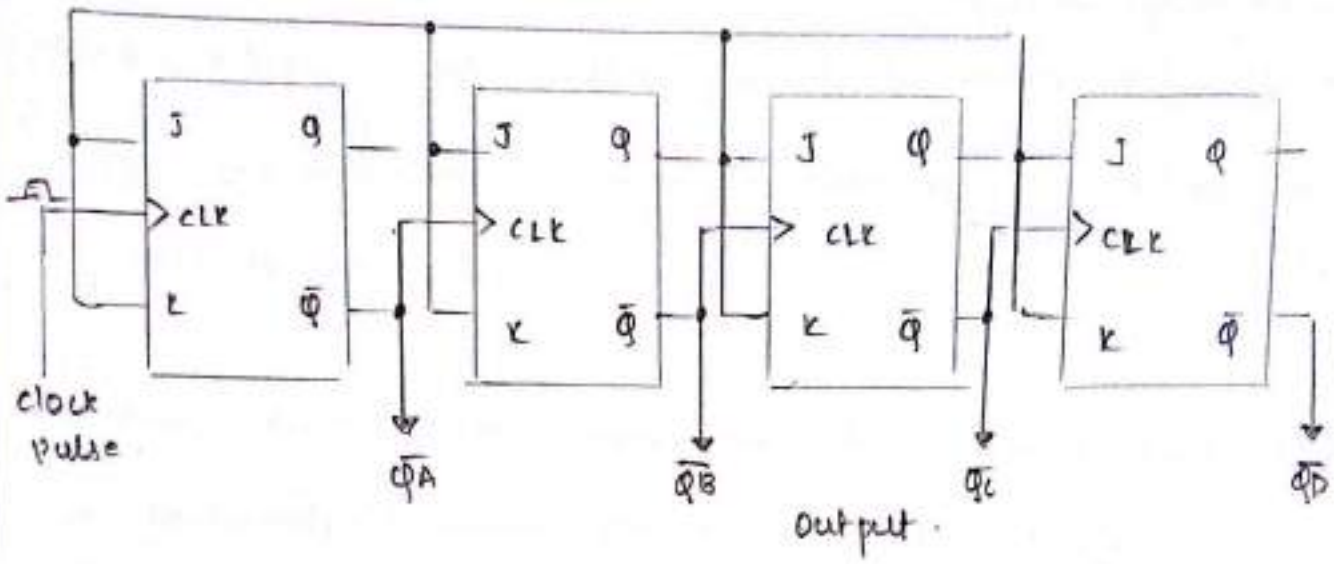


→ As well as counting "up" from zero and increasing or incrementing to some preset value, it is sometimes necessary to count "down" from a predetermined value to zero allowing us to produce an output that activates when the zero count or some other pre-set value is reached.

→ This type of counter is normally referred to as a Down Counter. In a binary or BCD down counter, the count decreases by one for each external clock pulse from preset value.

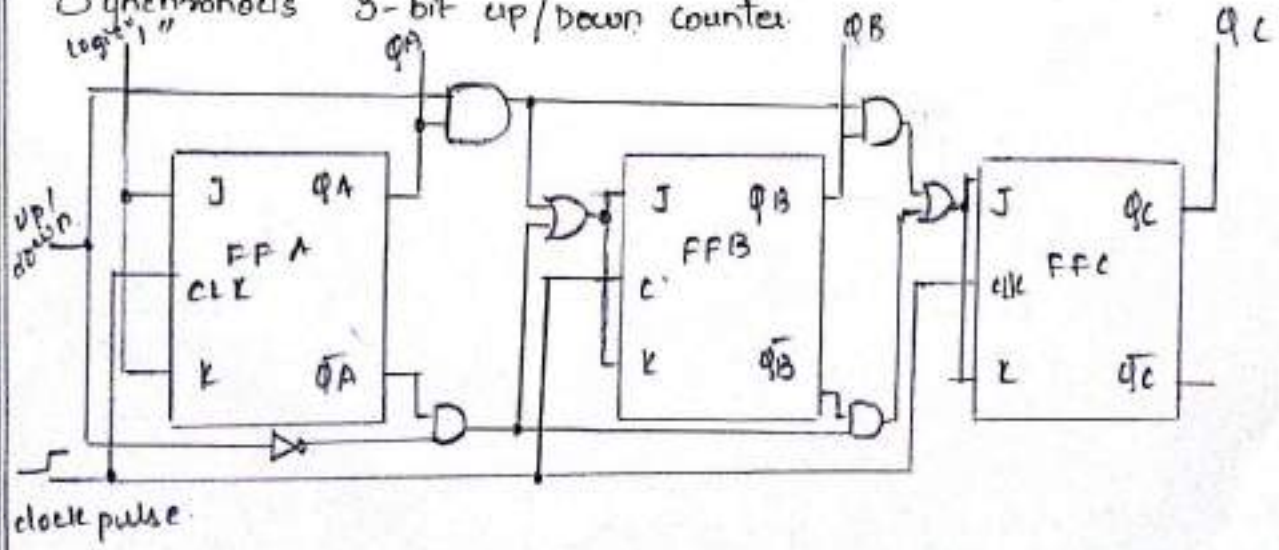
→ 4- bit binary up or down counters which have an additional input pin to select either the up or down count mode.

4- Bit Count Down Counter :-



→ In the 4-bit counter above the output of each flip-flop changes state on the falling edge of the CLK input which is triggered by the $\bar{Q}$ output of the previous flip-flop, rather than by the Q output as in the up counter configuration.

Synchronous 3-bit up/down counter

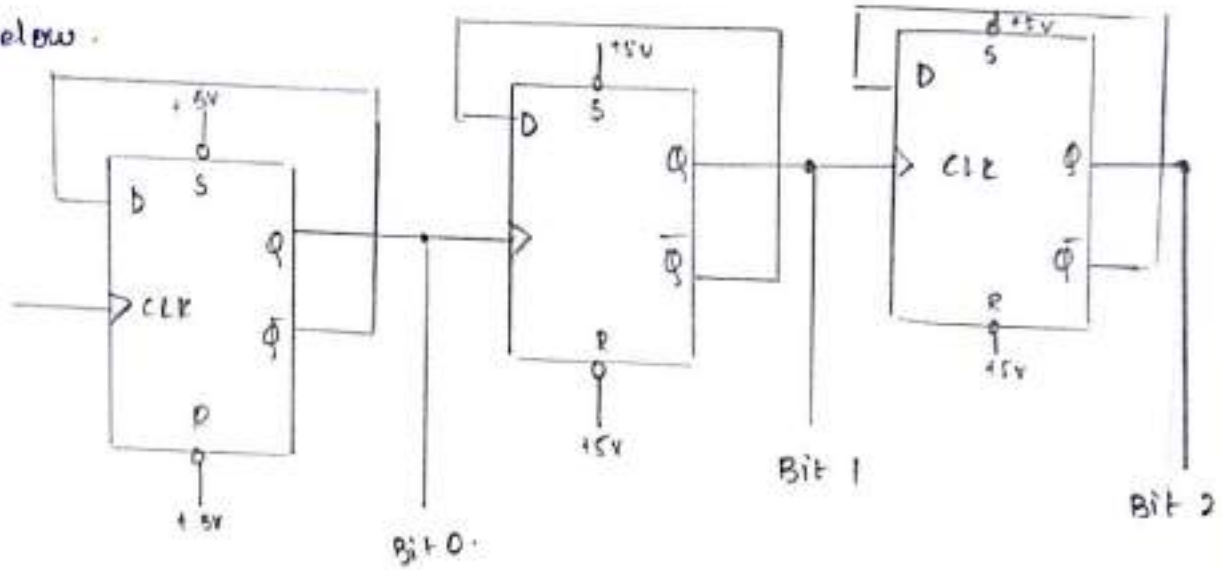


→ The circuit above is of a simple 3-bit up/down synchronous counter using JK flip-flops configured to operate as toggle or T-type flip-flop. giving a maximum count of zero (000) to seven (111) and back to zero again.

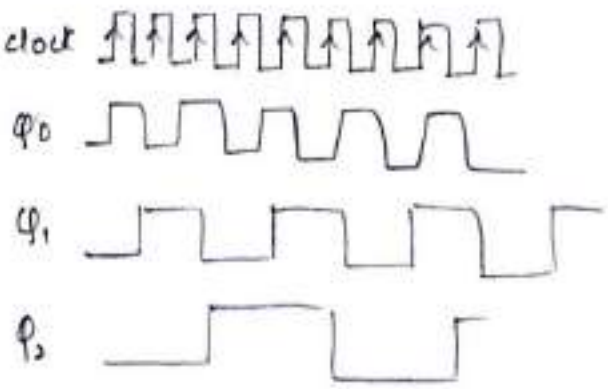
→ Then 3-bit counter advances upward in sequence (0,1,2,3,4,5,6,7) or downwards in reverse sequence (7,6,5,4,3,2,1,0).

Ripple Counter

→ A good first thought for making counters that can count higher is to chain divide by - 2 counters. We can feed the Q out of on flop into the clk of the next stage. The result looks like the below.



→ The ripple counter is easy to understand. Each stage acts as a Divide-by-2 counter on the previous stage's signal. The Q out of each stage acts as both an output bit, and as the clock signal for the next stage.



→ We can chain as many ripple counters together as we like. A three bit- ripple counter will count $2^3 = 8$ numbers, and an n-bit ripple counter will count 2^n numbers.

→ The propagation delay does not only slow down the counter, but it actually introduces errors into the system. These errors increase as we add additional stages to the ripple counter.

The 555 Timer Introduction:-

Signetic Corporation Introduced the device SE/NE 555 IC in early 1970s

Applications of 555 Timer:- It can be used as

1. Monostable & Astable multivibrators
2. DC-DC Converters
3. Digital logic probes
4. Waveform generators
5. Analog frequency meters
6. Tacho meters
7. Temperature measurement and Control
8. Infra red transmitter
9. Burglar
10. Toxic gas alarm
11. Voltage Regulators
12. Electonic Eye
13. In many high stable time delay oscillators.

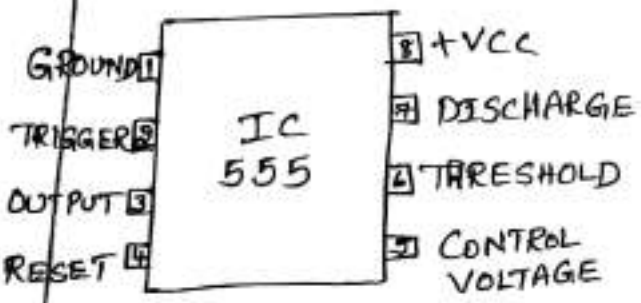
Features of Timer:-

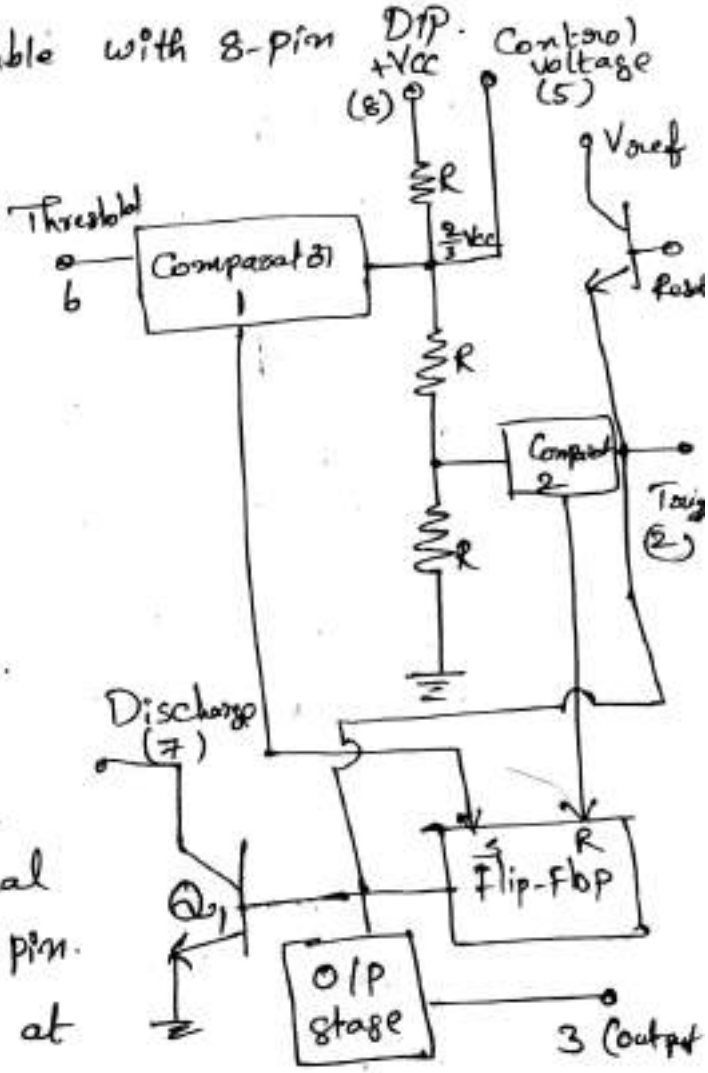
1. The 555 is a monolithic timer which can be used to produce accurate and highly stable time delays & Oscillations
2. It can be used to produce timedelay of few micro seconds to several hours.
3. It has two basic operating modes: Monostable & Astable
4. It is available in three packages: 8-Pin metal can, 8-Pin DIP and 14-Pin DIP. Where IC 556 contains two 555 timers.

4. It can operate with supply voltage 4.5 V to 18 V.
5. Sourcing and Sinking out put Currents 200mA
6. CMOS IC's can operate coith 2V to 18V and Cuoreut Sinking and Sourcing capabilities 100mA and 10mA
7. It has veay high temperature stabilpty, designed to operate in the temperature orange of -55°C to 125°C
8. Its Output is Compatible with TTL, CMOS and Op-Amp Circuits.

Functional Diagram:—

This device is available with 8-pin DIP.





Pin 1:- Ground

All voltages are measured with respect to the terminal.

Pin 2:- Trigger

Output of timer depends on the amplitude of the external trigger pulse applied to this pin. Output is low if the voltage at this pin is greater than $\frac{2}{3}$ Vcc, when a negative going pulse of amplitude larger than $\frac{1}{3}$ Vcc, the comparator 2 output goes to low, which inturn switches the o/p of the timer High.

Output remains high as long as the trigger terminal is held at a low voltage.

Pin3 : Output terminal :-

Output of the timer available at this pin.

There are two ways to connect the load.

1. Either between pin 3 and ground pin (1) → Off load (Normally)
2. Either between pin 3 and supply pin (8) → On load (Normally)

Pin4 : Reset terminal :-

To disable the timer a negative pulse is applied to this pin due to which it is referred to as reset terminal.

If this pin is not used for reset purpose, it should be connected to +Vcc to avoid any possibility of false triggering.

Pin 5 : Control Voltage Terminal :-

It is used to control the threshold and trigger levels. An External voltage or a pot connected to this pin determines the pulse width of the output waveform.

The External voltage applied to this pin can also be used to modulate the output waveform.

If this pin is not used, it should be connected to ground through a 0.01 μF to avoid any noise problem

Pin 6 : Threshold Terminal :-

This is the non-inverting input terminal of Comparator 1, which compares the voltage applied to this terminal with a reference voltage of $+\frac{2}{3}V_{CC}$.

Amplitude of voltage applied to this terminal is responsible for the set of flip-flop.

Pin 7 : Discharge terminal :-

This pin is connected internally to the collector of transistor and a capacitor is connected between this terminal and ground ~~terminal~~ as

If the transistor saturated, the capacitor discharges through the transistor.

When the transistor is cutoff, the capacitor charges at a rate determined by external resistor and capacitor

Pin 8 : Supply Terminal :-

A supply voltage of +5 V to +18 V is applied to this terminal with respect to ground.

Basics of 555 Timer :-

It consists of a relaxation oscillator, two comparators, an RS-Flip-Flop and a discharge capacitor.

RS-Flip Flop :-

A pair of cross-coupled transistors, each collector driving the opposite base through resistance RB

One transistor is saturate while the other is cutoff.

Saturated transistor collector voltage is zero

Cut off transistor collector voltage is +Vcc.

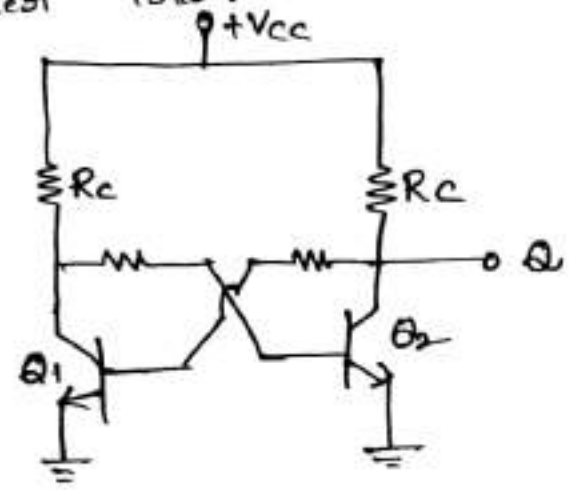
This high voltage produces enough base current to keep transistor Q_1 in saturation

There is no base drive for transistor Q_2 and it goes in to cut off.

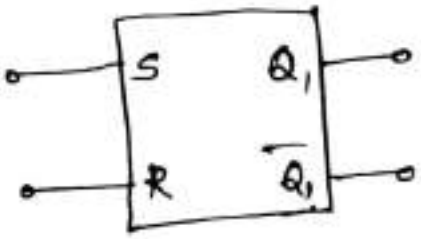
Depending on which transistor is saturated, the Q output is either low or high.

By adding more components to the circuit an R-S flip-flop is obtained.

R-S flip-flop is a circuit that can set the output to high or reset it Low.
A Complementary output is available from the collector of the other transistor

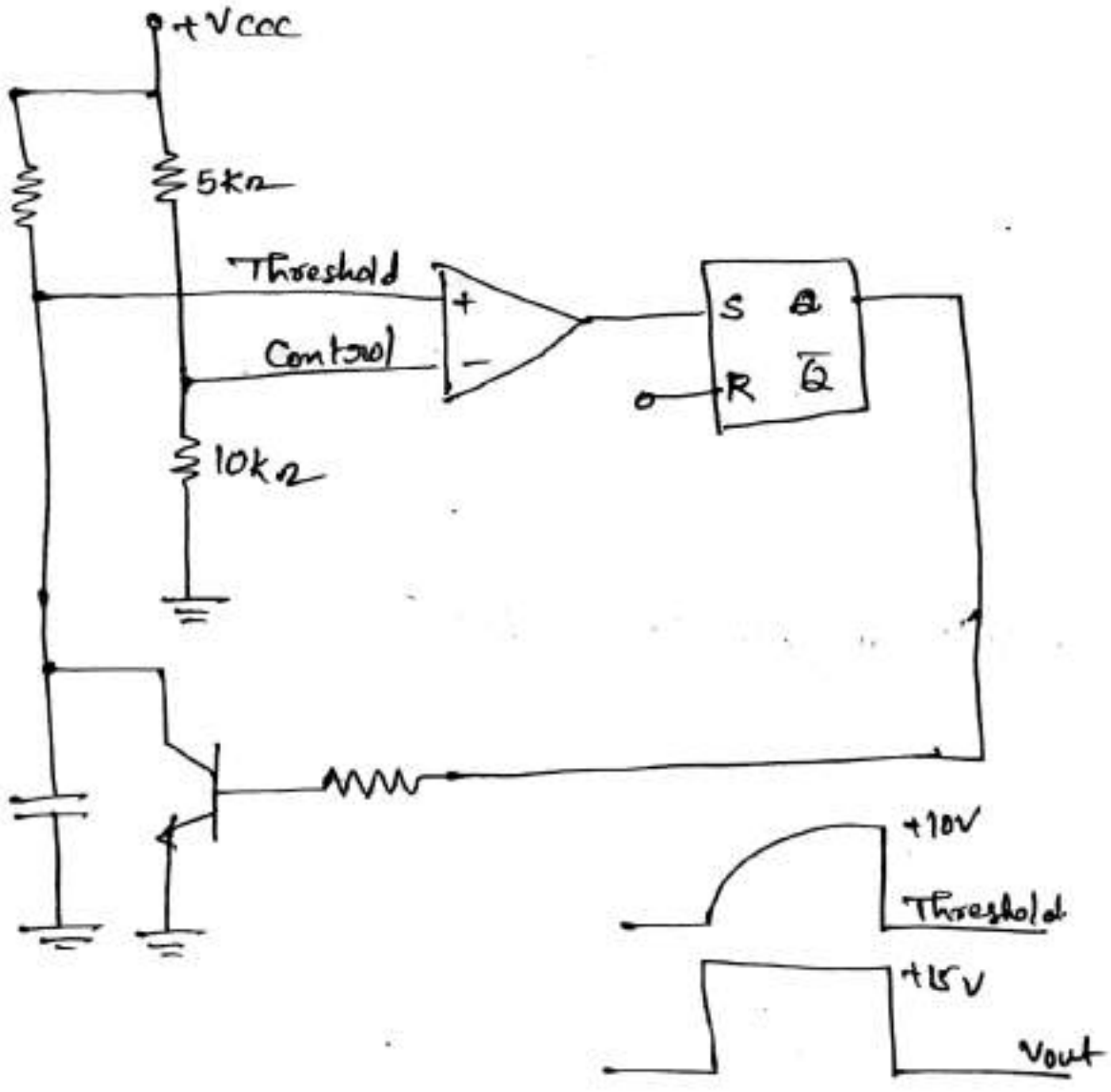


circuit Diagram



Symbol

Basic Timer Circuit :—



Assume output of flip-flop Q is high, the transistor saturated and the capacitor voltage clamped to zero on ground since the capacitor C is shorted and cannot charge

→ Non Inverting input voltage of the comparator is referred to as threshold voltage.

→ While the inverting input voltage is referred as Control voltage.

→ If the RS flip flop set, the saturated transistor holds the threshold voltage at zero. Thus Control voltage is fixed at $\frac{2}{3}$ Vcc [5kΩ & 10kΩ] $\frac{10}{15} \times Vcc = \frac{2}{3} Vcc$

→ If a high voltage applied to the R input, that resets the flip-flop, Output Q goes low and the transistor is driven into Cutoff.

→ Now Capacitor starts to charge to threshold voltage rises.

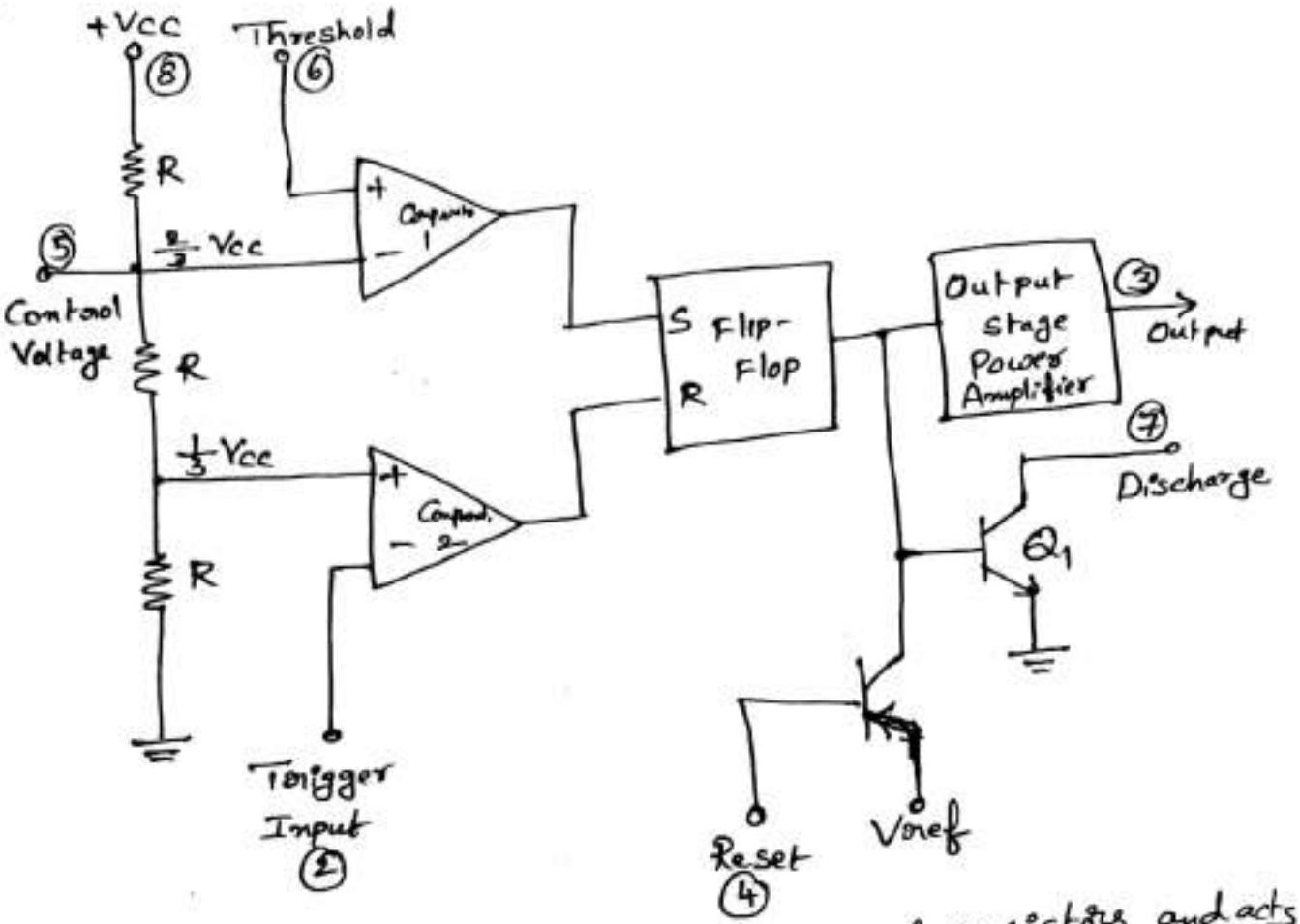
→ Hence the O/P of the Comparator then goes high, forces the R-S flip-flop to set.

The high output saturates the transistor and quickly discharges the capacitor.

Block diagram of 555 Timer :—

It Consists of two Comparators, An R-S flip-flop two transistors.

Resistive network Consists of three equal resistors and act as a voltage devider.



Resistive network consists of three equal resistors and acts as voltage divider

Comparator 1 Compares threshold voltage with a reference Voltage of $+\frac{2}{3}$ Vcc.

Comparator 2 Compares the trigger voltage with a reference Voltage of $+\frac{1}{3}$ Vcc volts

Output of both the Comparators is supplied to the flip-flop Flip flop, state is decided based on the output of the two Comparators.

One of the two transistors is a discharge transistor of which Collector is connected to the pin 7.

The transistor Saturation and Cutoff is decided by the output state of the flip-flop.

Saturated transistor provides a discharge path to a Capacitor Connected externally.
A pulse is applied to another Base of transistor resets the whole times Irrespective on any input

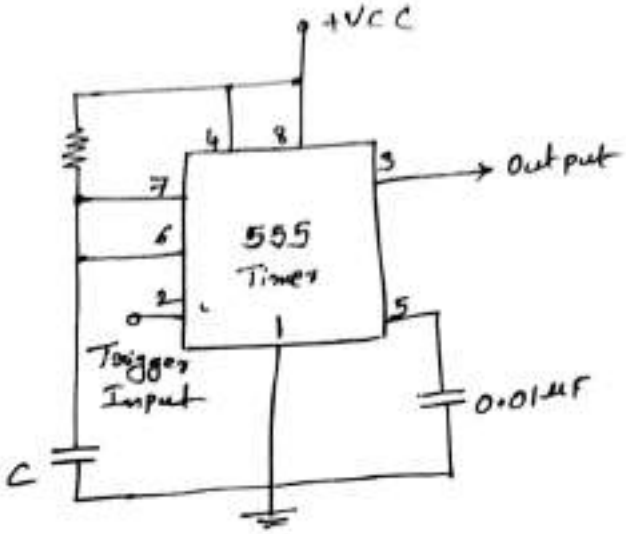
Working Of the 555 - timer :—

Comparator 1 has a threshold input and a Control input.
In most of the applications, the Control input is not used as that the Control voltage equal to $+\frac{2}{3}VCC$
Output of this Comparator is applied to Set input.
Whenever the threshold voltage greater than Control voltage, Comparator will set the flip-flop, saturates the transistor which discharge the Capacitor.
To Change the output of flip-flop to low, the Voltage at the trigger input must fall below $\frac{1}{3}$ Vcc then Comparator 2 triggers the flip-flop turn the discharge transistor and Charges the Capacitor.

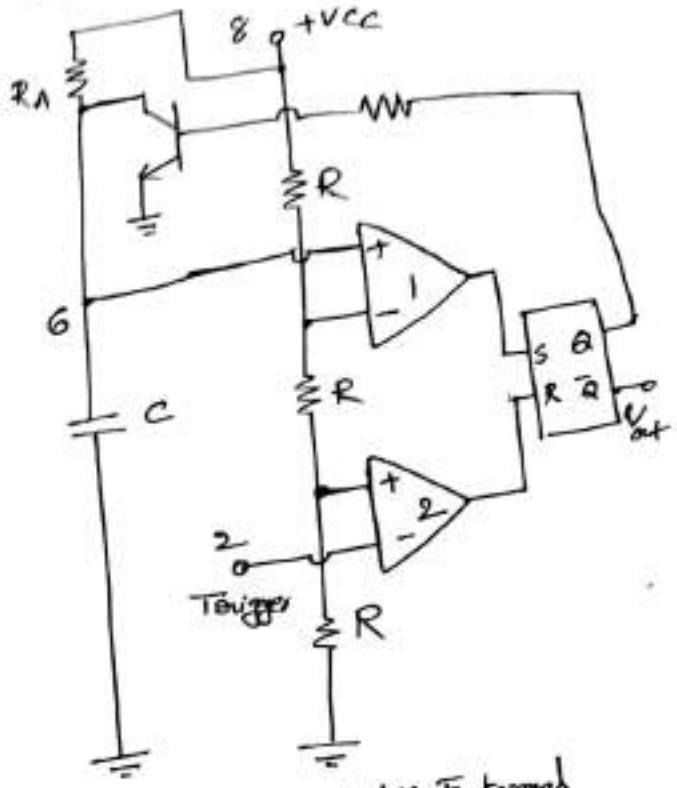
555 Timer As An Astable multivibrator :—

An Astable multi is a free running multivibrator. is a rectangular wave generator.
It doesnot require any External trigger signal. to Change the state of output. hence the name free - running

555 Timer As a Monostable Multivibrator



Circuitary of the Timer 555 as a Monostable Multivibrator



Internal Circuitary With External Connections.

→ Pin 1 is grounded.

→ Trigger input is applied to pin 2

→ The output of this pin is kept In quiescent Condition of output of this input is kept at +VCC

→ To obtain a transistion from stable output state to Quasi stable state, a negative going pulse of narrow width and a amplitude of greater than $\frac{2}{3}$ Vcc is applied to pin 2.

→ Out put is Collected from pin 3

→ pin 4 is Connected to +VCC to avoid accidental reset

Pin 5 is grounded through a 0.01μF to pin 7.
A resistor R_A is connected between pin 6 is shorted to pin 7.
A resistor R_A is connected between pin 6 and 8.
pin 7 is connected with a discharge capacitor
pin 8 is connected to supply Vcc.

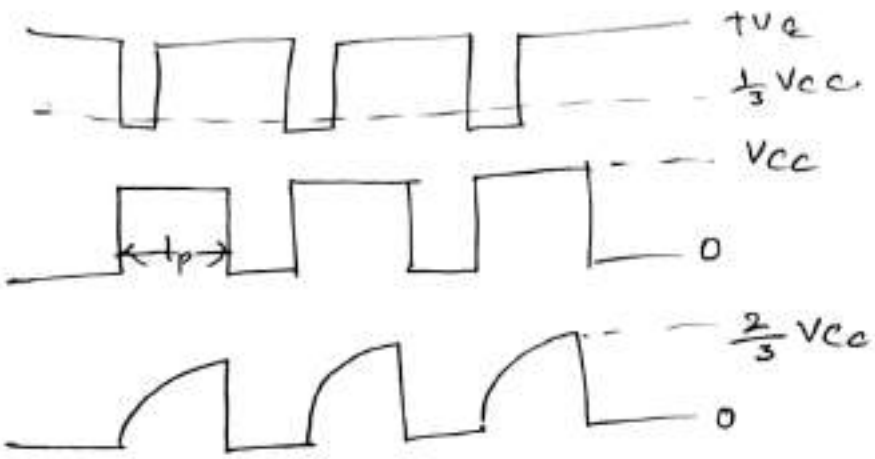
Mono Stable Operation:—

Initially, the output at pin 3 is low, the circuit in a stable state, the transistor is on and the Capacitor C is shorted to ground.
When a negative pulse is applied to pin 2, the trigger input falls below $+\frac{1}{3}$ Vcc, the output of Comparator goes high which resets the flip-flop and consequently the transistor turns off and the output goes high. this is the transistion of the output from stable to quasi stable state.

→ As the discharge transistor is cutoff, the Capacitor begins to charge towards +Vcc through a resistance RA with a time Constant RAC.

→ If the increasing Capacitor voltage greater than $\frac{2}{3}$ Vcc, the O/p of Comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation there by discharging the capacitor and the time O/p goes low. Thus the output returns back to stable state from Quasi state.

Output of MMV remains low until a trigger pulse is applied. Then the cycle repeats.



The time during which the timer output remains high

$$t_p = 1.0986 R_A C$$

Voltage across the capacitor at any instant during charging period

$$v_c = V_{cc}(1 - e^{-t/R_A C})$$

$v_c = \frac{2}{3} V_{cc}$ in the above equation we get the time taken by the capacitor to charge from 0 to $+\frac{2}{3} V_{cc}$

$$\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-t/R_A C}).$$

$$e^{-t/R_A C} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$e^{t/R_A C} = 3.$$

$$\ln e^{t/R_A C} = \ln 3.$$

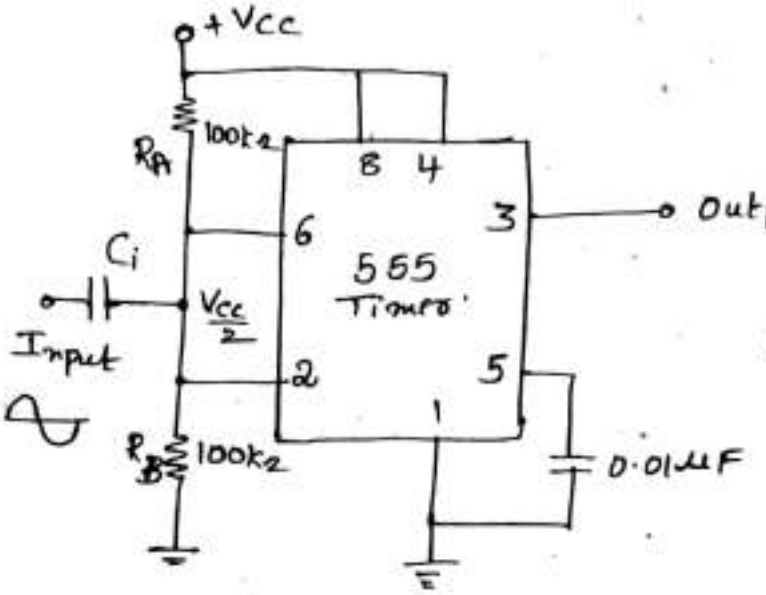
$$\frac{t}{R_A C} \ln e = \ln 3 \Rightarrow \frac{t}{R_A C} = 1.0986$$

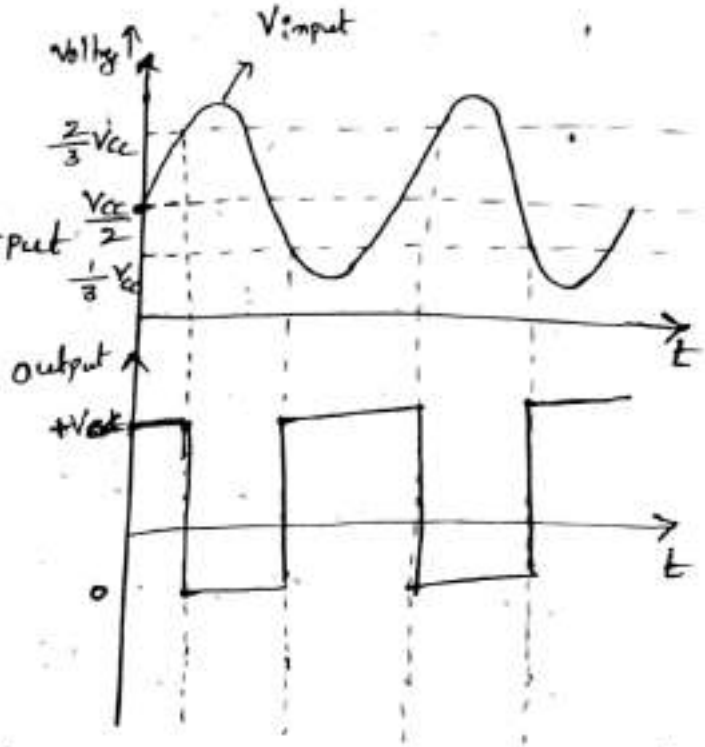
$$t_p = R_A C . \log_e 3 .$$

$$= R_A C . 1.0986 .$$

$$\boxed{t_p = 1.1 R_A C}$$

Schmitt Trigger Design Using 555 Timer:-





→ Schmitt Trigger is a waveshaping circuit that converts any kind of periodically changing A C Signal waveform to a Square wave Signal or pulse wave signal.

→ It is also known as Squaring Circuit. Since its Output is always a Square wave Signal.

→ It is a fast Operating Voltage level detector. When I/p voltage rises above or falls below the Upper threshold voltage Or lower threshold voltage respectively, the output Signal rapidly change from High to Low and vice versa.

→ The Input Signal is applied to pin no. 2 and pin no. 6 through a Coupling Capacitor and O/p is taken from Pin no. 3.

Pin 4 & pin 8 are shorted and connected to $+V_{CC}$.
Here the two internal comparator inputs like non-inverting of comparator 1 i.e, threshold input and inverting input of comparator 2 i.e, Trigger input are tied together and externally biased at $\frac{V_{CC}}{2}$. using the external resistors R_A & R_B
R_A is connected between pin 6 and $+V_{CC}$, R_B is connected between pin 2 & ground.
Pin 5 is grounded through 0.01μF capacitor to avoid noise problems.

Working :-

The input sinusoidal voltage V_{in} is applied commonly to pin 6 & 2 through a capacitor.
The capacitor C is used for isolation of input AC signal & DC signal in the circuit.
The internal comparator 1 changes its output at $\frac{2}{3}V_{CC}$ and comparator 2 changes its output at $\frac{1}{3}V_{CC}$.
The bias provided by R_A & R_B which is $\frac{1}{2}V_{CC}$ lies between these two threshold voltage levels.
Therefore the input sinusoidal wave signal of sufficient amplitude i.e, magnitude must be larger than $\left(\frac{2}{3}V_{CC} - \frac{1}{3}V_{CC}\right)$ i.e, $\frac{1}{6}\cdot V_{CC}$, exceeding the threshold levels, makes the internal flip-flop to alternately set & reset.

The final output of IC 555 timer alternately switches between high state & Low state.

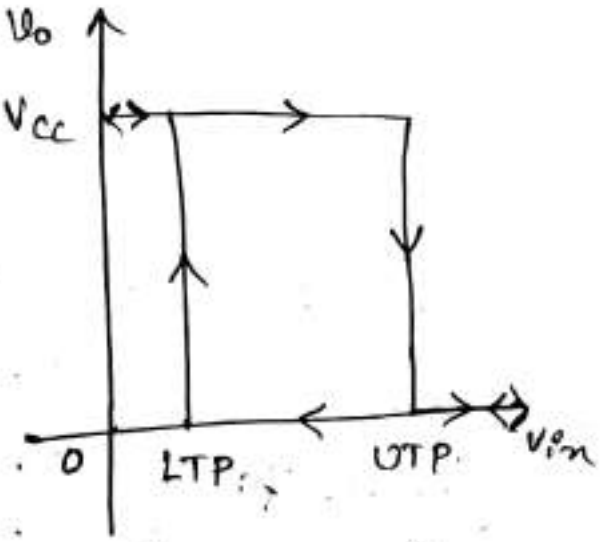
Thus the square wave signal is produced at the output of timer.

The frequency of output square wave signal will be as same the input sinewave signal.

→ As the i/p signal crosses $\frac{2}{3}$ Vcc voltage the output switches from high to low level. again when i/p sine wave signal falls below the $\frac{1}{3}$ Vcc voltage level, the o/p switches from Low to high

→ So At $\frac{2}{3}$ Vcc the o/p switches from high to low state and at $\frac{1}{3}$ Vcc the o/p switches from Low to high state. This is periodically repeated so the i/p sinewave signal is converted into square wave signal at o/p of Schmitt Trigger.

→ It is a graph of o/p voltge versus I/p voltage Vin.



Hysterisis is caused due to two threshold voltage levels

The output triggering points are Hysteresis Curve defined as the two distinct values of input signal voltage at which the output changes the state

→ The Upper Trip point / Triggering point = $\frac{2}{3} V_{cc}$

→ The Lower Triggering point = $\frac{1}{3} V_{CC}$.

→ when the I/p signal exceeds UTP i.e $\frac{2}{3} V_{cc}$, O/p signal switches from high voltage level to low voltage level

→ The o/p remains in low state until the input signal falls below the LTP = $\frac{1}{3} V_{cc}$.

→ The difference between the triggering point is the Hysterisis voltage ~~or~~ the lagging of lower threshold voltage from Upper threshold voltage is known as Hysterisis

→ It is given as $V_H = UTP - LTP$

$= \frac{2}{3} V_{CC} - \frac{1}{3} V_{CC}$

$= \frac{1}{3} V_{cc}$ volt

→ V_H is the dead zone of the Schmitt Trigger fantasy as long as the ~~o~~/p signal within the range of ~~hysteresis~~ ($\frac{2}{3}$ to $\frac{1}{3}$ Vcc) O/p of schmitt Trigger will not change, where the ~~o~~/p signal goes in dead zone the O/p of schmitt trigger switches from high to low state and Lowstate to high state

→ This hysteresis is desirable in schmitt Trigger bcoz it prevents noise signal from causing false Triggering.