Unit-2

Transistor Biasing.

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Unit-2

Transistor Biasing

1. BJTs: Transistor Configurations:

Introduction to BJTs:

Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers Since that the name is given as bipolar.
It is used in amplifiers and oscillator circuits and as a switch in digital circuits.

Applications of BJT's:

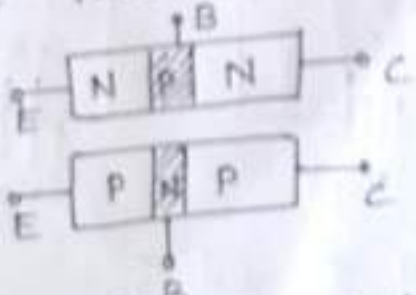
1. Computers
2. Satellites
3. Modern Communication systems.

Types of BJT's:

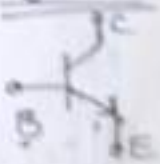
BJT's consists of a silicon or germanium crystal in which a thin layer of N-type or P-type is sandwitched between two layers of P-type or N-type.

Two types of transistors

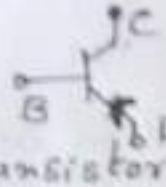
1. NPN →
2. PNP →



Symbols



NPN



PNP

Three terminals available on each transistor they are 1. Emitter, 2. Base and 3. Collector.

The arrow on the Emitter specifies the direction of current flow.

→ Emitter is heavily doped so that it can inject the large number of charge carriers into the base.

→ The base is lightly doped and very thin layer. and passes most of the injected carriers from the emitter into the collector

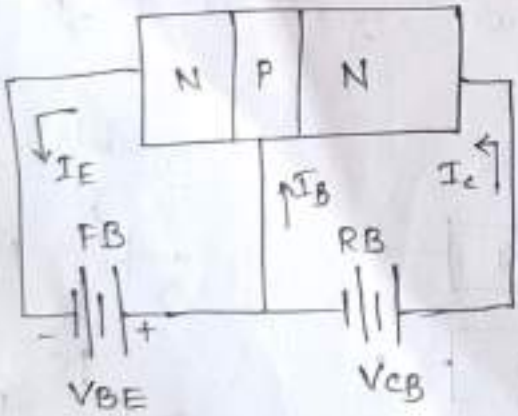
→ The collector is moderately doped occupies large space. and collects the injected carriers from Base.

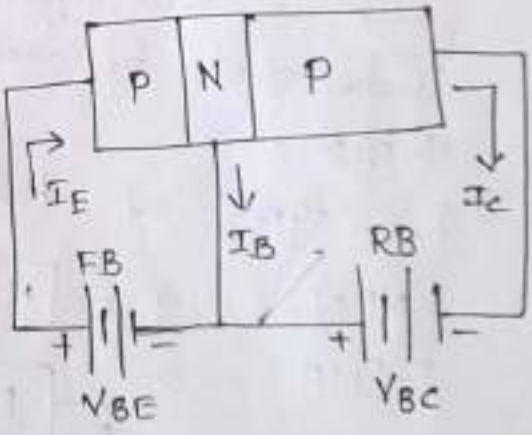
Transistor Biasing:

Generally the Emitter – Base junction is forward biased and Collector – Base junction is reverse biased.

Due to forward bias on Emitter - Base junction an Emitter current flows through the base into the collector.

The Collector – Base junction reverse biased, almost the entire Emitter current flows through the collector





Operation of NPN Transistor:

Applied forward bias at Emitter-base junction causes a lot of electrons from emitter region enter into the base region.

→ As the base is lightly doped with p-type impurities the no of holes in the base region is very small. Hence, a few electrons combine with holes constitute a base current I_B.

→ The remaining electrons cross over into collector region to constitute a collector current I_C.

→ Thus $I_E = -(I_C + I_B)$.

→ In the external circuit of NPN transistor, I_E, I_B and I_C are related by $\boxed{I_E = I_B + I_C}$

Types Of Configurations :—

→ When a transistor is connected in electronic circuits we need to use one terminal as input, the other terminal as output and the third terminal is used as a common terminal in between input and output terminals.

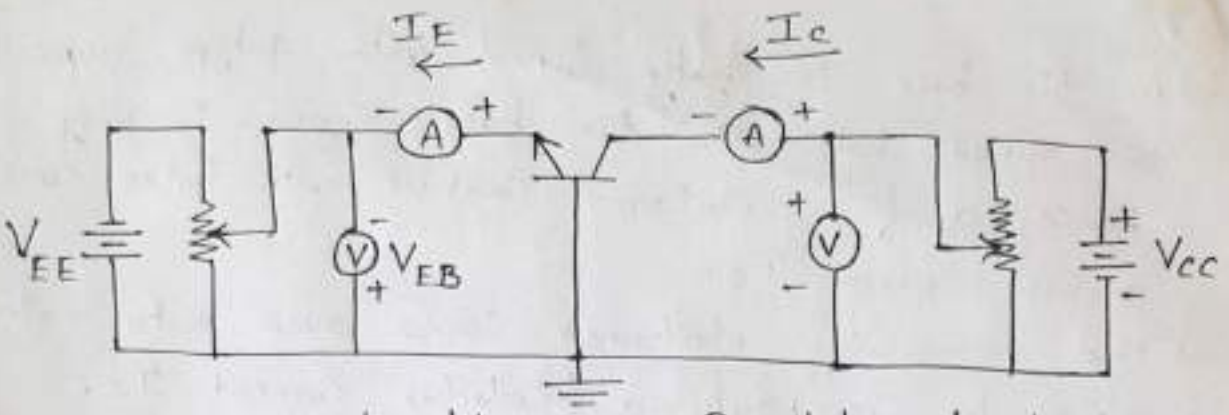
→ Depending on input, output and common terminal a transistor is connected in three configurations They are

1. Common Base Configuration (CB)
2. Common Emitter Configuration (CE)
3. Common Collector Configuration (CC)

Common Base Configuration (CB) :—

This is also called Grounded - Base Configuration.

In this Configuration Emmitter is Input terminal
Collector is Output terminal
Base is Common terminal



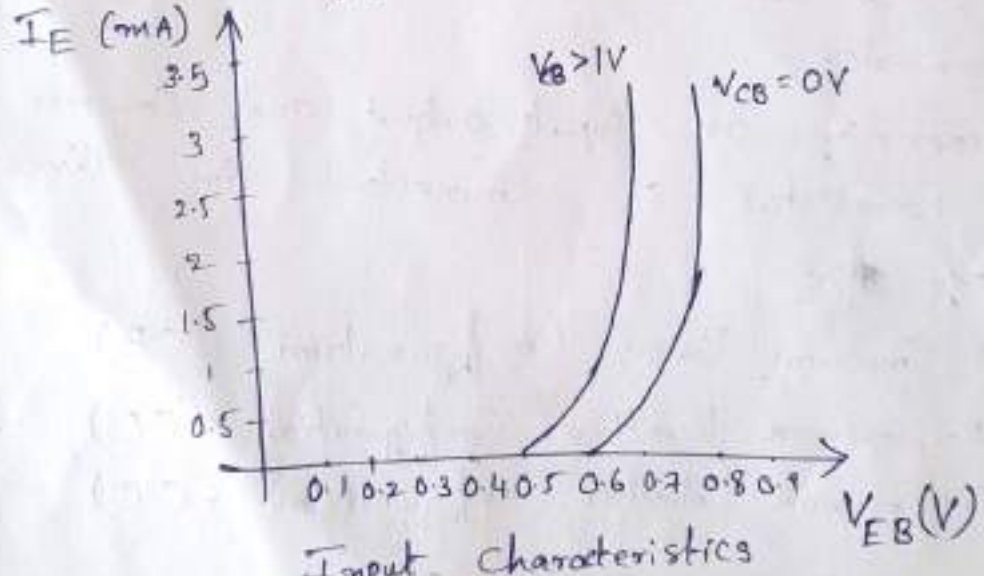
Circuit to determine CB static characteristics

Input Characteristics :—

→ To determine Input characteristics the Collector - base voltage V_{CB} is kept constant at zero and the Emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}.

→ This process is repeated for higher fixed values of V_{CB}.

→ With this method we will obtain the Input characteristics of Common Base Configuration.



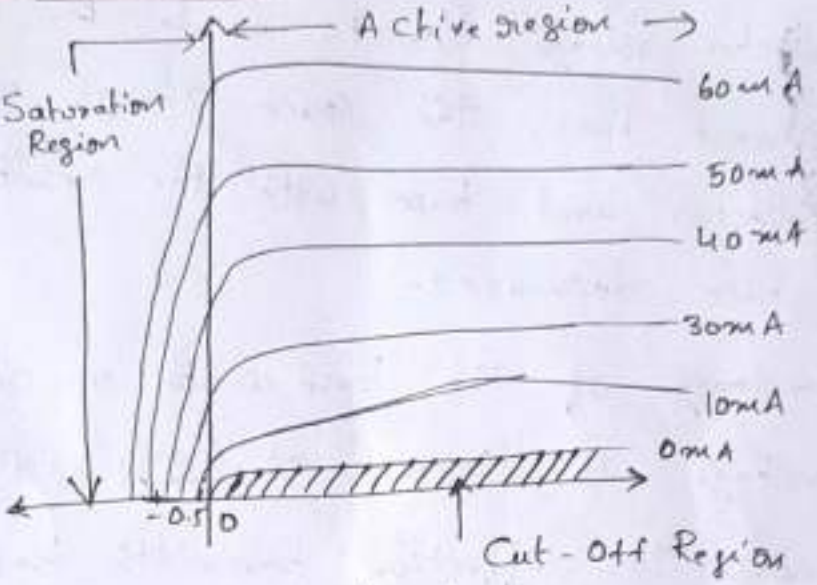
Input Characteristics

→ When V_{CB} = 0 Volt, the Emitter base junction is forward biased so that Emitter Current I_E increases rapidly with small increase in Emitter - Base Voltage (V_{EB}).

When V_{CB} is increased by keeping V_{EB} constant, the width of the base region decreases This result in an increase of I_E.

Therefore the curve shift towards the left as V_{CB} is increased

Output Characteristics:



CB Output Characteristics

→ To determine the output characteristics, the emitter current I_E is kept constant by adjusting the emitter base voltage V_{EB}

→ V_{CB} is increased in equal steps and the collector current I_C is noted for each value of I_E. This is repeated for different fixed values of I_E.

→ At constant value of I_E, I_C is independent of V_{CB} the curves are parallel to the axis of V_{CB}.

→ I_C flows even V_{CB} is equal to zero

→ As the emitter base junction is forward biased the majority carriers i.e, electrons from the emitter

are injected into the base region.
Due to the action of the internal potential barrier at the reverse-biased collector-base junction they flow into the collector region and give rise to I_C even V_{CB} is zero

Early Effect or Base Width modulation:

As the collector voltage V_{CC} is made to increase with the reverse bias, the space charge width increases between collector and base with the result the effective width of base decreases.

This dependency of the base width on collector-to-Emitter voltage is known as Early Effect.

The decrease in effective basewidth has three Consequences:

1. Less chance for recombination with in the base region α increases with V_{CB}.
2. The charge gradient is increases and the majority carriers injected across the emitter junction increases.
3. For extremely large voltages, the effective base width may reduced to zero which causes the voltage breakdown in the transistor.

This phenomenon is called Punch-through or Reach-through.

Transistor Parameters:

Slope of CB characteristics will give four parameters They are commonly known as common-base hybrid parameters or h-parameters.

Input Impedance (h_{ib}):

It is defined as the ratio of change in Emitter voltage to the change in emitter current with the output collector voltage V_{CB} is constant.

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, \quad V_{CB} \text{ Constant}$$

Typical value of h_{ib} range from 20Ω to 50Ω

Output ~~Admittance~~ (h_{ob}):

It is defined as the ratio of change in the collector current to the corresponding change in collector voltage with the emitter current I_E kept constant

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, \quad I_E \text{ Constant}$$

Typical value of h_{ob} is in the order of 0.1 to ~~10 micro mhos~~ 10 μmhos

Forward Current Gain (h_{fb}):

It is defined as the ratio of the change in the collector current to the corresponding change in the emitter current with collector voltage V_{CB} constant. Typical value varies from 0.9 to 1.

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, \quad V_{CB} \text{ Constant}$$

Reverse Voltage gain (h_{rb}):

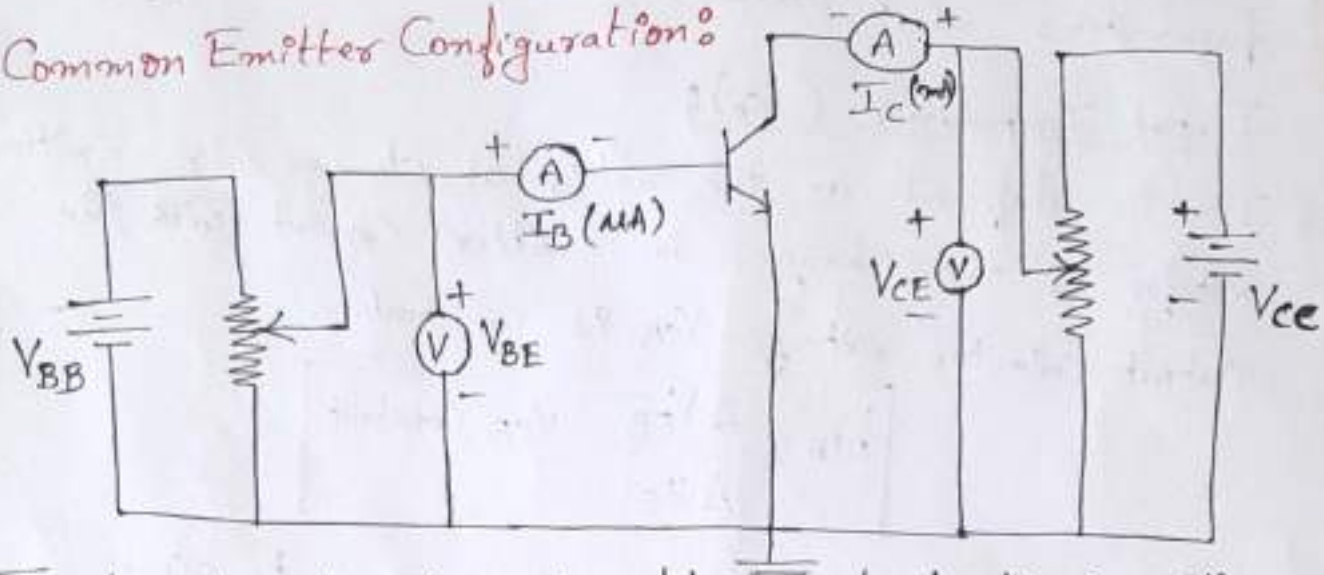
It is defined as the ratio of the change in the emitter voltage and the corresponding change in collector

Voltage with Constant emitter Current I_E. Hence

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ Constant}$$

It's typical value is in the order of 10^{-5} to 10^{-4}.

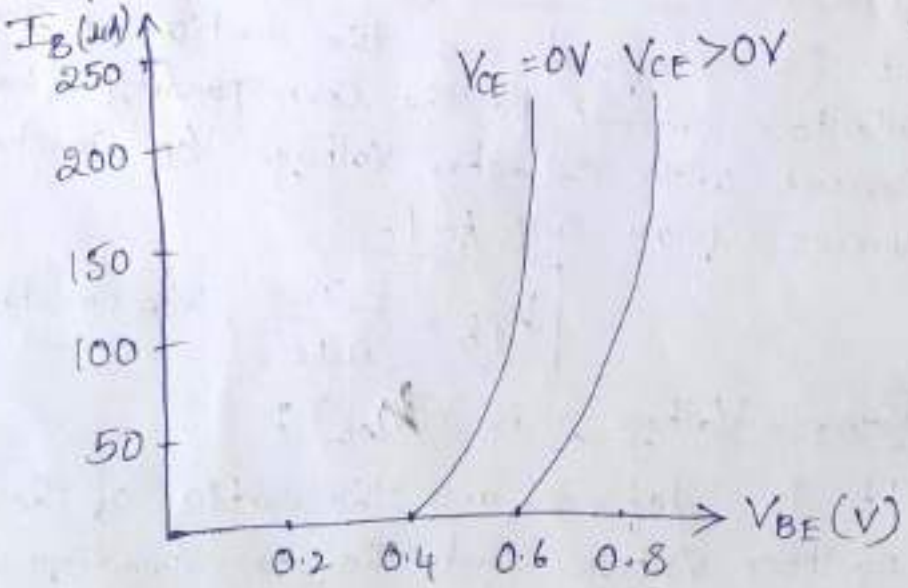
Common Emitter Configuration:



Input characteristics is determined by keeping the Collector to Emitter Voltage constant at Zero volt, and the base Current is increased from Zero & in equal steps by increasing V_{BE}.

For each step of V_{BE} the value of I_B is noted. This procedure is repeated for higher fixed values of V_{CE}.

The Curves of I_B Verses V_{BE} is drawn thus we obtain the input characteristics of CE Configuration.

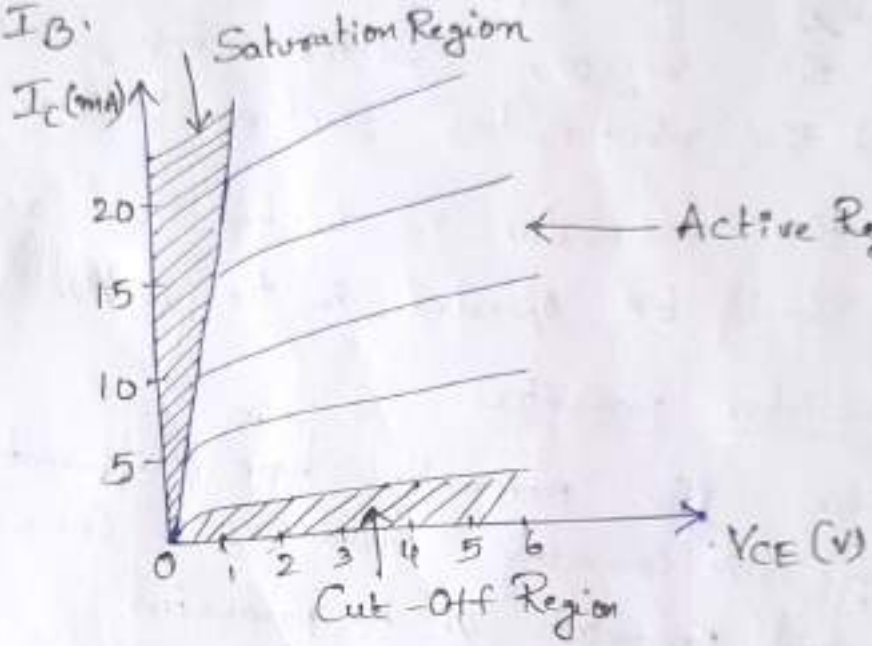


Output Characteristics:-

→ The output characteristics is determined by keeping the base current I_B constant at a suitable value by adjusting the base-emitter voltage V_{BE}.

→ The magnitude of the collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE}.

→ The curves of I_C versus V_{CE} is plotted for different values of I_B.



→ Output characteristics have three regions

1. Saturation region
2. Cutt-off region
3. Active region

→ The region of to the left of characteristics is called Saturation region, in this region both junctions forward biased and an increase in base current does not cause a corresponding large change in I_C.

→ The region below the curve for $I_B = 0$ is called cut-off region. In this region both junctions are reverse biased.

→ If the operating point enter into cutoff region, the transistor is OFF.

→ In this region, the collector current is zero and the collector voltage almost equals to V_{cc}

→ The central region where the curves are uniform in spacing and slope is called the active region. In this region, Emitter base junction is forward biased and the collector-base junction is reverse biased.

→ If the transistor is to be used as linear amplifier it should be operated in the active region.

Transistor parameters

Since the parameters have different dimensions they are commonly known as, Common-Emitter hybrid parameters or h-parameters

Input Impedance (hie):-

It is defined as the ratio of change in base voltage to the base current with collector voltage constant. Typical value ranges from 500 to 2000Ω.

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{Constant}}$$

Output Admittance (hoe):-

It is defined as the ratio of change in the output collector current to the corresponding change in

Collector voltage with the base current I_B kept constant

$$\therefore h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, \quad I_B \text{ Constant}$$

The typical value of the parameter is in the order of 0.1 to 10 μ mhos.

Forward Current gain (h_{fe}) :-

It is defined as the ratio of change in collector current to the corresponding change in the base current keeping the collector voltage V_{CE} constant. Hence.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, \quad V_{CE} \text{ constant}$$

Typical value varies from 20 to 200

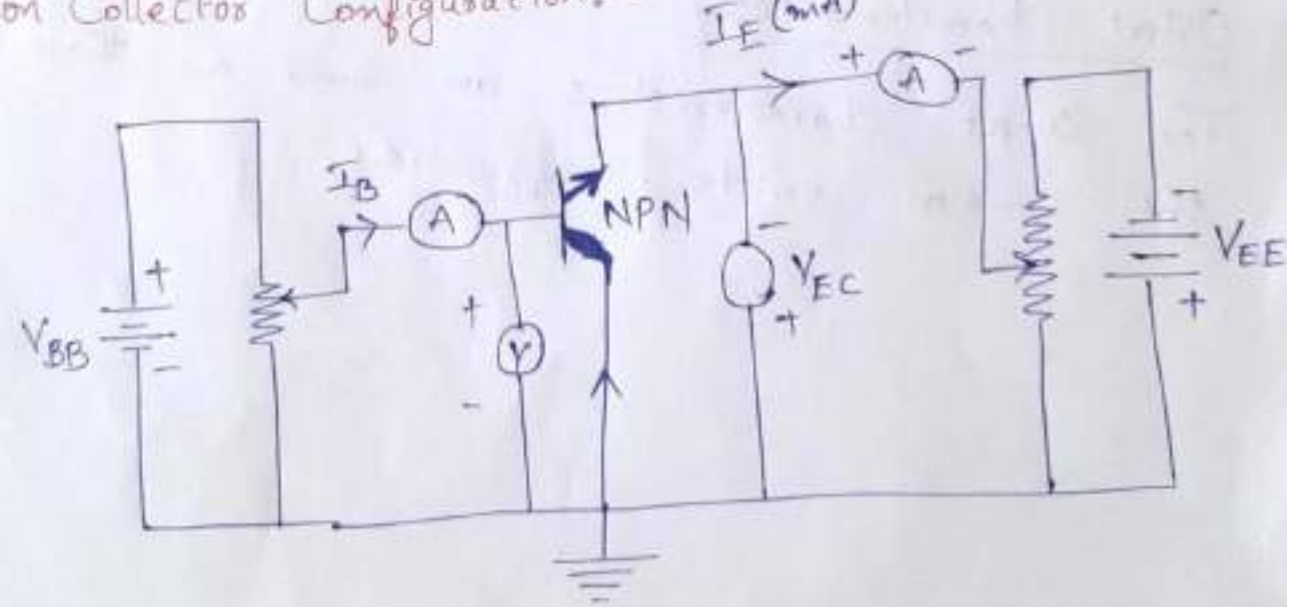
Reverse Voltage gain (h_{re}) :-

It is defined as the ratio of change in the base Voltage and the corresponding change in collector voltage with constant base current I_B. Hence

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, \quad I_B \text{ Constant}$$

It's typical value is in the order of 10^{-5} to 10^{-4}.

Common Collector Configuration :-

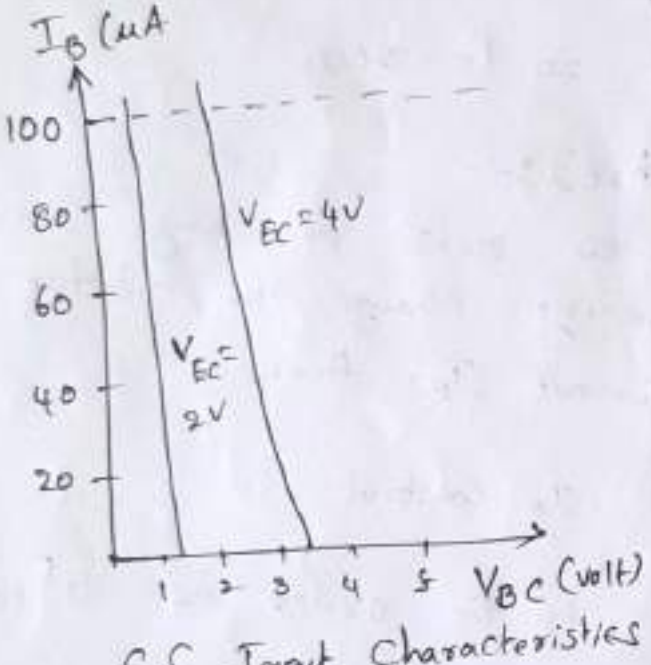


Input Characteristics:-

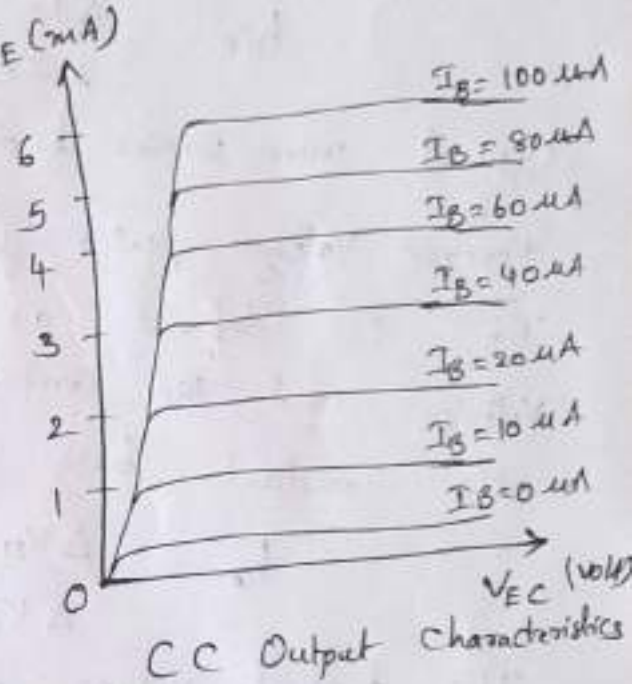
To determine the input characteristics, V_{EC} is kept at a suitable fixed value.

The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for a different fixed values of V_{EC}.

Plots of V_{BC} versus I_B for different values of V_{EC} defines the input characteristics.



CC Input Characteristics



CC Output Characteristics

Output Characteristics:-

The output characteristics are same as those of the common emitter configuration.

Large Signal Current gain: (α)

In a PNP transistor, the magnitudes of the emitter current I_E the base current I_B and the Collector current I_C are related by

$$I_E = -(I_C + I_B)$$

Large Signal Current gain is defined as in Common-Base Configuration is defined as the ratio of the Collector Current to the Emitter Current

$$\alpha = \frac{I_C - I_{CBO}}{I_E - 0} \Rightarrow$$

I_{CBO} → or I_{C_0} → Reverse Saturation Current flowing through reverse biased Collector-base junction. i.e, Collector leakage current with Emitter open.

I_{CBO} is negligible Compared with I_C.

$$\therefore \alpha = \frac{I_C}{I_E}$$

Typical value is in between 0.9 to 0.995.

Relation among I_C, I_B & I_{CBO}

$$I_C = -\alpha I_E + I_{CBO}$$

$$I_C = -\alpha \left[-(I_C + I_B)\right] + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{(1-\alpha)} I_B + \frac{1}{(1-\alpha)} \cdot I_{CBO}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\therefore \boxed{I_C = (1+\beta) I_{CBO} + \beta I_B} \rightarrow (1)$$

Relation ship among I_C, I_B and I_{CEO}

In Common Emitter Configuration I_B is input Current and I_C is the output Current.

If the Base terminal is open, $I_B = 0$ then a small collector Current flows from the collector to Emitter. This is Current is denoted as I_{CEO}, the collector Current with base open.

This is also called Collector to Emitter leakage current.

In CE Configuration, the Emitter-base junction is forward-biased and Collector-base junction is reverse biased hence the collector Current is the Sum of the Emitter Current that reaches Collector and Collector Emitter leakage Current I_{CEO}

$\therefore I_E$ which reaches Collector $= I_C - I_{CEO}$.

Large signal Current gain in Common Emitter Configuration

$$\text{is } \beta = \frac{I_C - I_{CEO}}{I_B}.$$

$$I_C = \beta I_B + I_{CEO} \rightarrow (2)$$

Relation ship between I_{CBO} and I_{CEO}

From the above two equations (1) & (2).

$$I_{CEO} = (1+\beta) I_{CBO}.$$

$I_E = I_C + I_B$ → $I_E = \beta I_B + I_{CEO} + I_B \Rightarrow I_B(1+\beta) + I_{CEO}$

$= (1+\beta) I_{CBO} + (1+\beta) I_C$ ∵ $(I_{CEO}) = (1+\beta) I_{CBO}$

$= \frac{1}{1-\alpha} I_{CBO} + \frac{1}{(1-\alpha)} I_B$ ∵ $\beta = \frac{\alpha}{1-\alpha}$

DC Current Gain β_{dc} or h_{fe} :-

Ratio of Collector Current to the Base Current.

$$\beta_{dc} = h_{fe} = \frac{I_C}{I_B}$$

I_C is >> I_{CEO} Therefore β is approximately equal to h_{fe}

Current Amplification Factor:-

It is the ratio of change in Output Current to the change in input Current is known as amplification factor

In the CB Configuration, the Current amplification factor,

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

In the CE Configuration, the Current amplification factor

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

In CC Configuration, the Current amplification factor

$$\gamma = \frac{\Delta I_E}{\Delta I_B}.$$

Relationship between α and β :-

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\Delta I_C = \alpha \Delta I_E$$

$$\Delta I_E = \alpha \Delta I_E + \Delta I_B$$

$$\Delta I_B = \Delta I_E (1-\alpha).$$

Dividing both sides by ΔI_C, we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1-\alpha).$$

$$\frac{1}{\beta} = \frac{1}{\alpha}(1-\alpha).$$

$$\therefore \boxed{\beta = \frac{\alpha}{(1-\alpha)}}$$

$$\alpha = \frac{\beta}{1+\beta} \quad \text{or} \quad \frac{1}{\alpha} - \frac{1}{\beta} = 1$$

$\alpha \rightarrow$ approaches unit, β approaches infinity CE Configuration is used for almost all transistor application since of it high current gain β.

Relation among α, β and γ:-

I_B is the input Current, I_E is the output Current in Common Collector

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Substituting $\Delta I_B = \Delta I_E - \Delta I_C$

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

dividing numerator and dr on RHS by ΔI_E, we get

$$\gamma = \frac{\Delta I_E / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} = (\beta+1).$$

$$\therefore \boxed{\gamma = \frac{1}{(1-\alpha)} = (\beta+1)}$$

Comparison Of Transistor Configurations:

Property	CB	CE	CC
1. Input resistance	Low (100Ω)	Moderate (750Ω)	High (750 kΩ)
2. Output resistance	High (450kΩ)	Moderate (45kΩ)	Moderate Low (25Ω)
3. Current gain	1	High	High
4. Voltage gain	About 150	About 500	Less than 1
5. phase shift between Input and output Voltages	0 or 360°	180°	0 or 360°
6. Applications	In High frequency Circuits	Audio frequency ckt	Impedance matching

Operating Point :-

Quiescent or Operating point of a transistor amplifier should be established in the active region of its characteristics.

Since the transistor parameters such as β, I_{CO} and V_{BE} are functions of temperature, the operating point shifts with changes in temperature.

To stabilize the operating point different methods of biasing and Compensation techniques are used.

Need for Biasing :-

The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called **Biasing**.

The Circuits used for getting the desired and proper operating point are known as biasing circuits.

- Collector Current of Common Emitter amplifier is

$$I_C = \beta I_B + I_{CEO}$$

$$I_C = \beta I_C + (1+\beta) I_{CO}$$

Here, the three variables β, I_B and I_{CO} increases with temperature.

→ For every 10°C raise in temperature, I_{CO} doubles itself.

→ If I_{CO} increases I_C increase significantly.

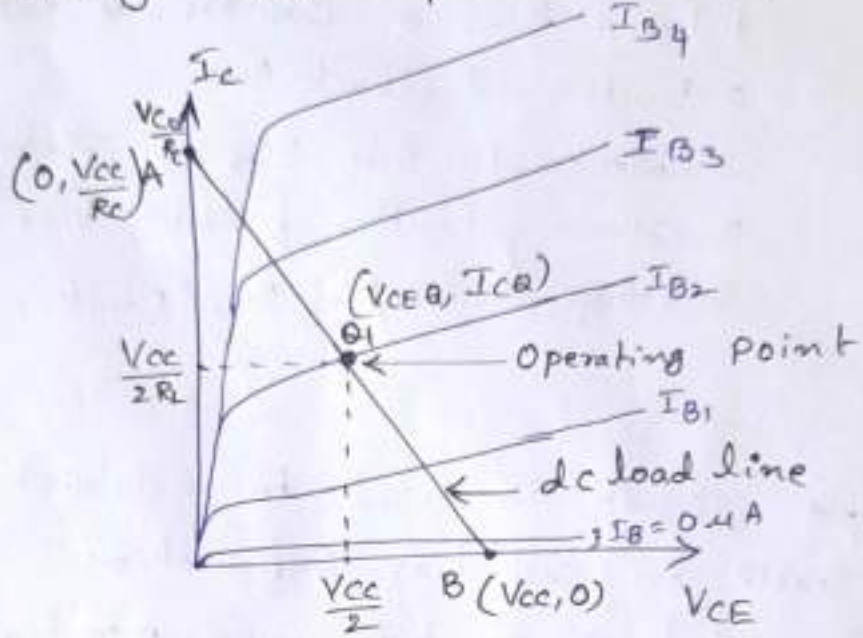
→ This causes power dissipation to increase hence I_{CO} increase further and the process becomes cumulative which leads to thermal runaway that can destroy the transistor.

→ The quiescent operating point can shift due to temperature changes and the transistor is driven into saturation.

→ In addition with temperature, change is Base to Emitter voltage V_{BE} can shift the operating point. Since, $|V_{BE}|$ decreases at the rate of 2.5 mv/°C for increase in temperature

→ Hence the operating point shifts accordingly.

To establish the operating point in the active region with quiescent voltage and current V_{CEQ} and I_{CQ} proper biasing and Compensation techniques are needed



DC load line:-

The straight line AB represents dc load line

The coordinate of the A is obtained with $V_{CE}=0$ and $I_C = \frac{V_{CC}}{RC}$.

The coordinates of the B is obtained with $I_C = 0$ and $V_{CE} = V_{CC}$

The quiescent point Ps located at the mid point of the dc load line to get faithful amplification.

Applying KVL at out put terminal of transistor

$$V_{CC} - I_C R_C - V_{CE} = 0.$$

$$V_{CC} = I_C R_C + V_{CE}$$

A is obtained with $V_{CE} = 0 \Longrightarrow (0, \frac{V_{CC}}{R_C})$

B is obtained with $I_C = 0 \Longrightarrow (V_{CE}, 0)$

Self-Biasing:—

There are some commonly used biasing circuits are available they are.

1. Fixed Bias or Base Resistor method
2. Emitter-Feedback Bias
3. Collector-to-Base Bias or Collector-Feedback bias
4. Collector-Emitter feedback bias
5. Voltage divider / Self Bias / Emitter Bias.

Self-Bias / Voltage divider Bias or Emitter Bias:—

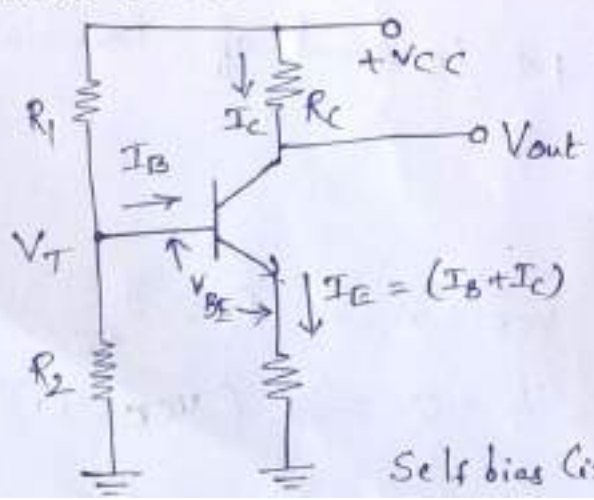
A Simple circuit is used to establish the operating point stable in self-bias configuration.

It is also called emitter bias and potential divider bias.

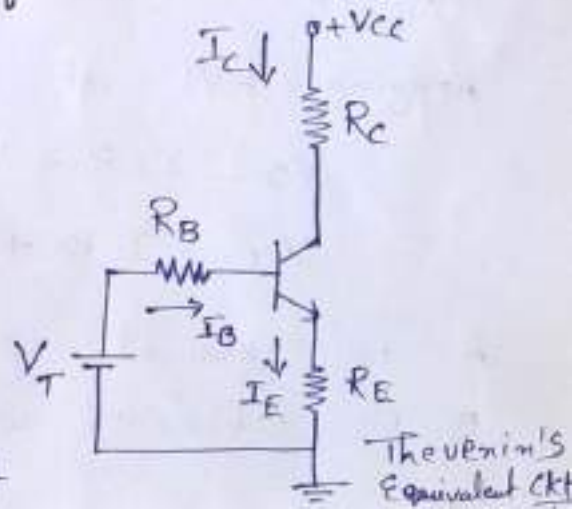
→ A potential divider circuit is used for low collector resistance

→ Emitter resistance R_E causes a voltage drop in the direction to reverse bias the emitter junction.

→ To operate the transistor in active-region the base-Emitter junction is forward biased and it is obtained from the power supply through the potential divider network of the resistances R_1 & R_2



Self bias Circuit



Thevenin's Equivalent ckt

If I_C tends to increase due to increased in I_{CO} with temperature, the current in R_E [I_E] increases.

Hence the drop across R_E increases [V_E] thereby decreasing the base current.

As a result I_C is maintained almost constant inspite of variation is temperature.

Stabilization Factor S :-

It is determind by applying Thevenin's theorem on to the self-bias circuit

$$V_T = \frac{R_2 \cdot V_{CC}}{R_1 + R_2} \quad \text{and} \quad R_B = \frac{R_1 R_2}{R_1 + R_2} \text{ or } R_1 \| R_2$$

Apply the KVL at p/p loop

$$V_T - I_B R_B - V_{BE} - (I_E) \cdot R_E = 0$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) \cdot R_E$$

Differentiate the above equation with respect to I_C we get

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_E + R_B}$$

Stability factor is a measure of Collector Current I_C is stabilized withe varying I_{CO}.

It is defined as the rate of change of Collector Current I_C with respect to the collector - base leakage Current I_{CO}, keeping both β and I_B Constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}}$$, β and I_B Constant

In CE Amplifier

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

Differentiate above equation w.r.to. I_C

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \cdot \frac{dI_{CO}}{dI_C}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = (1+\beta) \times \frac{1}{S}$$

$$\boxed{S = \frac{1+\beta}{1 - \beta \cdot \frac{dI_B}{dI_C}}}$$

Substituting $\frac{dI_B}{dI_C} = \frac{-R_E}{R_E+R_B}$

$$S = \frac{1+\beta}{1 - \beta \cdot \left(\frac{-R_E}{R_E+R_B}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

$$= \frac{(1+\beta)(R_E+R_B)}{R_E+R_B+\beta R_E} = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$

Divide Nr and Dr with R_E

$$= \frac{(1+\beta)\left(1+\frac{R_B}{R_E}\right)}{\frac{R_B}{R_E}+(1+\beta)}$$

$$\boxed{S = (1+\beta) \cdot \left[\frac{\left(1+\frac{R_B}{R_E}\right)}{1+\beta+\frac{R_B}{R_E}}\right]}$$

Thermal runaway :-

The collector current of CE $I_C = \beta I_B + (1+\beta) I_{CO}$

The three variable in the above equation β, I_{CO} and I_B increase with rise in temperature.

The reverse saturation current I_{CO} changes greatly with temperature and doubles for every 10°C rise in temperature.

The increase in collector current I_C causes the collector – base junction temperature to rise inturn increases I_{CO} as a result I_C will increase further.

This process will become cumulative leads to Thermal runaway.

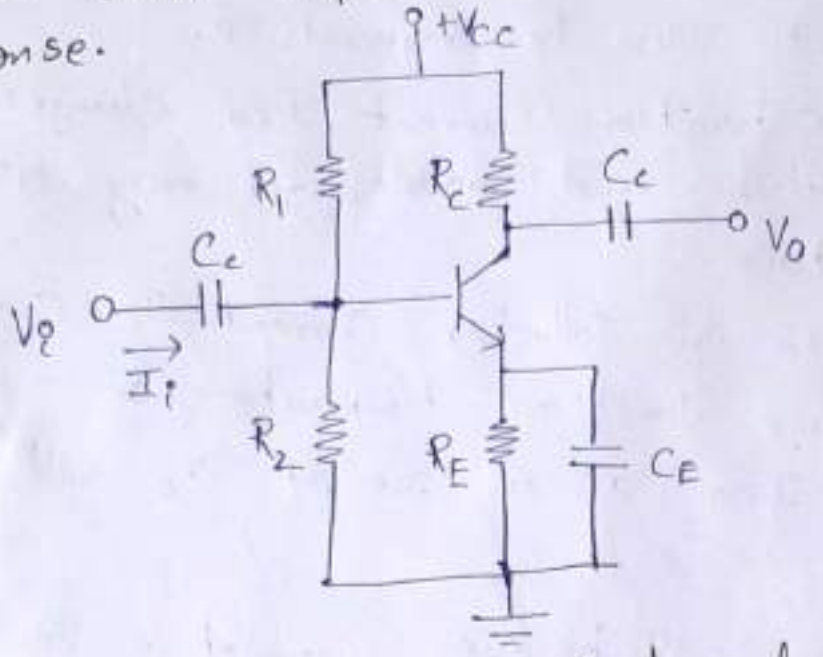
If the ratings of transistor are exceeded which may destroy the transistor itself.

The collector is normally made of larger size than the emitter that helps to dissipate the heat developed at the collector junction.

The circuit is designed in such away that the base current I_B is made to decrease automatically with rise in temperature then the decrease in βI_B will compensate the increase in $(1+\beta) I_{CO}$ that keeps I_C almost constant

RC Coupled amplifier:—

Most Commonly used amplifier is RC Coupled amplifier It is least expensive and has a good frequency response.



→ Here Vcc along with R_1 & R_2 will forward bias the Emitter - base junction and Vcc supply will reverse biase the Collector to base junction

→ This biasing makes the transistor to operate in the active region. This magnitude of the input a c signal V_i always forward bias the emitter - base junction regardless of the polarity of signal.

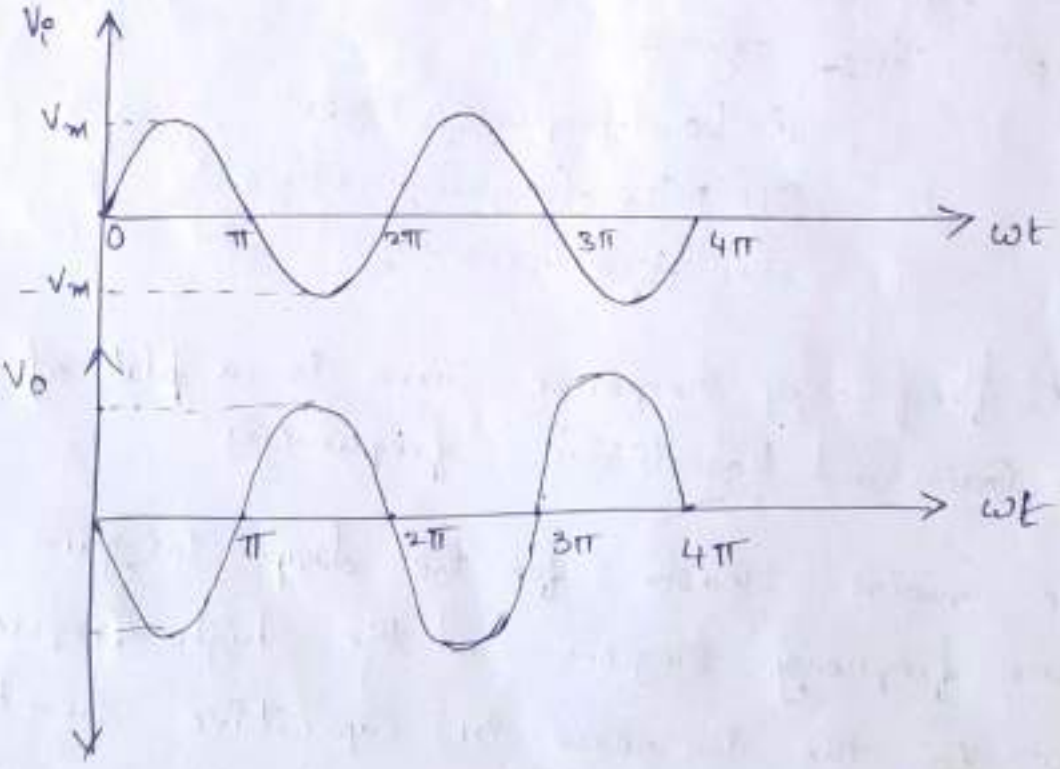
→ During positive half cycle of input, the forward bias across emitter - base junction is increased

→ More number of electrons are injected into the base and reaches the Collector which increases in Collector Current I_C. This increase in collector current produce a greater voltage drop across the load resistance R_L

During negative half cycle of the input signal, the forward bias across the Emitter - base junction is decreased, results in a decrease in Collector Current I_c.
This decrease in Collector Current produces a Smaller voltage drop across the R_c.
Hence a small Change in the input ac signal is CE transistor amplifier produces a large change at the output with a voltage gain around 500 and a phase shift of 180°

Voltage gain the ratio of output voltage to input voltage.

CE transistor Configuration is the widely used in amplifier Circuit due to its high voltage gain



Frequency response of CE Amplifier :-

→ The response of Single stage CE Amplifier is influenced by the frequency of applied Signal.

→ At Low frequencies, the effect of Capacitors Cannot be neglected due to their high value of Capacitive reactance.

→ Under this Condition, the frequency response of the CE amplifier is effected

→ While plotting the frequency response of a Circuit it is Conventional to use a logarithmic Scale along with the X-axis. So as to permit a plot extending from Low to High frequency

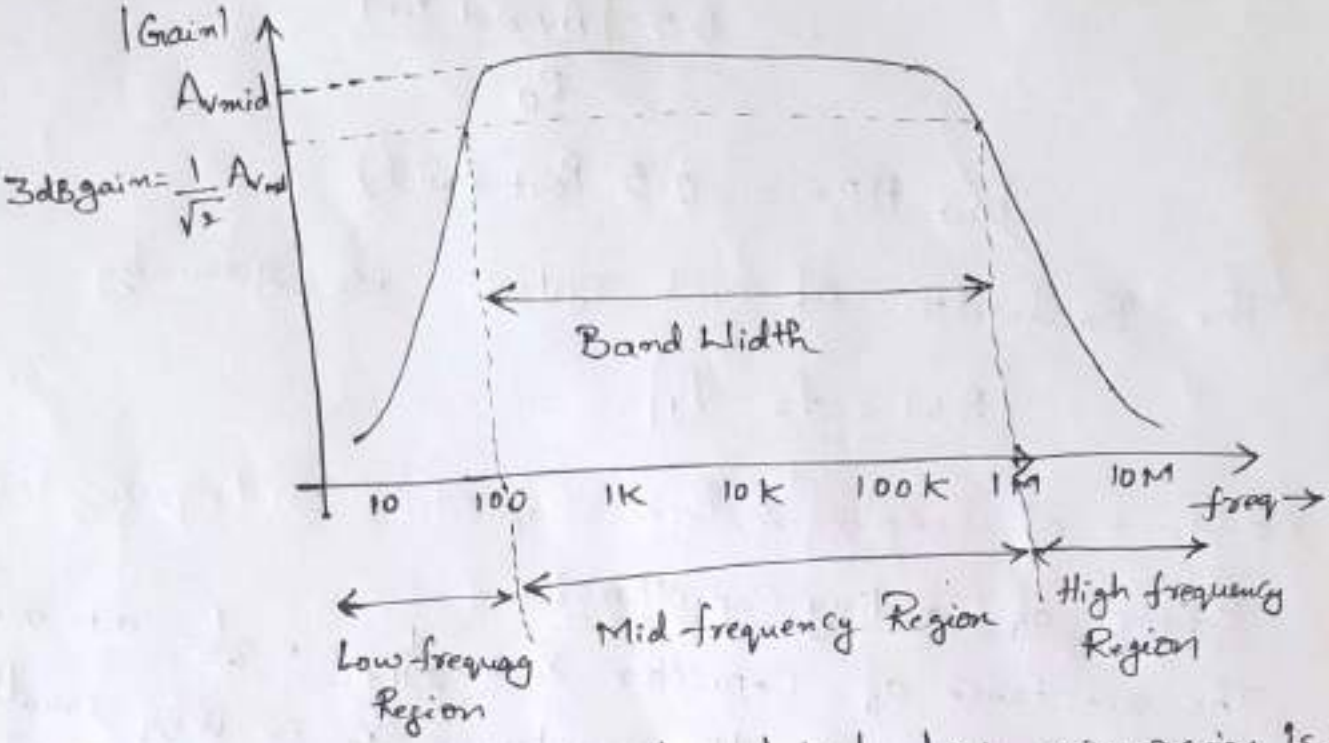
→ In general the frequency response Curve is splitted into three regions.

(i) Low frequency Region
(ii) Mid frequency Region
(iv) Hight frequency Region

→ The frequency response Curve is a plot of magnitude of Gain and Logarithmic frequencies

→ The main reason for the drop in gain at the lower frequency region and the high frequency is due to the increase in Capacitive reactance in the low frequency region and due to parasitic Capacitance elements or the frequency dependence

of network gain on the active device in the high frequency.



→ The frequency boundaries of relatively high gain region is determined by choosing $\frac{1}{\sqrt{2}} A_{V(max)}$ to be the gain at the cut off levels.

→ The frequencies corresponding to such values f_1 & f_2 are called CUTOFF frequencies or Band frequencies or Corner frequencies (or) Half power frequencies.

→ At Cutoff frequencies the output power is half the mid band power output

$$P_{out} = \frac{|V_{out}^2|}{R_O} = \frac{|A_{v\,mid}\ V_{in}|^2}{R_O}$$

$$\because |A_{v\,mid}| = \left|\frac{V_{out}}{V_{in}}\right| \Rightarrow V_{out} = |A_{v\,mid} \cdot V_{in}|$$

→ At half power frequencys f_1 & f_2

$$P_{out\ HPF} = \frac{|0.707\ A_{vmid}\ V_{in}|^2}{R_0}$$

$$= \frac{0.5\ |A_{vmid}\ V_{in}|^2}{R_0}$$

$$P_{out\ HPF} = 0.5\ P_{out\ (mid)}$$

The Bandwidth of each system is given by

$$\boxed{BW = f_2 - f_1}$$

Effect of Coupling & Bypass Capacitors on Frequency Response:

Effect of Coupling Capacitors:

The reactance of Capacitor $X_C = \frac{1}{2\pi fC} = \frac{1}{\omega C}$ at medium & high frequencies, the reactance X_C is very small. so that all coupling Capacitors behave as short circuits. At low frequencies, X_C increases, this increase in X_C drops the signal voltage across the Capacitor and reduces the Circuit gain.

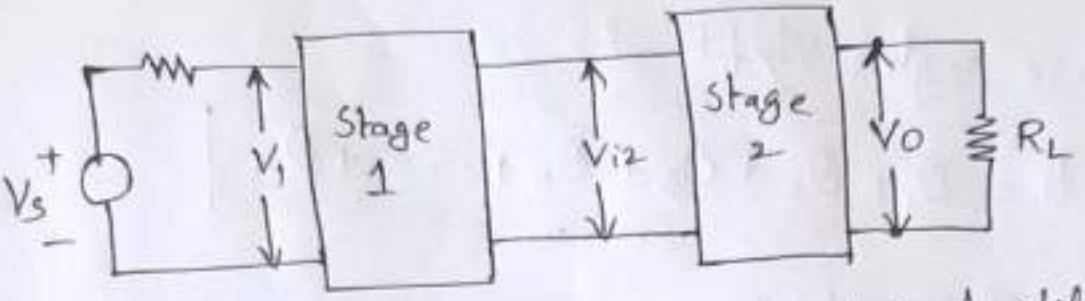
As signal frequencie decrease, the X_C increase and gain continues to fall reducing the output voltage.

Effect of Bypass Capacitors:

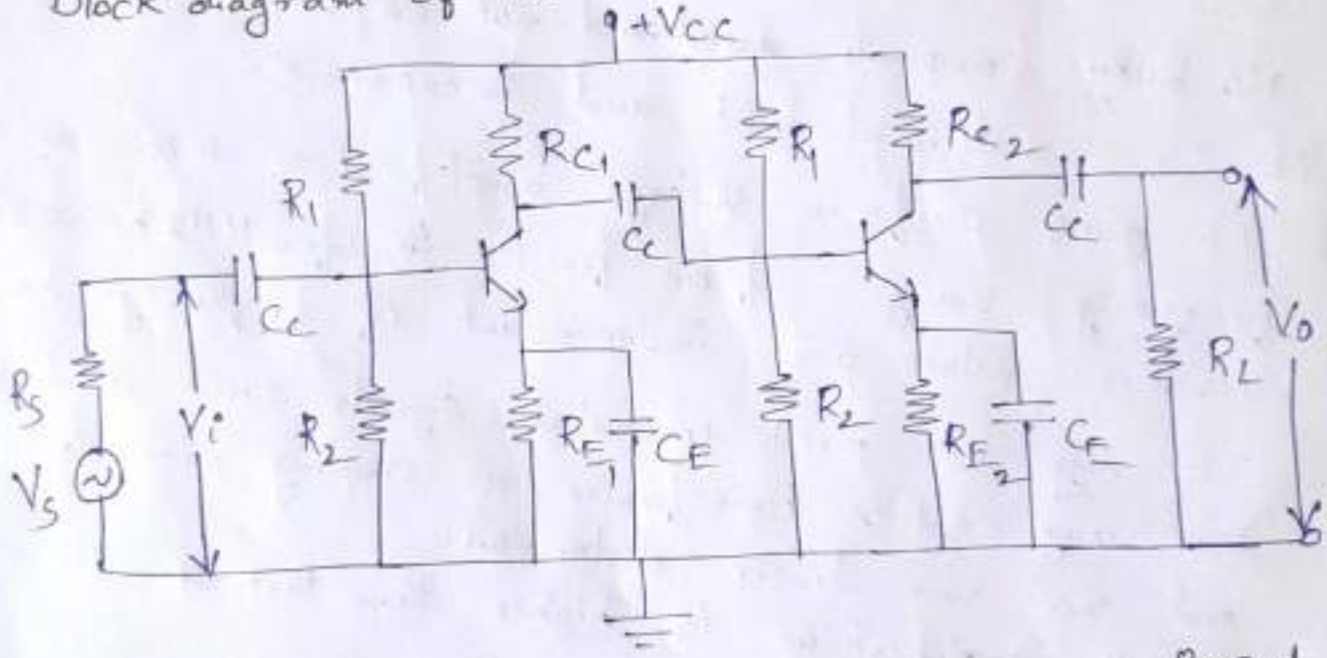
At lower frequencies, the bypass Capacitor C_E is not a short. So the emitter is not at AC ground. X_C is paralled with R_E creates an impedance. The signal drops across the impedance reducing the Circuit Gain.

Two Stage Cascaded Amplifiers :—

Two stage cascaded Amplifier is connected in such away that the output of first stage is connected to the input of the second stage.



Block diagram of the two Cascaded Amplifiers



Assuming $R_{C1} = R_{C2} = R_C$, V_s is the Source input V_i is the input at stage 1, V_{i2} is the o/p of first stage and input of stage 2, V_2 is the o/p of the second stage.

∴ The overall voltage gain $A_V = \frac{V_2}{V_1}$

$$= \frac{V_2}{V_{i2}} \times \frac{V_{i2}}{V_1}$$

$$\boxed{A_V = A_{V_1} \times A_{V_2}}$$

∴ For n stages the overall voltage gain is product of all gains

$$A_{Vn} = A_{V_1} \times A_{V_2} \times A_{V_3} \times A_{V_4} \times \cdots \times A_{V_n}$$

The phase angle shift is

$$\theta = \theta_1 + \theta_2 + \theta_3 + \theta_4 + \cdots + \theta_n$$

Advantages of RC Coupling:-

1. No bulky components used and not expensive. Hence it is small and light and inexpensive.
2. It gives uniform voltage amplification over a wide frequency range from few Hz to few MHz because resistor values are independent of frequency change.
3. It may not pick unwanted signals since it doesn't use any coil or transformer as coupling elements and no non-linear distortion.
4. Overall amplification is higher than that of the other coupling.

Advantage over Single stage:-

1. It's overall amplification is higher
2. Non-linear distortion is less.
3. Frequency response is much better under audiofrequency range.

Application:- These are used as a voltage amplifiers in the initial stages of a public Address System.

Overview Of FET :-

FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence the name Field Effect Transistor.

Current Conduction is only by majority carriers, FET is said to be Unipolar device.

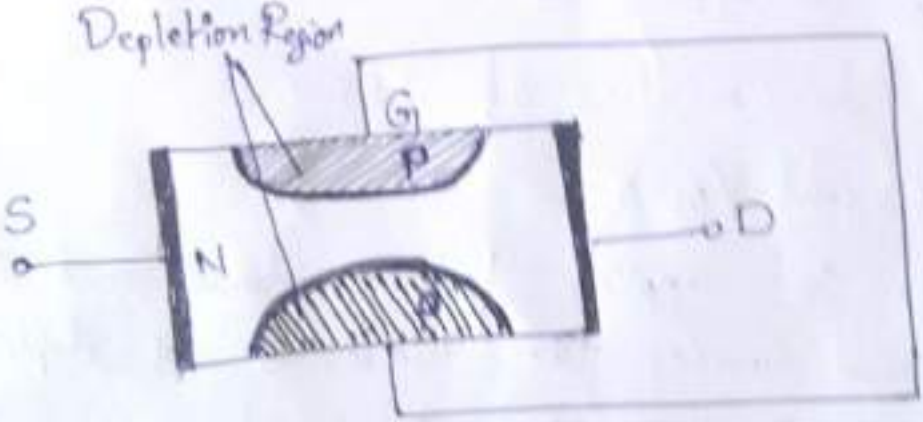
FETs are classified in to two types

1. Junction Field Effect Transistor (JFET)
2. Metal Oxide Semi Conductor FET (MOSFET) or Insulated Gate FET (IGFET)

Depending on the majority carriers, JFET has been classified into two types.

1. N- Channel JFET (Electrons are majority carriers)
2. P- Channel JFET (holes " " ")

Construction Of N- Channel JFET :-



It Consists of a N- type bar which is made of Silicon. Ohmic Contacts are made at the two ends of the bar called as Source and Drain

Source:

It is terminal connected to the negative pole of battery. The majority Carriers (electrons) in N-type bar enter in to the bar through this terminal.

Drain:

This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal

Gate:

Heavily doped P-type silicon is diffused on both sides of the N-type Silicon bar by which a PN junction is formed. These layers are joined together and called Gate G.

Channel:- The region of N-type bar between the depletion region is called the Channel. Majority Carriers move from the source to drain when a potential difference V_{DS} is applied between the source and Drain.

Volt-Ampere Characteristics of JFET:-

When $V_{GS}=0$ and $V_{DS}=0$:-

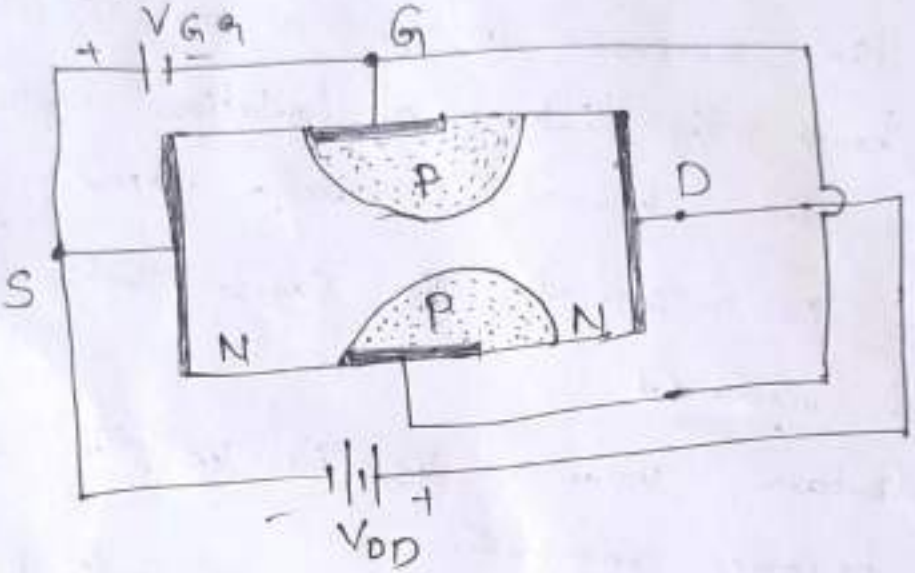
No voltage is applied between drain and Source and gate and source, the thickness of depletion region around the PN Junction is uniform.

When $V_{DS}=0$ and V_{GS} is decreased from zero

In this case, the PN Junction is reverse biased and

the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN Junction is increased and hence the thickness of the depletion region in the channel increases until the two depletion region Contact with each other.

In this Condition, the channel is said to be Cut-off The value of V_{GS} which is required to Cut-off the chanel is called Cut-off voltage



When $V_{GS}=0$ and V_{DS} is increased from Zero:

Drain is positive with respect to the Source with $V_{GS}=0$

The majority Carriers flows through the N-Channel from Source to drain.

The Conventional Current I_D flows from Source to drain

The magnitude of the Current will depend on the following factors.

1. NO. of majority carrier availability
2. Length of the Channel
3. Cross Sectional Area
4. Magnitude of V_{DS}. Where the channel act as a resista

$$R = \frac{\rho l}{A}.$$

$$I_D = \frac{V_{DS}}{R} = \frac{V_{DS}}{\frac{\rho l}{A}} = \frac{A \cdot V_{DS}}{\rho l}$$

$\rho \rightarrow$ Resistivity of the channel.

Since of this resistance of the channel and the applied voltage V_{DS}. there is an increase of potential along the channel from source to drain.

→ Thus the reverse voltage across PN junction increases and hence the thickness of depletion region increases.

→ Therefore the channel is wedge shaped.

→ If V_{DS} is increased, the cross-section area of the channel reduced.

→ At certain value of V_{DS} i.e, V_P the cross-sectional area becomes minimum.

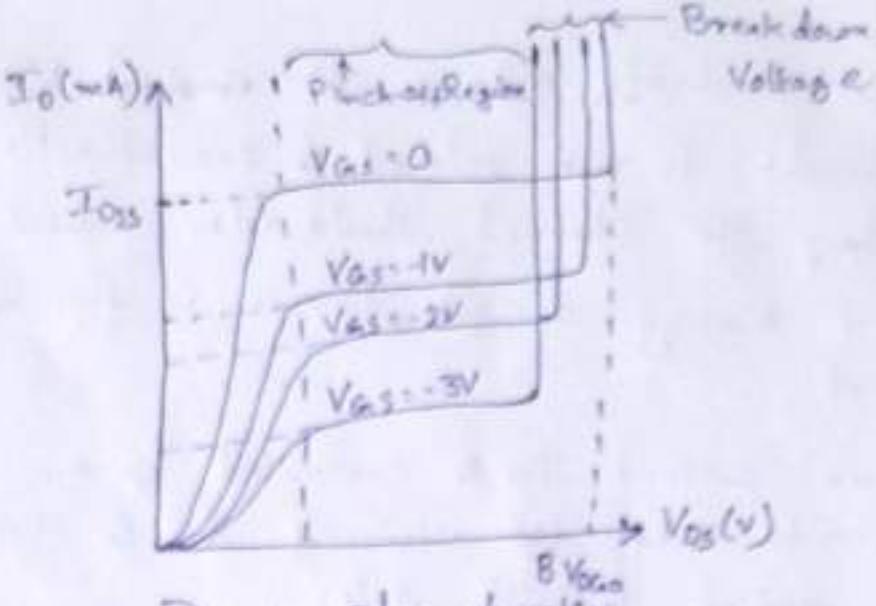
→ At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off Voltage.

→ Decreasing cross sectional area of the channel with increase in V_{DS} result the following

a) V_{DS} is increased from zero, I_D increases ~~along~~ and the rate of increase of I_D with decrease in V_{DS}.

→ The region from $V_{DS} = 0V$ to $V_{DS} = V_P$ is called the Ohmic region.

→ In this region the drain to source resistance = $\frac{V_{DS}}{I_D}$ which depends on V_{GS}. This is used as VVR or VDR. (Voltage Variable Resistor) (Voltage Dependent Resistor)



Drain characteristics

b. If $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off & saturation increases. Hence there is no further increase of I_D.

c. At certain point of voltage, I_D suddenly increases this effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds of the atoms in the depletion region between the gate and the drain.

The drain voltage at which breakdown occurs is denoted by BV_{DGO}.

When V_{GS} is negative and V_{DS} is increased:

If the gate is maintained at a negative voltage less than the negative cut-off voltage, the curve of I_D vs V_{DS} is similar to that for $V_{GS}=0$, but the values of V_P and BV_{DGO} are lower.

→ For the fixed values of V_{DS}, I_D increase with an increase of V_{GS}. Hence a JFET is suitable for use as a voltage amplifier.

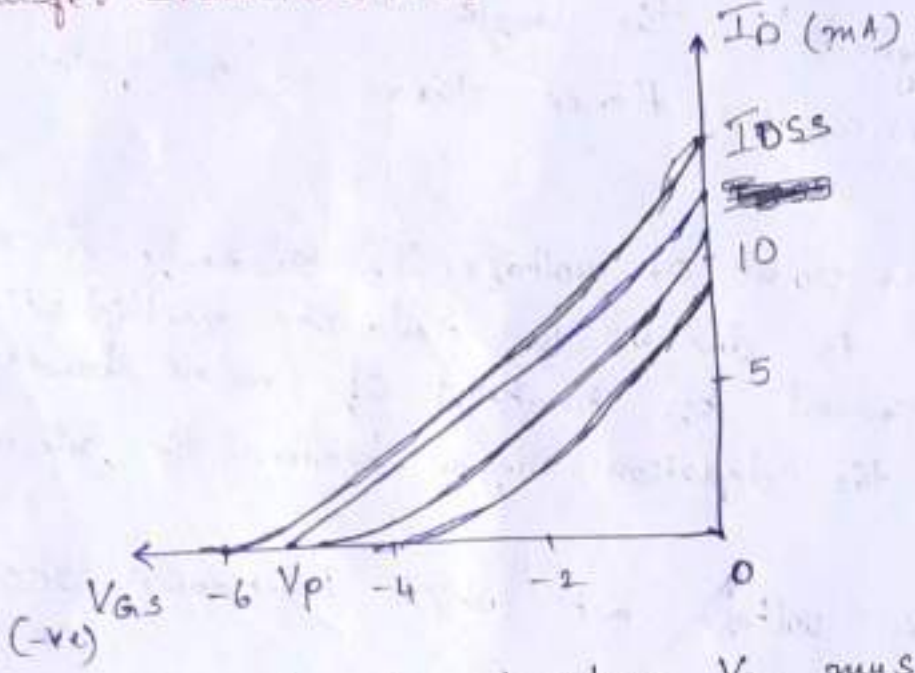
Above the pinch-off voltage at ~~Constant~~ $V_{DS} = V_p$, the drain current is not reduced to zero due to ohmic voltage drop along the channel should also reduced to zero.

The reverse biasing to gate-source is essential for pinch-off the channel.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate.

Hence this device has been given the name Field Effect Transistor

Transfer Characteristics :-



To obtain transfer characteristics V_{DS} must be kept constant with a value greater than the pinch-off voltage V_p.

The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero.

Shape of the transfer characteristics is approximately in the shape of parabola.

Where I_{DSS} is value of saturation drain current with $V_{GS} = 0$ and

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Characteristics parameters of the JFET :—

Drain Current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}.

The relation between the two parameter are determined by the any one of the varaible must be kept fixed.

The relations are determined by the parameters.

* Mutual Conductance or Transconductance g_m.

It is the slope of the transfer characteristic curve and is defined by the ratio of small change in drain current to the corresponding change in gate voltage at constant drain voltage.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS}=\text{Constant}} \quad \text{or} \quad = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{V_{DS}=\text{Constant}}$$

2. Drain resistance, r_d :—

It is the reciprocal of the slope of the drain characteristics.

It is defined as the ratio of small change in the drain voltage to the corresponding small change in the drain current at a constant gate votage.

$$r_d = \frac{\partial V_{DS}}{\partial I_D}\bigg|_{V_{GS}=\text{Constant}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=\text{Constant}}.$$

3. Amplification factor :-

It is defined as the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current.

$$\mu = \left.\frac{\partial V_{DS}}{\partial V_{GS}}\right| I_D = \text{Constant}$$

$$= \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right| I_{DS} = \text{Constant}$$

Relation ship among FET parameters :-

As I_D depends on V_{GS} and V_{DS}

$$I_D = f(V_{DS}, V_{GS})$$

$$\Delta I_D = \frac{\partial I_D}{\partial V_{DS}} \cdot \Delta V_{DS} + \frac{\partial I_D}{\partial V_{GS}} \cdot \Delta V_{GS}$$

Divide the above equation with ΔV_{GS}

$$\frac{\Delta I_D}{\Delta V_{GS}} = \frac{\partial I_D}{\partial V_{DS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \frac{\partial I_D}{\partial V_{GS}}$$

If I_D is constant the $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

$$0 = \frac{\partial I_D}{\partial V_{DS}} \cdot \frac{\Delta V_{DS}}{\Delta V_{GS}} + \frac{\partial I_D}{\partial V_{GS}}$$

$$0 = \frac{1}{r_d}(-\mu) + g_m$$

$$\boxed{\mu = g_m \cdot r_d}$$

FET Amplifiers:-

Common Source Amplifiers:- (CS Amplifier):

Features of FET Amplifiers:

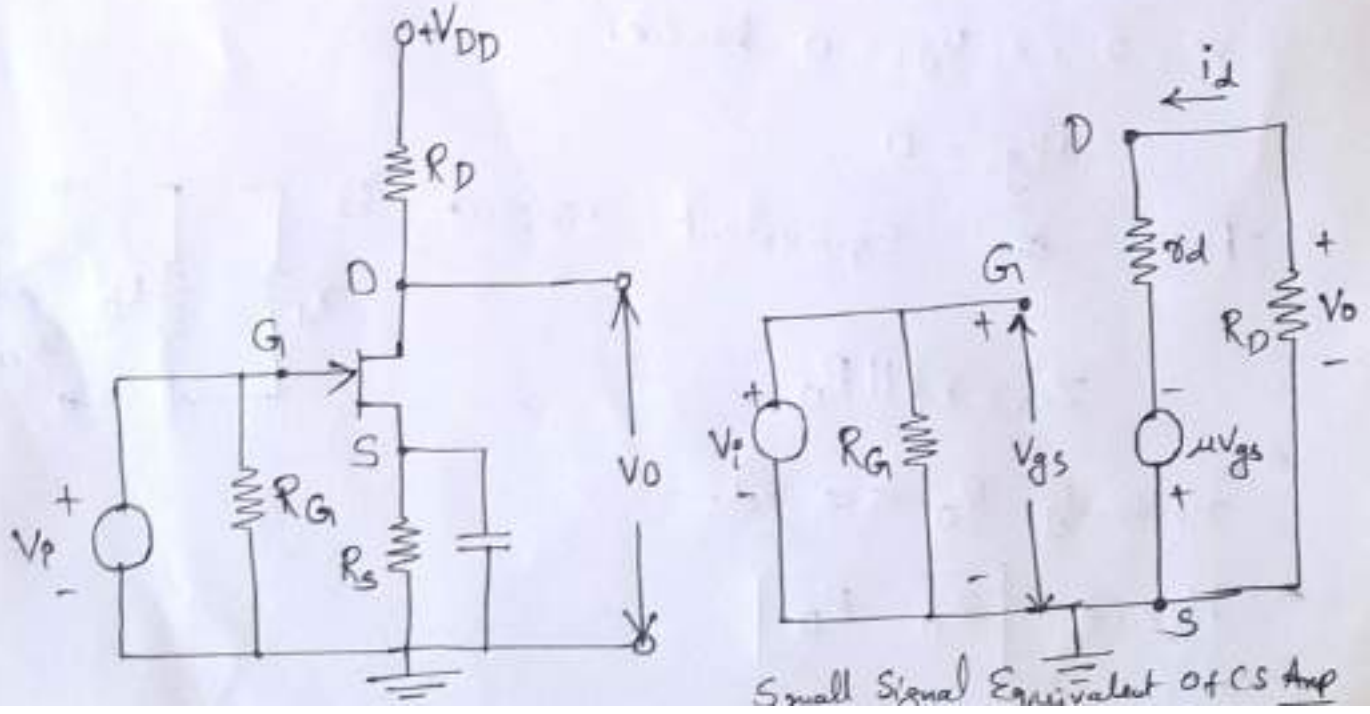
1. FET amplifiers provide an excellent voltage gain with the added features of high input impedance.
2. They have low power consumption with good frequency response.
3. Minimal size and weight.
4. The noise output level is low.

→ These features very useful in an amplifier circuit with small signal amplification.

→ The Common Source is the popular one, provides an inverted and amplified signal.

→ The Common Drain (Source follower) circuit provides Unity gain with no inversion.

Common Source Amplifier (CS) Amplifier:-



Voltage Gain:-

Source resistance R_S is used to set the Q-point

It is bypassed by capacitor C_S for mid-frequency operation

$$V_o = \frac{-R_D}{R_D + r_d} \cdot \mu V_{gs}$$

Where $V_{gs} = V_i$ is the input voltage.

Hence Voltage gain = $\boxed{A_V = \frac{V_o}{V_i} = \frac{-\mu \cdot R_D}{R_D + r_d}}$

Input Impedance:-

It is given by $\boxed{Z_i = R_G}$

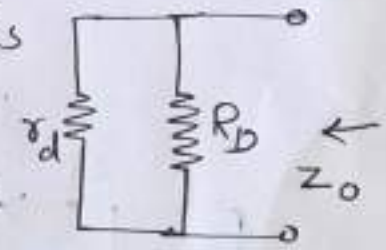
Output Impedance:-

It is measured at the output terminals with input voltage zero. i.e, $V_i = 0$

$V_i = 0$ i.e, $V_{gs} = 0$ hence.

$\mu V_{gs} = 0$

Then the Equivalent circuit is

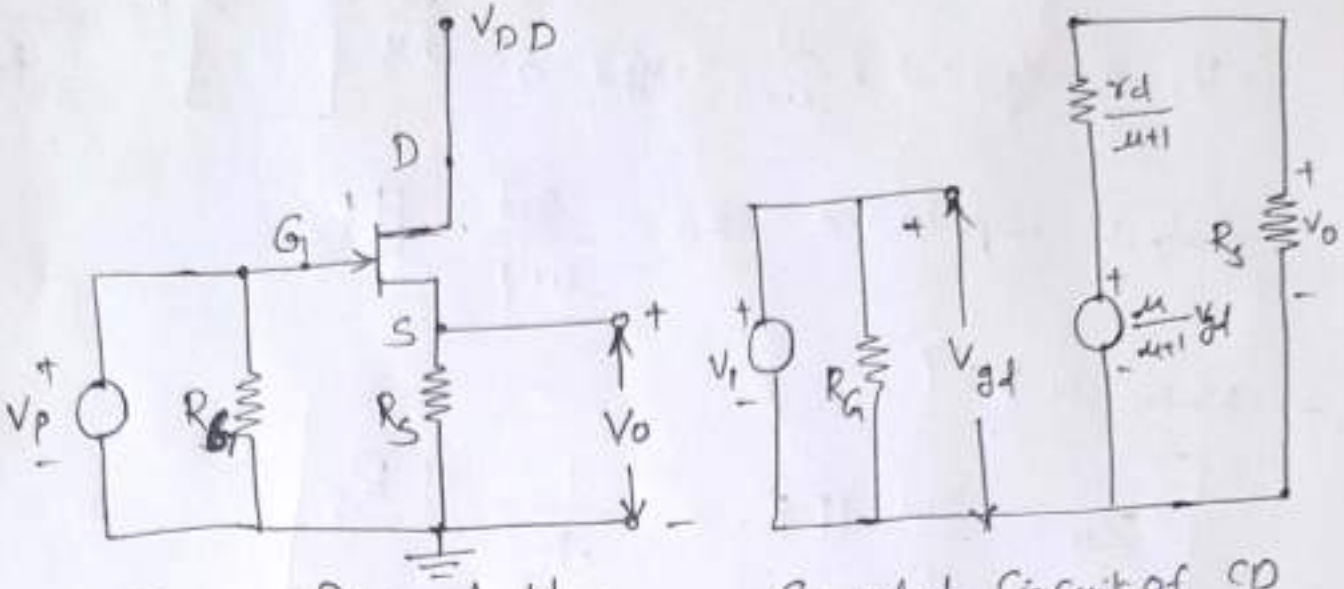


$$Z_o = r_d \,||\, R_D$$

normally $R_D << r_d$.

Hence $\boxed{Z_o = R_D}$

Common Drain Amplifier (CD Amplifier):



a) Common Drain Amplifier

b) Equivalent Circuit of CD Amplifier.

Output voltage $V_o = \dfrac{R_S}{R_S + \frac{r_d}{\mu+1}} \times \dfrac{\mu}{\mu+1} \cdot V_{gd}$

$$= \frac{\mu R_S V_{gd}}{(\mu+1) R_S + r_d}$$

$\because V_{gd} = V_i \Rightarrow$ $\boxed{A_V = \dfrac{V_o}{V_{gd}} = \dfrac{V_o}{V_i} = \dfrac{\mu R_S}{(\mu+1) R_S + r_d}}$

Input Impedance Z_p :-

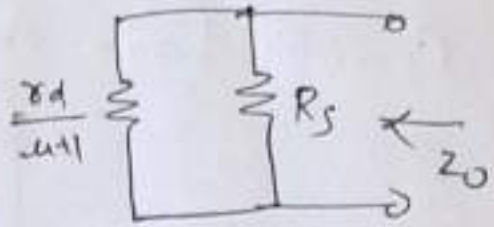
$$Z_p = R_G$$

Output Impedance Z_o :-

It is measured at the o/p terminals with

input voltage $V_i = 0$

$$V_i = 0 = V_{gd} = 0, \quad \frac{\mu}{\mu+1} \cdot V_{gd} = 0$$



Output impedance $z_o = \frac{r_d}{\mu+1} \| R_S$

when $\mu >> 1$

$$Z_o = \frac{r_d}{\mu} \| R_S = \frac{1}{g_m} \| R_S$$