

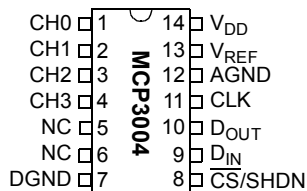
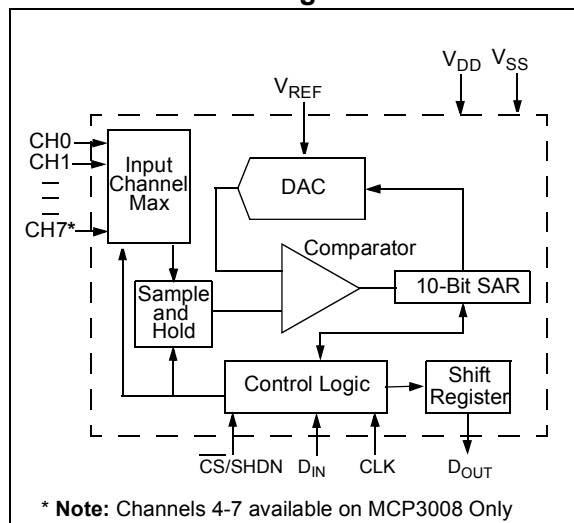
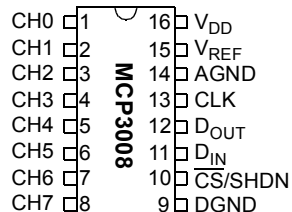


Features

- ### Description

Applications

- ## Package Types

**PDIP, SOIC**

MCP3004/3008

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

V_{DD} 7.0V

All inputs and outputs w.r.t. V_{SS} -0.6V to V_{DD} +0.6V

Storage temperature -65°C to +150°C

Ambient temp. with power applied -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins > 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{DD}	+2.7V to 5.5V Power Supply
DGND	Digital Ground
AGND	Analog Ground
CH0-CH7	Analog Inputs
CLK	Serial Clock
D_{IN}	Serial Data In
D_{OUT}	Serial Data Out
CS/SHDN	Chip Select/Shutdown Input
V_{REF}	Reference Voltage Input

ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, all parameters apply at $V_{DD} = 5V$, $V_{REF} = 5V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$, $f_{SAMPLE} = 200$ kps and $f_{CLK} = 18 \cdot f_{SAMPLE}$. Unless otherwise noted, typical values apply for $V_{DD} = 5V$, $T_{AMB} = 25^{\circ}C$.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Conversion Rate						
Conversion Time	t_{CONV}	—	—	10	clock cycles	
Analog Input Sample Time	t_{SAMPLE}	1.5			clock cycles	
Throughput Rate	f_{SAMPLE}	—	—	200 75	kps kps	$V_{DD} = V_{REF} = 5V$ $V_{DD} = V_{REF} = 2.7V$
DC Accuracy						
Resolution			10		bits	
Integral Nonlinearity	INL	—	± 0.5	± 1	LSB	
Differential Nonlinearity	DNL	—	± 0.25	± 1	LSB	No missing codes over temperature
Offset Error		—	—	± 1.5	LSB	
Gain Error		—	—	± 1.0	LSB	
Dynamic Performance						
Total Harmonic Distortion		—	-76		dB	$V_{IN} = 0.1V$ to $4.9V@1$ kHz
Signal to Noise and Distortion (SINAD)		—	61		dB	$V_{IN} = 0.1V$ to $4.9V@1$ kHz
Spurious Free Dynamic Range		—	78		dB	$V_{IN} = 0.1V$ to $4.9V@1$ kHz
Reference Input						
Voltage Range		0.25	—	V_{DD}	V	Note 2
Current Drain		—	100 0.001	150 3	μA μA	$\overline{CS} = V_{DD} = 5V$

Note 1: This parameter is established by characterization and not 100% tested.

Note 2: See graphs that relate linearity performance to V_{REF} levels.

Note 3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2, "Maintaining Minimum Clock Speed", for more information.

ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, all parameters apply at $V_{DD} = 5V$, $V_{REF} = 5V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$, $f_{SAMPLE} = 200$ kps and $f_{CLK} = 18 \cdot f_{SAMPLE}$. Unless otherwise noted, typical values apply for $V_{DD} = 5V$, $T_{AMB} = 25^{\circ}C$.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Analog Inputs						
Input Voltage Range for CH0 or CH1 in Single-Ended Mode		V_{SS}	—	V_{REF}	V	
Input Voltage Range for IN+ in pseudo-differential mode		IN-	—	$V_{REF} + IN-$		
Input Voltage Range for IN- in pseudo-differential mode		$V_{SS} - 100$	—	$V_{SS} + 100$	mV	
Leakage Current		—	0.001	± 1	μA	
Switch Resistance		—	1000	—	Ω	See Figure 4-1
Sample Capacitor		—	20	—	pF	See Figure 4-1
Digital Input/Output						
Data Coding Format		Straight Binary				
High Level Input Voltage	V_{IH}	$0.7 V_{DD}$	—	—	V	
Low Level Input Voltage	V_{IL}	—	—	$0.3 V_{DD}$	V	
High Level Output Voltage	V_{OH}	4.1	—	—	V	$I_{OH} = -1$ mA, $V_{DD} = 4.5V$
Low Level Output Voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 1$ mA, $V_{DD} = 4.5V$
Input Leakage Current	I_{LI}	-10	—	10	μA	$V_{IN} = V_{SS}$ or V_{DD}
Output Leakage Current	I_{LO}	-10	—	10	μA	$V_{OUT} = V_{SS}$ or V_{DD}
Pin Capacitance (All Inputs/Outputs)	C_{IN} , C_{OUT}	—	—	10	pF	$V_{DD} = 5.0V$ (Note 1) $T_{AMB} = 25^{\circ}C$, $f = 1$ MHz
Timing Parameters						
Clock Frequency	f_{CLK}	—	—	3.6 1.35	MHz MHz	$V_{DD} = 5V$ (Note 3) $V_{DD} = 2.7V$ (Note 3)
Clock High Time	t_{HI}	125	—	—	ns	
Clock Low Time	t_{LO}	125	—	—	ns	
\overline{CS} Fall To First Rising CLK Edge	t_{SUCS}	100	—	—	ns	
\overline{CS} Fall To Falling CLK Edge	t_{CSD}	—	—	0	ns	
Data Input Setup Time	t_{SU}	—	—	50	ns	
Data Input Hold Time	t_{HD}	—	—	50	ns	
CLK Fall To Output Data Valid	t_{DO}	—	—	125 200	ns ns	$V_{DD} = 5V$, See Figure 1-2 $V_{DD} = 2.7V$, See Figure 1-2
CLK Fall To Output Enable	t_{EN}	—	—	125 200	ns ns	$V_{DD} = 5V$, See Figure 1-2 $V_{DD} = 2.7V$, See Figure 1-2
\overline{CS} Rise To Output Disable	t_{DIS}	—	—	100	ns	See Test Circuits, Figure 1-2
\overline{CS} Disable Time	t_{CSH}	270	—	—	ns	
D_{OUT} Rise Time	t_R	—	—	100	ns	See Test Circuits, Figure 1-2 (Note 1)
D_{OUT} Fall Time	t_F	—	—	100	ns	See Test Circuits, Figure 1-2 (Note 1)

Note 1: This parameter is established by characterization and not 100% tested.

2: See graphs that relate linearity performance to V_{REF} levels.

3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2, "Maintaining Minimum Clock Speed", for more information.

MCP3004/3008

ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, all parameters apply at $V_{DD} = 5V$, $V_{REF} = 5V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$, $f_{SAMPLE} = 200$ kps and $f_{CLK} = 18 \cdot f_{SAMPLE}$. Unless otherwise noted, typical values apply for $V_{DD} = 5V$, $T_{AMB} = 25^{\circ}C$.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	—	425 225	550	μA	$V_{DD} = V_{REF} = 5V$, D_{OUT} unloaded $V_{DD} = V_{REF} = 2.7V$, D_{OUT} unloaded
Standby Current	I_{DSS}	—	0.005	2	μA	$\overline{CS} = V_{DD} = 5.0V$
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	$^{\circ}C$	
Operating Temperature Range	T_A	-40	—	+85	$^{\circ}C$	
Storage Temperature Range	T_A	-65	—	+150	$^{\circ}C$	
Thermal Package Resistance						
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	$^{\circ}C/W$	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	108	—	$^{\circ}C/W$	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	$^{\circ}C/W$	
Thermal Resistance, 16L-PDIP	θ_{JA}	—	70	—	$^{\circ}C/W$	
Thermal Resistance, 16L-SOIC	θ_{JA}	—	90	—	$^{\circ}C/W$	

- Note 1:** This parameter is established by characterization and not 100% tested.
Note 2: See graphs that relate linearity performance to V_{REF} levels.
Note 3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2, "Maintaining Minimum Clock Speed", for more information.

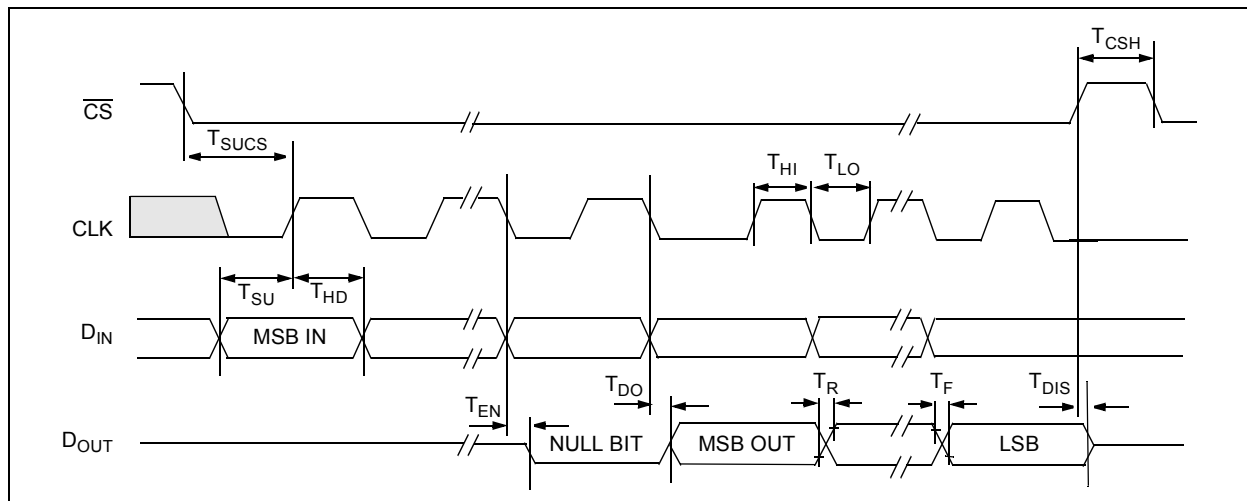


FIGURE 1-1: Serial Interface Timing.

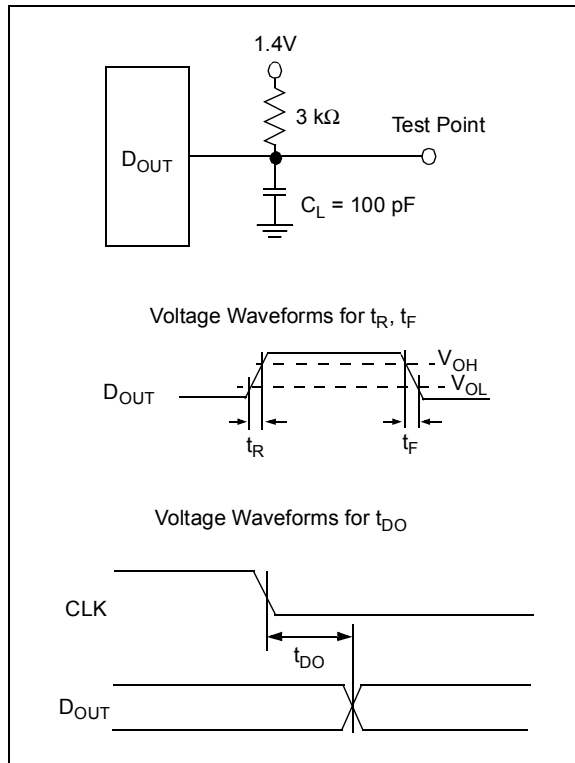


FIGURE 1-2: Load Circuit for t_R , t_F , t_{DO} .

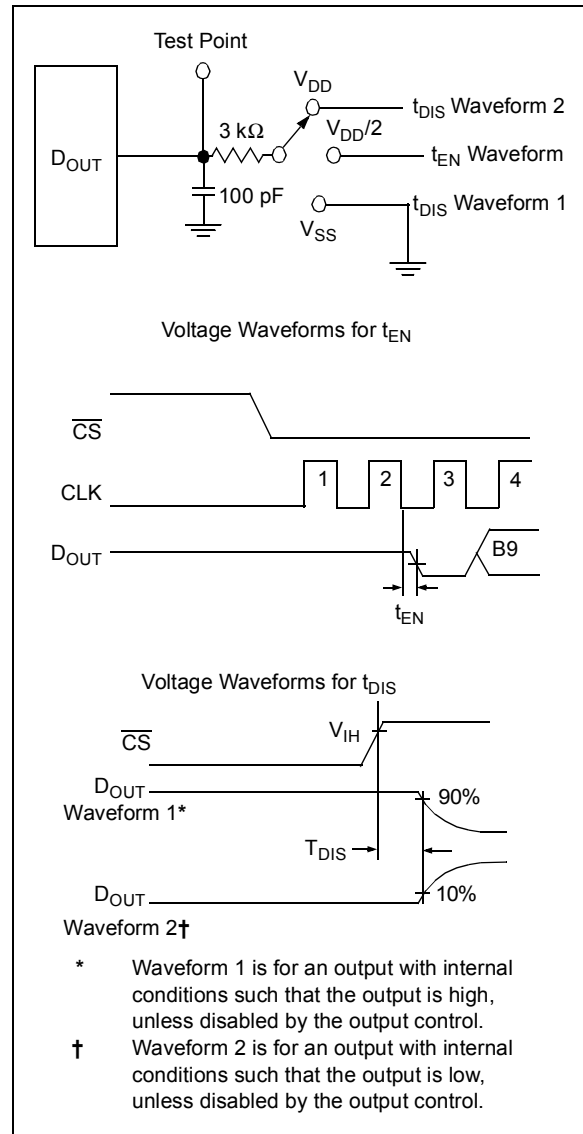


FIGURE 1-3: Load circuit for t_{DIS} and t_{EN} .

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $f_{CLK} = 18 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

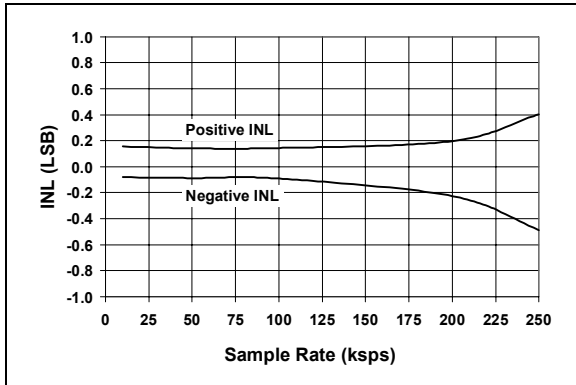


FIGURE 2-1: Integral Nonlinearity (INL) vs. Sample Rate.

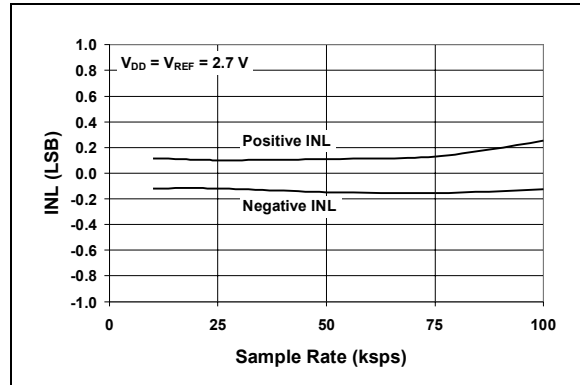


FIGURE 2-4: Integral Nonlinearity (INL) vs. Sample Rate ($V_{DD} = 2.7V$).

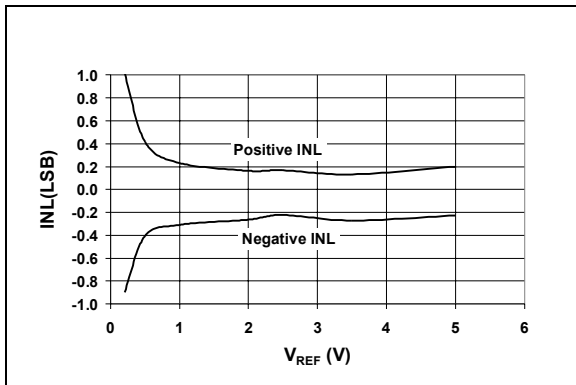


FIGURE 2-2: Integral Nonlinearity (INL) vs. V_{REF}

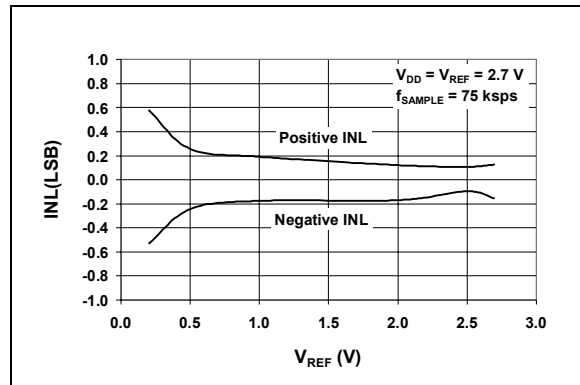


FIGURE 2-5: Integral Nonlinearity (INL) vs. V_{REF} ($V_{DD} = 2.7V$).

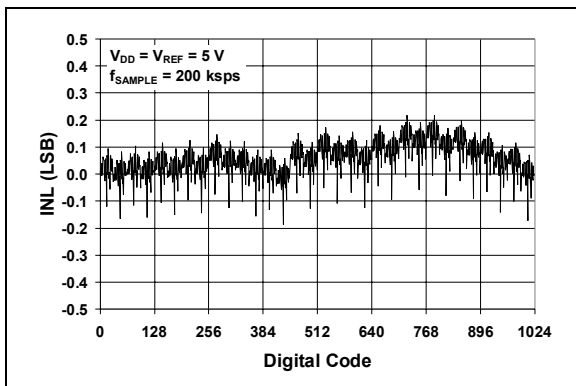


FIGURE 2-3: Integral Nonlinearity (INL) vs. Code (Representative Part).

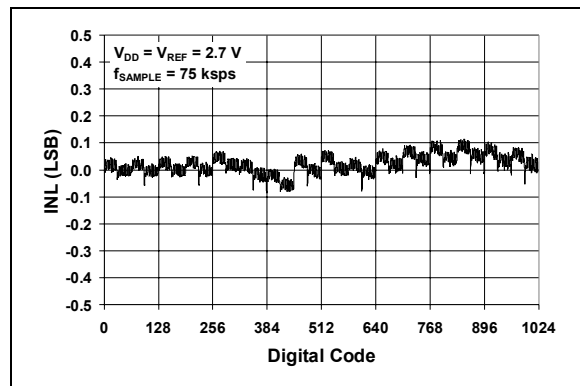


FIGURE 2-6: Integral Nonlinearity (INL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $f_{CLK} = 18 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

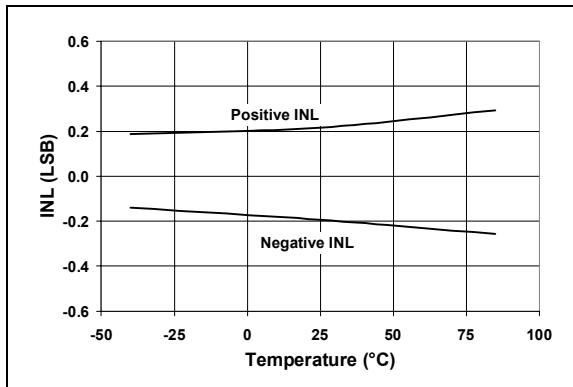


FIGURE 2-7: Integral Nonlinearity (INL) vs. Temperature.

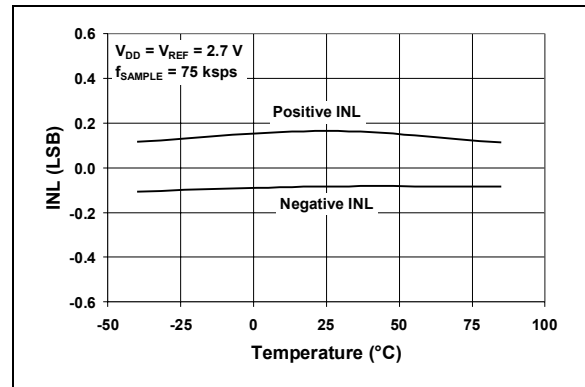


FIGURE 2-10: Integral Nonlinearity (INL) vs. Temperature ($V_{DD} = 2.7V$).

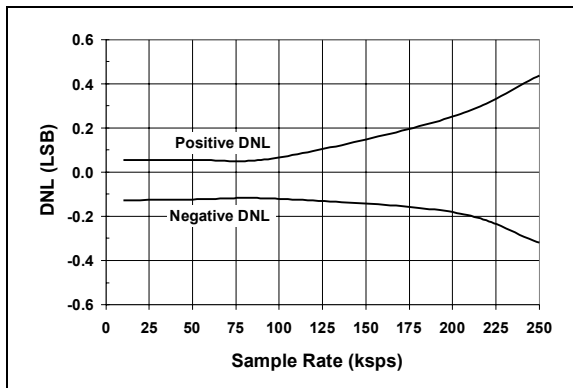


FIGURE 2-8: Differential Nonlinearity (DNL) vs. Sample Rate.

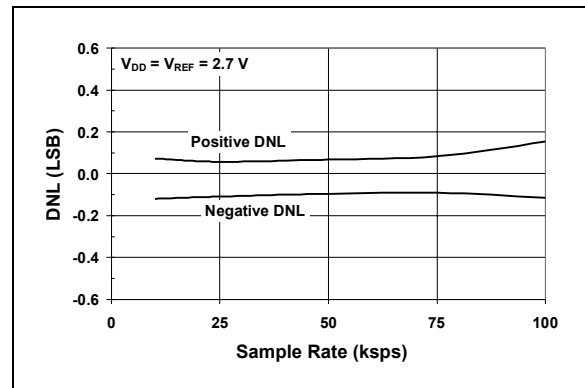


FIGURE 2-11: Differential Nonlinearity (DNL) vs. Sample Rate ($V_{DD} = 2.7V$).

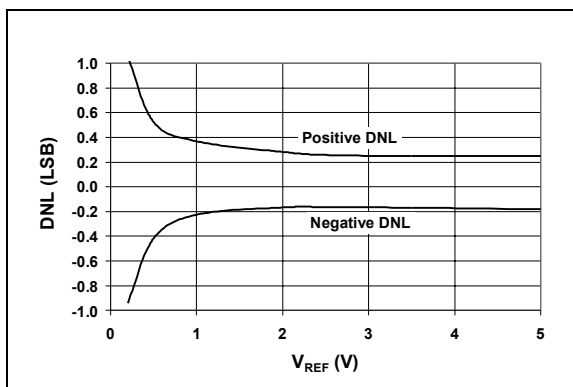


FIGURE 2-9: Differential Nonlinearity (DNL) vs. V_{REF}

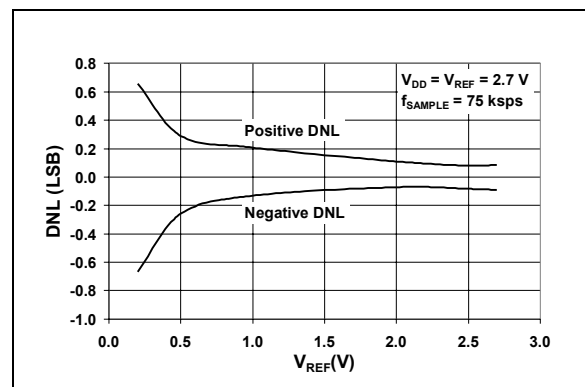


FIGURE 2-12: Differential Nonlinearity (DNL) vs. V_{REF} ($V_{DD} = 2.7V$).

MCP3004/3008

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $f_{CLK} = 18 \cdot f_{SAMPLE}$, $T_A = 25^\circ C$.

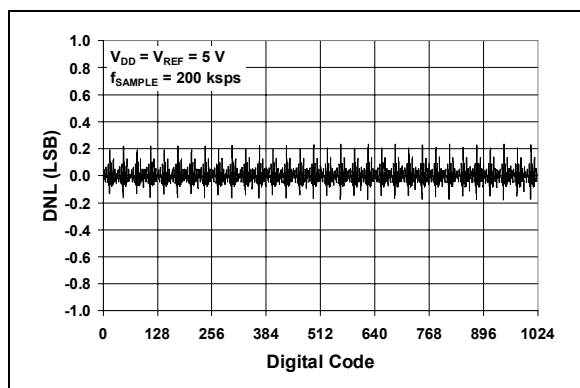


FIGURE 2-13: Differential Nonlinearity (DNL) vs. Code (Representative Part).

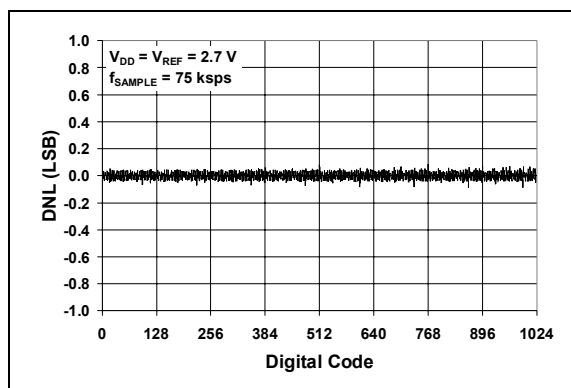


FIGURE 2-16: Differential Nonlinearity (DNL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

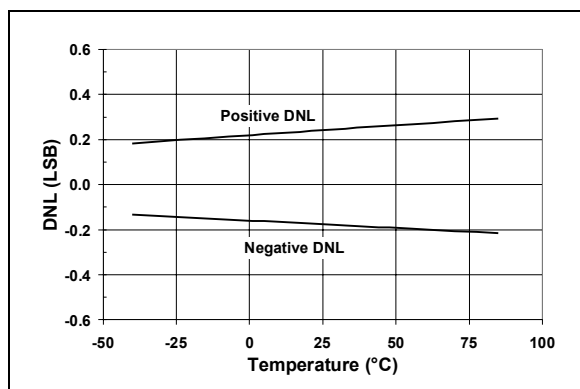


FIGURE 2-14: Differential Nonlinearity (DNL) vs. Temperature.

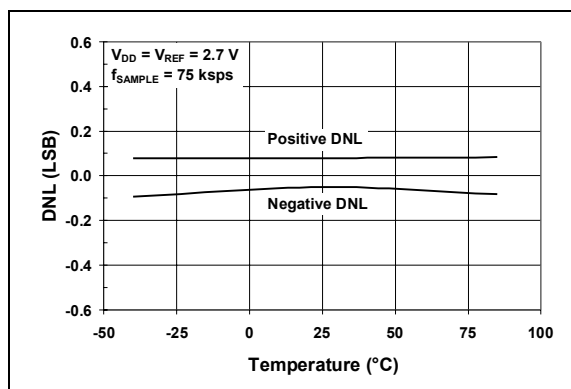


FIGURE 2-17: Differential Nonlinearity (DNL) vs. Temperature ($V_{DD} = 2.7V$).

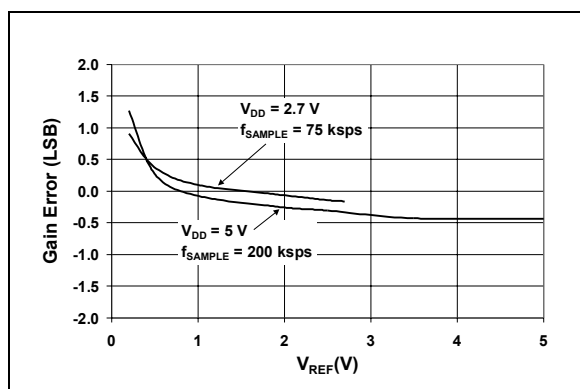


FIGURE 2-15: Gain Error vs. V_{REF}

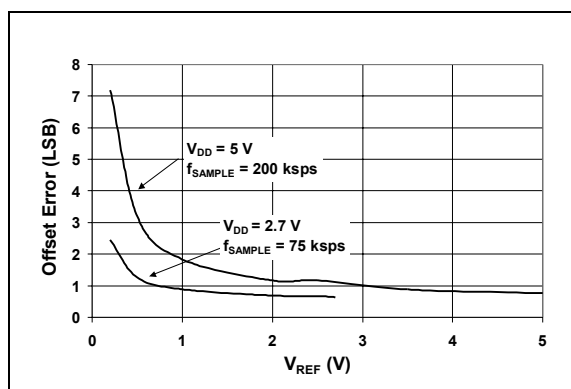


FIGURE 2-18: Offset Error vs. V_{REF}

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $f_{CLK} = 18 \cdot f_{SAMPLE}$, $T_A = 25^\circ C$.

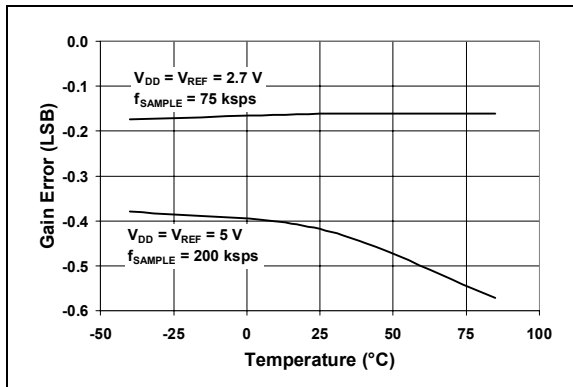


FIGURE 2-19: Gain Error vs. Temperature.

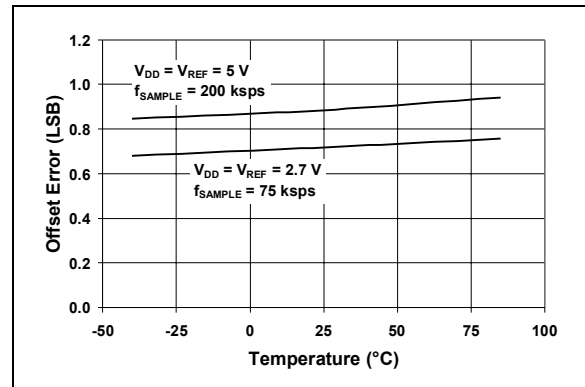


FIGURE 2-22: Offset Error vs. Temperature.

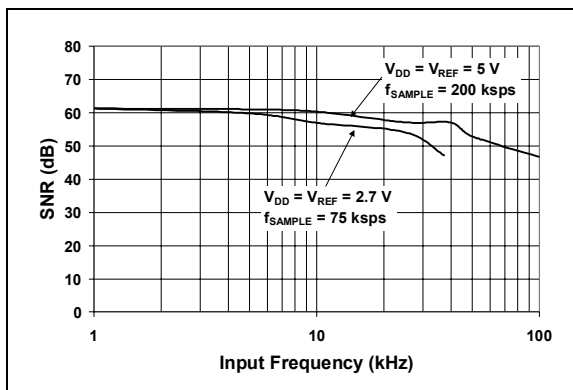


FIGURE 2-20: Signal to Noise (SNR) vs. Input Frequency.

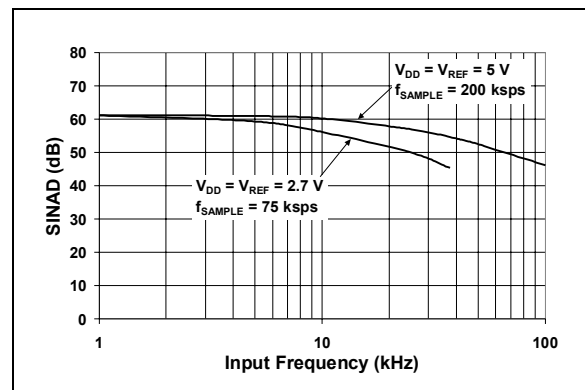


FIGURE 2-23: Signal to Noise and Distortion (SINAD) vs. Input Frequency.

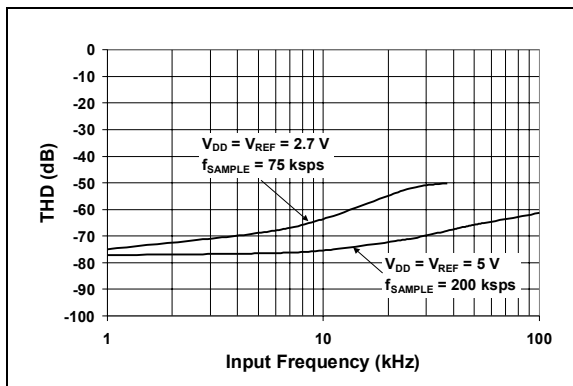


FIGURE 2-21: Total Harmonic Distortion (THD) vs. Input Frequency.

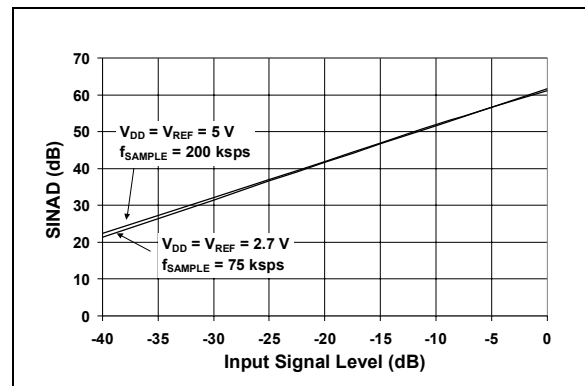


FIGURE 2-24: Signal to Noise and Distortion (SINAD) vs. Input Signal Level.

MCP3004/3008

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $f_{CLK} = 18 * f_{SAMPLE}$, $T_A = 25^\circ C$.

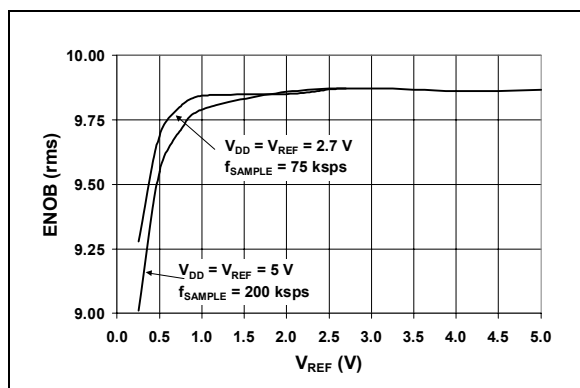


FIGURE 2-25: Effective Number of Bits (ENOB) vs. V_{REF}

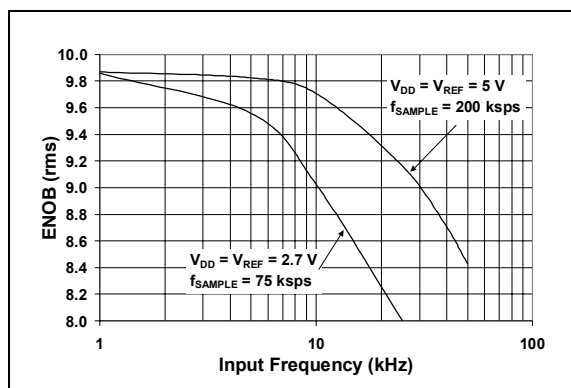


FIGURE 2-28: Effective Number of Bits (ENOB) vs. Input Frequency.

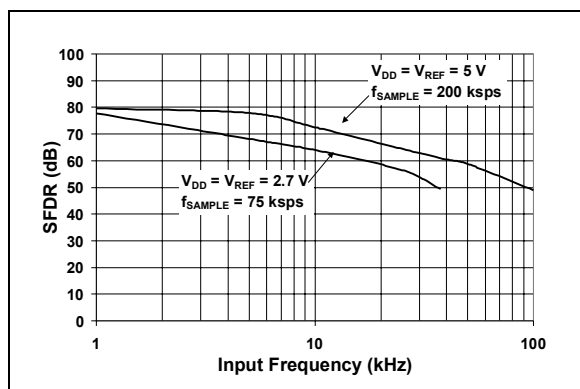


FIGURE 2-26: Spurious Free Dynamic Range (SFDR) vs. Input Frequency.

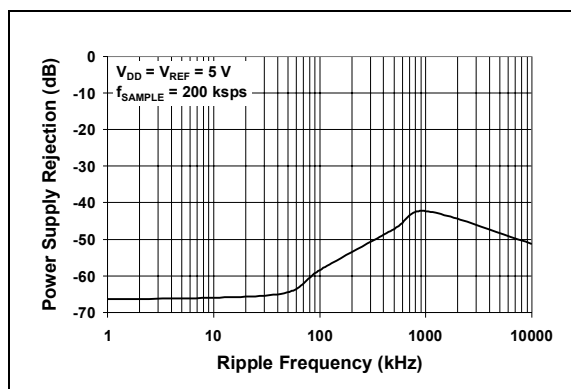


FIGURE 2-29: Power Supply Rejection (PSR) vs. Ripple Frequency.

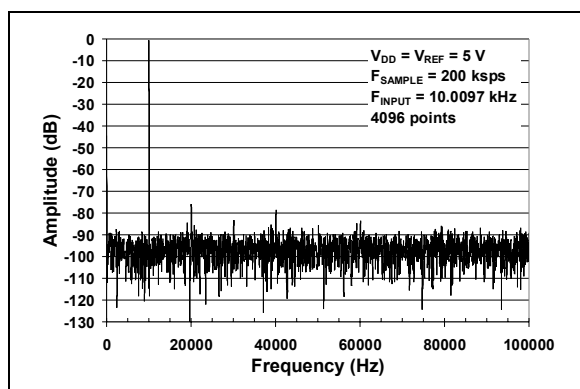


FIGURE 2-27: Frequency Spectrum of 10 kHz Input (Representative Part).

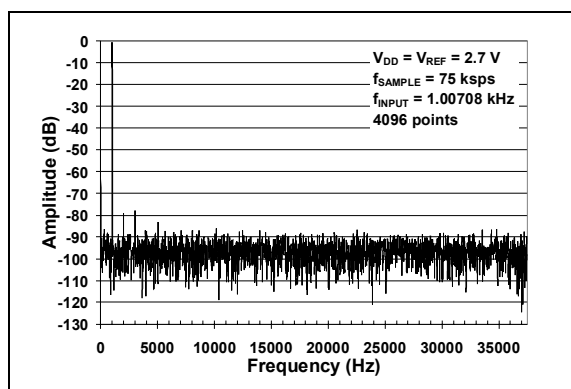


FIGURE 2-30: Frequency Spectrum of 1 kHz Input (Representative Part, $V_{DD} = 2.7V$).

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $f_{CLK} = 18 \cdot f_{SAMPLE}$, $T_A = 25^\circ C$.

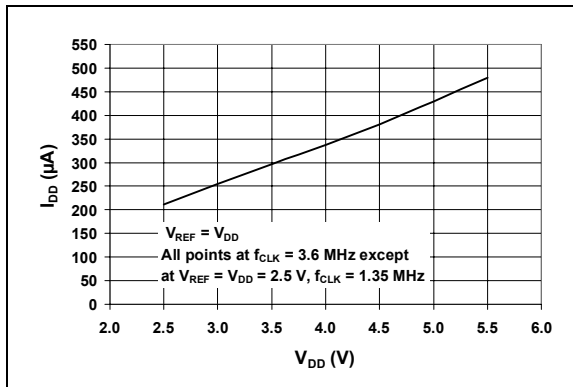


FIGURE 2-31: I_{DD} vs. V_{DD} .

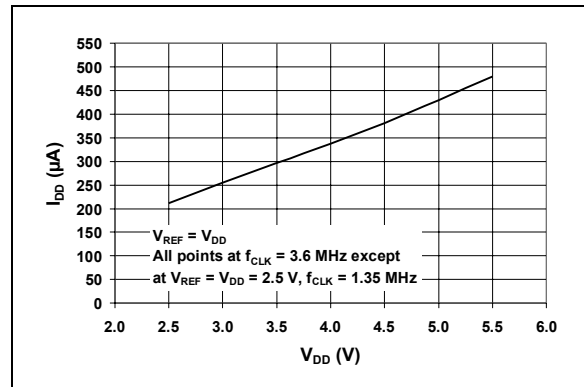


FIGURE 2-34: I_{REF} vs. V_{DD} .

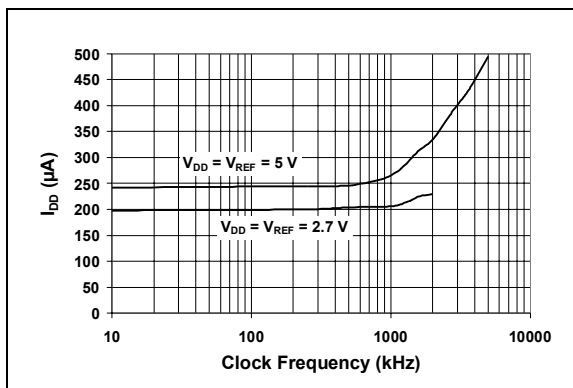


FIGURE 2-32: I_{DD} vs. Clock Frequency.

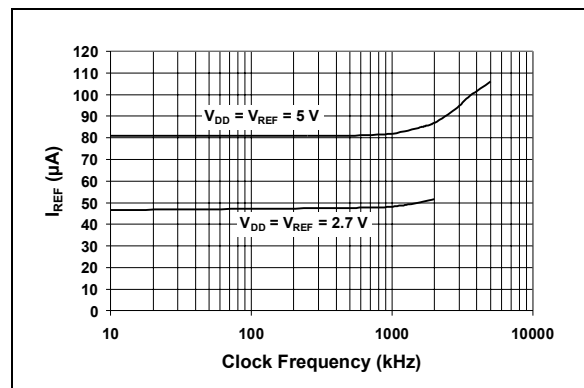


FIGURE 2-35: I_{REF} vs. Clock Frequency.

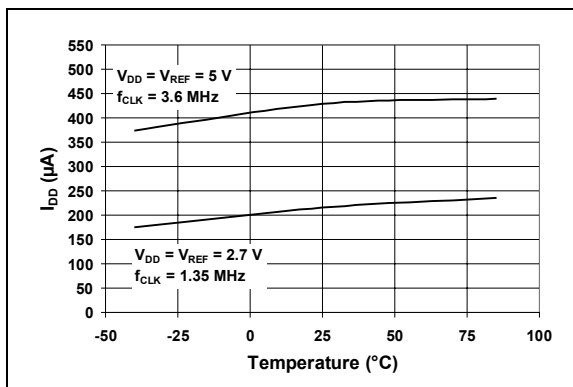


FIGURE 2-33: I_{DD} vs. Temperature.

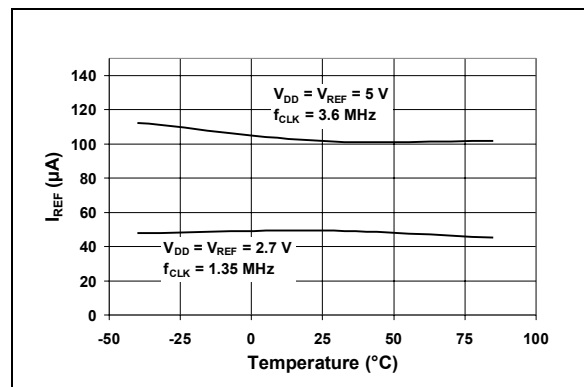


FIGURE 2-36: I_{REF} vs. Temperature.

MCP3004/3008

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $f_{CLK} = 18 * f_{SAMPLE}$, $T_A = 25^{\circ}C$.

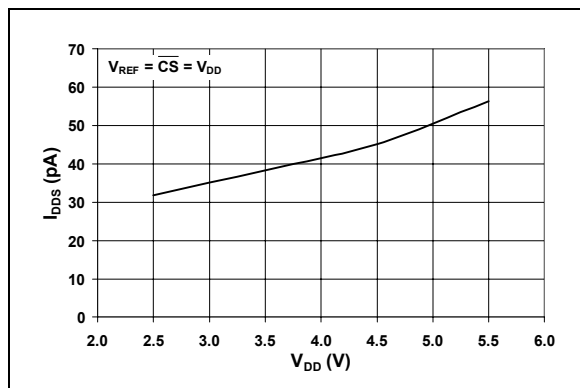


FIGURE 2-37: I_{DDs} vs. V_{DD} .

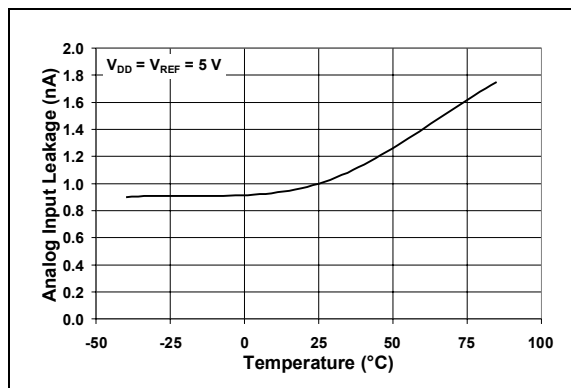


FIGURE 2-39: Analog Input Leakage Current vs. Temperature.

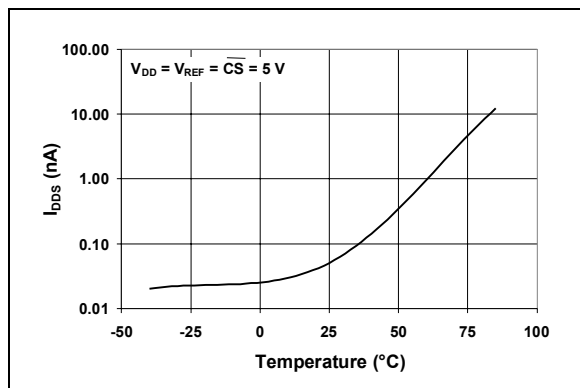


FIGURE 2-38: I_{DDs} vs. Temperature.

3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN FUNCTION TABLE

Name	Function
V _{DD}	+2.7V to 5.5V Power Supply
DGND	Digital Ground
AGND	Analog Ground
CH0-CH7	Analog Inputs
CLK	Serial Clock
D _{IN}	Serial Data In
D _{OUT}	Serial Data Out
CS/SHDN	Chip Select/Shutdown Input
V _{REF}	Reference Voltage Input

3.1 DGND

Digital ground connection to internal digital circuitry.

3.2 AGND

Analog ground connection to internal analog circuitry.

3.3 CH0 - CH7

Analog inputs for channels 0 - 7, respectively, for the multiplexed inputs. Each pair of channels can be programmed to be used as two independent channels in single-ended mode or as a single pseudo-differential input where one channel is IN+ and one channel is IN-. See Section 4.1, "Analog Inputs", and Section 5.0, "Serial Communication", for information on programming the channel configuration.

3.4 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and clock out each bit of the conversion as it takes place. See Section 6.2, "Maintaining Minimum Clock Speed", for constraints on clock speed.

3.5 Serial Data Input (D_{IN})

The SPI port serial data input pin is used to load channel configuration data into the device.

3.6 Serial Data Output (D_{OUT})

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

3.7 Chip Select/Shutdown (CS/SHDN)

The CS/SHDN pin is used to initiate communication with the device when pulled low. When pulled high, it will end a conversion and put the device in low power standby. The CS/SHDN pin must be pulled high between conversions.

4.0 DEVICE OPERATION

The MCP3004/3008 A/D converters employ a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the first rising edge of the serial clock once CS has been pulled low. Following this sample time, the device uses the collected charge on the internal sample and hold capacitor to produce a serial 10-bit digital output code. Conversion rates of 100 ksp/s are possible on the MCP3004/3008. See Section 6.2, "Maintaining Minimum Clock Speed", for information on minimum clock rates. Communication with the device is accomplished using a 4-wire SPI-compatible interface.

4.1 Analog Inputs

The MCP3004/3008 devices offer the choice of using the analog input channels configured as single-ended inputs or pseudo-differential pairs. The MCP3004 can be configured to provide two pseudo-differential input pairs or four single-ended inputs. The MCP3008 can be configured to provide four pseudo-differential input pairs or eight single-ended inputs. Configuration is done as part of the serial command before each conversion begins. When used in the pseudo-differential mode, each channel pair (i.e., CH0 and CH1, CH2 and CH3 etc.) are programmed as the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to (V_{REF} + IN-). The IN- input is limited to ±100 mV from the V_{SS} rail. The IN- input can be used to cancel small signal common-mode noise, which is present on both the IN+ and IN- inputs.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than [V_{REF} + (IN-)] - 1 LSB, then the output code will be 3FFh. If the voltage level at IN- is more than 1 LSB below V_{SS}, the voltage level at the IN+ input will have to go below V_{SS} to see the 000h output code. Conversely, if IN- is more than 1 LSB above V_{SS}, the 3FFh code will not be seen unless the IN+ input level goes above V_{REF} level.

For the A/D converter to meet specification, the charge holding capacitor (C_{SAMPLE}) must be given enough time to acquire a 10-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

This diagram illustrates that the source impedance (R_S) adds to the internal sampling switch (R_{SS}) impedance, directly affecting the time that is required to charge the capacitor (C_{SAMPLE}). Consequently, larger source impedances increase the offset, gain and integral linearity errors of the conversion (see Figure 4-2).

MCP3004/3008

4.2 Reference Input

For each device in the family, the reference input (V_{REF}) determines the analog input voltage range. As the reference input is reduced, the LSB size is reduced accordingly.

EQUATION

$$LSB\ Size = \frac{V_{REF}}{1024}$$

The theoretical digital output code produced by the A/D converter is a function of the analog input signal and the reference input, as shown below.

EQUATION

$$Digital\ Output\ Code = \frac{1024 \times V_{IN}}{V_{REF}}$$

V_{IN} = analog input voltage

V_{REF} = reference voltage

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the A/D converter.

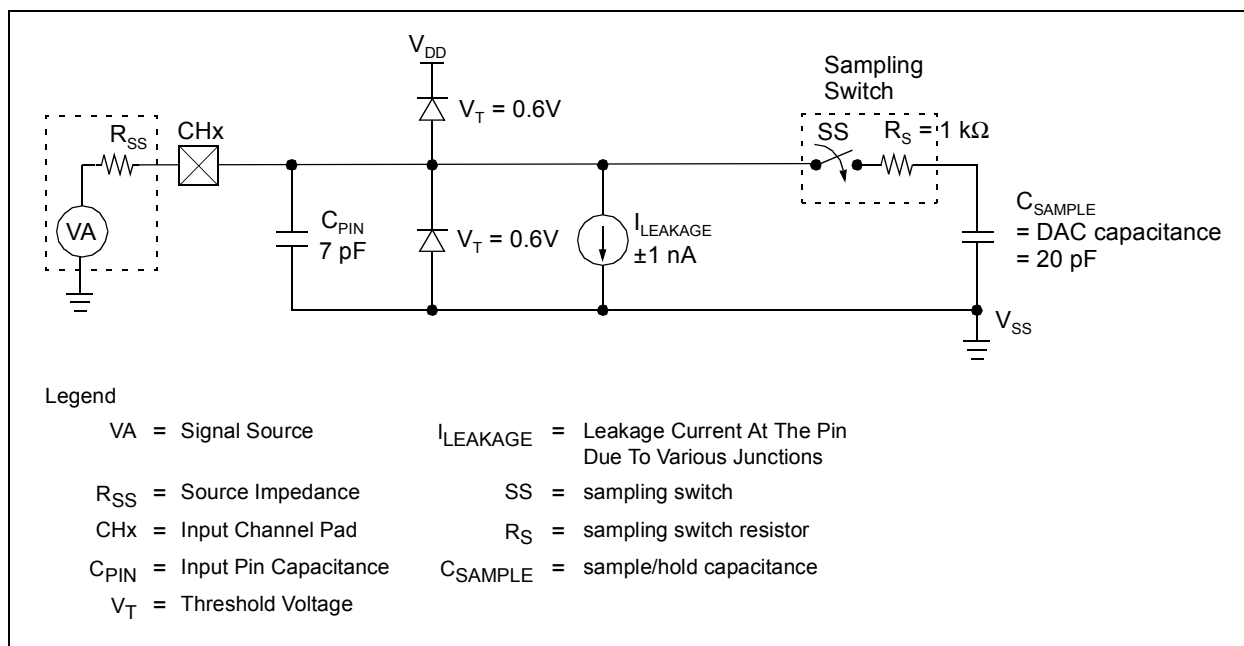


FIGURE 4-1: Analog Input Model.

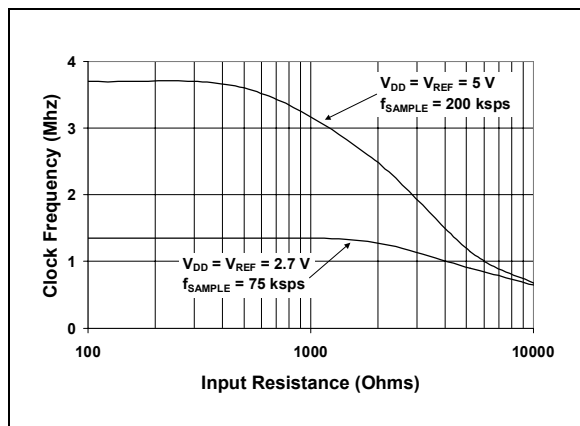


FIGURE 4-2: Maximum Clock Frequency vs. Input resistance (R_S) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.

5.0 SERIAL COMMUNICATION

Communication with the MCP3004/3008 devices is accomplished using a standard SPI-compatible serial interface. Initiating communication with either device is done by bringing the \overline{CS} line low (see Figure 5-1). If the device was powered up with the \overline{CS} pin low, it must be brought high and back low to initiate communication. The first clock received with \overline{CS} low and D_{IN} high will constitute a start bit. The SGL/DIFF bit follows the start bit and will determine if the conversion will be done using single-ended or differential input mode. The next three bits (D0, D1 and D2) are used to select the input channel configuration. Table 5-1 and Table 5-2 show the configuration bits for the MCP3004 and MCP3008, respectively. The device will begin to sample the analog input on the fourth rising edge of the clock after the start bit has been received. The sample period will end on the falling edge of the fifth clock following the start bit.

Once the D0 bit is input, one more clock is required to complete the sample and hold period (D_{IN} is a “don’t care” for this clock). On the falling edge of the next clock, the device will output a low null bit. The next 10 clocks will output the result of the conversion with MSB first, as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 10 data bits have been transmitted and the device continues to receive clocks while the \overline{CS} is held low, the device will output the conversion result LSB first, as is shown in Figure 5-2. If more clocks are provided to the device while \overline{CS} is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring \overline{CS} low and clock in leading zeros on the D_{IN} line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1, “Using the MCP3004/3008 with Microcontroller (MCU) SPI Ports”, for more details on using the MCP3004/3008 devices with hardware SPI ports.

TABLE 5-1: CONFIGURE BITS FOR THE MCP3004

Control Bit Selections				Input Configuration	Channel Selection
Single/Diff	D2*	D1	D0		
1	X	0	0	single-ended	CH0
1	X	0	1	single-ended	CH1
1	X	1	0	single-ended	CH2
1	X	1	1	single-ended	CH3
0	X	0	0	differential	CH0 = IN+ CH1 = IN-
0	X	0	1	differential	CH0 = IN- CH1 = IN+
0	X	1	0	differential	CH2 = IN+ CH3 = IN-
0	X	1	1	differential	CH2 = IN- CH3 = IN+

* D2 is “don’t care” for MCP3004

TABLE 5-2: CONFIGURE BITS FOR THE MCP3008

Control Bit Selections				Input Configuration	Channel Selection
Single/Diff	D2	D1	D0		
1	0	0	0	single-ended	CH0
1	0	0	1	single-ended	CH1
1	0	1	0	single-ended	CH2
1	0	1	1	single-ended	CH3
1	1	0	0	single-ended	CH4
1	1	0	1	single-ended	CH5
1	1	1	0	single-ended	CH6
1	1	1	1	single-ended	CH7
0	0	0	0	differential	CH0 = IN+ CH1 = IN-
0	0	0	1	differential	CH0 = IN- CH1 = IN+
0	0	1	0	differential	CH2 = IN+ CH3 = IN-
0	0	1	1	differential	CH2 = IN- CH3 = IN+
0	1	0	0	differential	CH4 = IN+ CH5 = IN-
0	1	0	1	differential	CH4 = IN- CH5 = IN+
0	1	1	0	differential	CH6 = IN+ CH7 = IN-
0	1	1	1	differential	CH6 = IN- CH7 = IN+

MCP3004/3008

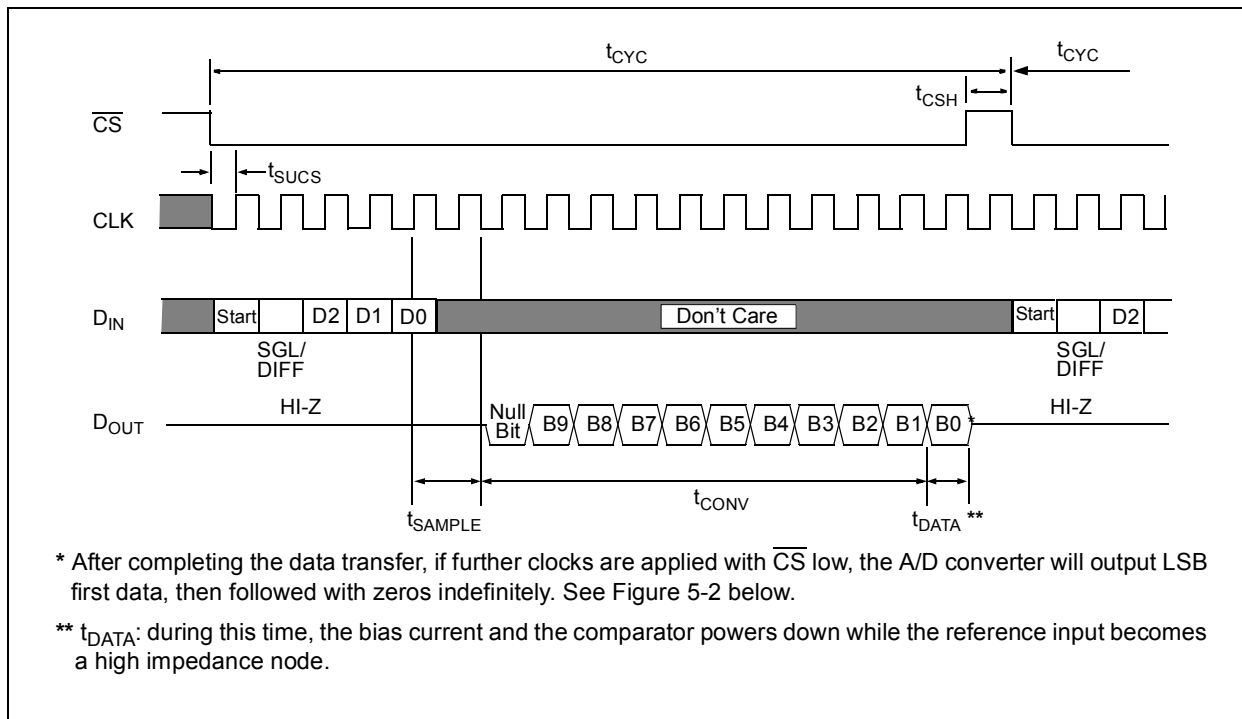


FIGURE 5-1: Communication with the MCP3004 or MCP3008.

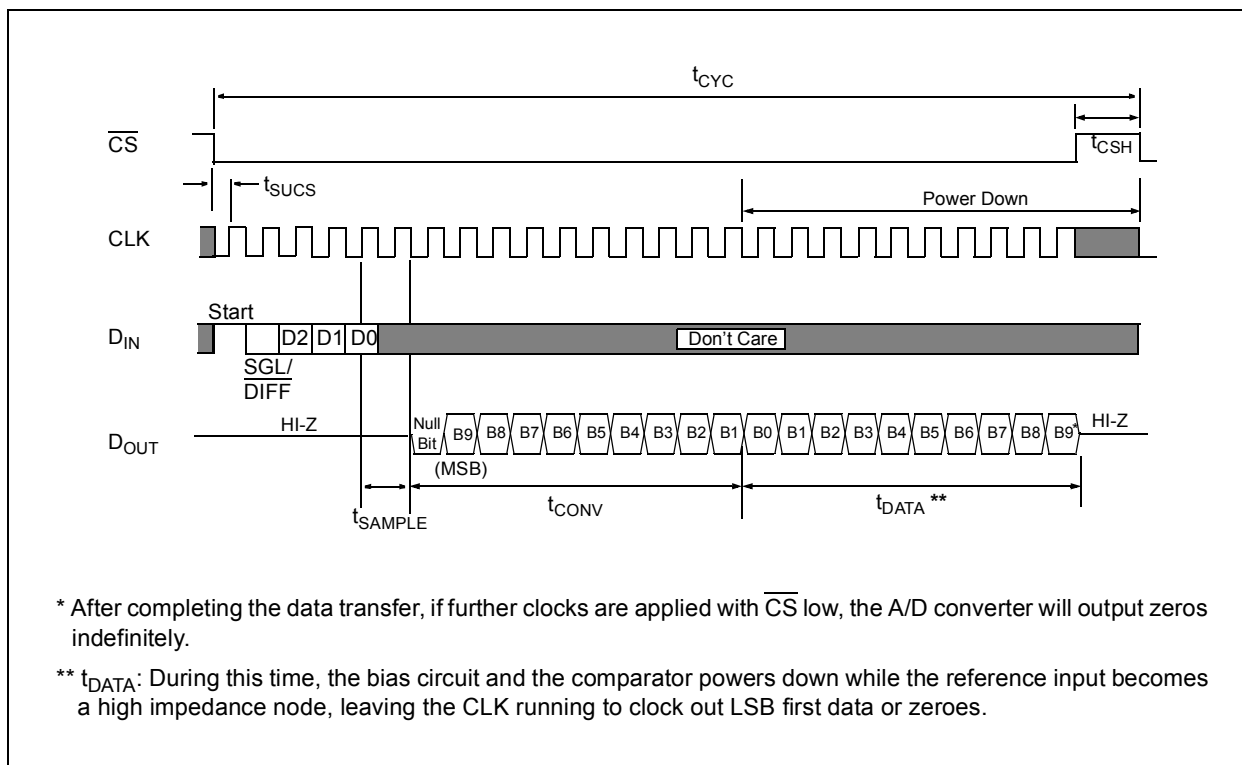


FIGURE 5-2: Communication with MCP3004 or MCP3008 in LSB First Format.

6.0 APPLICATIONS INFORMATION

6.1 Using the MCP3004/3008 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Because communication with the MCP3004/3008 devices may not need multiples of eight clocks, it will be necessary to provide more clocks than are required. This is usually done by sending 'leading zeros' before the start bit. As an example, Figure 6-1 and Figure 6-2 shows how the MCP3004/3008 can be interfaced to a MCU with a hardware SPI port. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the SCLK from the MCU idles in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1, where the clock idles in the 'high' state.

As is shown in Figure 6-1, the first byte transmitted to the A/D converter contains seven leading zeros before the start bit. Arranging the leading zeros this way induces the 10 data bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D converter on the falling edge of clock number 14. Once the second eight clocks have been sent to the device, the MCU receive buffer will contain five unknown bits (the output is at high impedance for the first two clocks), the null bit and the highest order 2 bits of the conversion. Once the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Employing this method ensures simpler manipulation of the converted data.

Figure 6-2 shows the same thing in SPI Mode 1,1, which requires that the clock idles in the high state. As with mode 0,0, the A/D converter outputs data on the falling edge of the clock and the MCU latches data from the A/D converter in on the rising edge of the clock.

MCP3004/3008

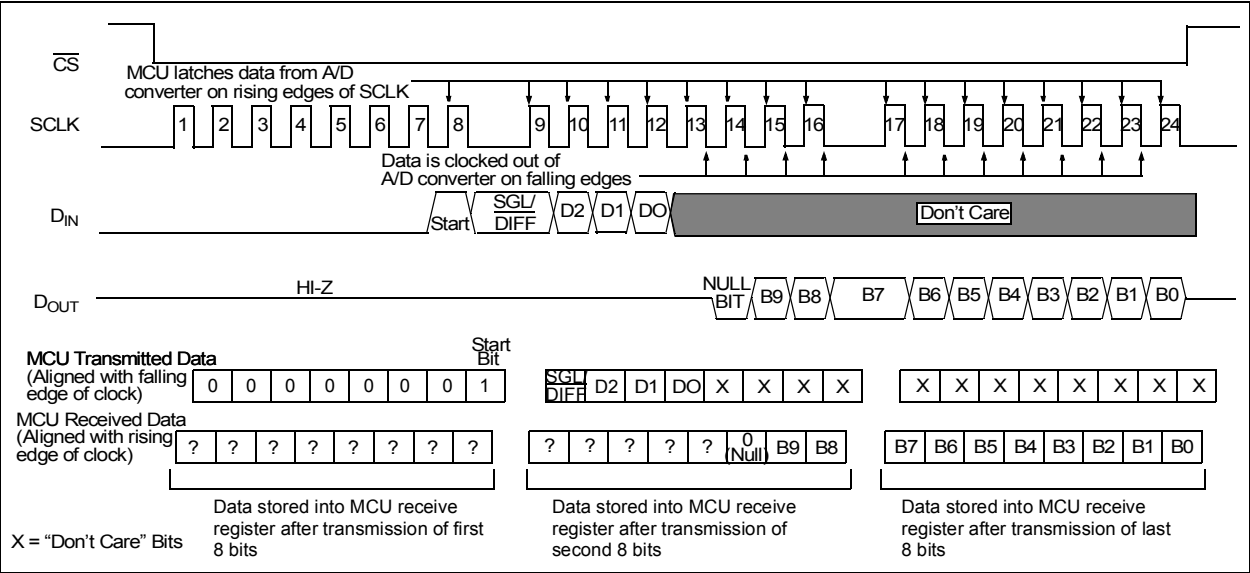


FIGURE 6-1: SPI Communication with the MCP3004/3008 using 8-bit segments (Mode 0,0: SCLK idles low).

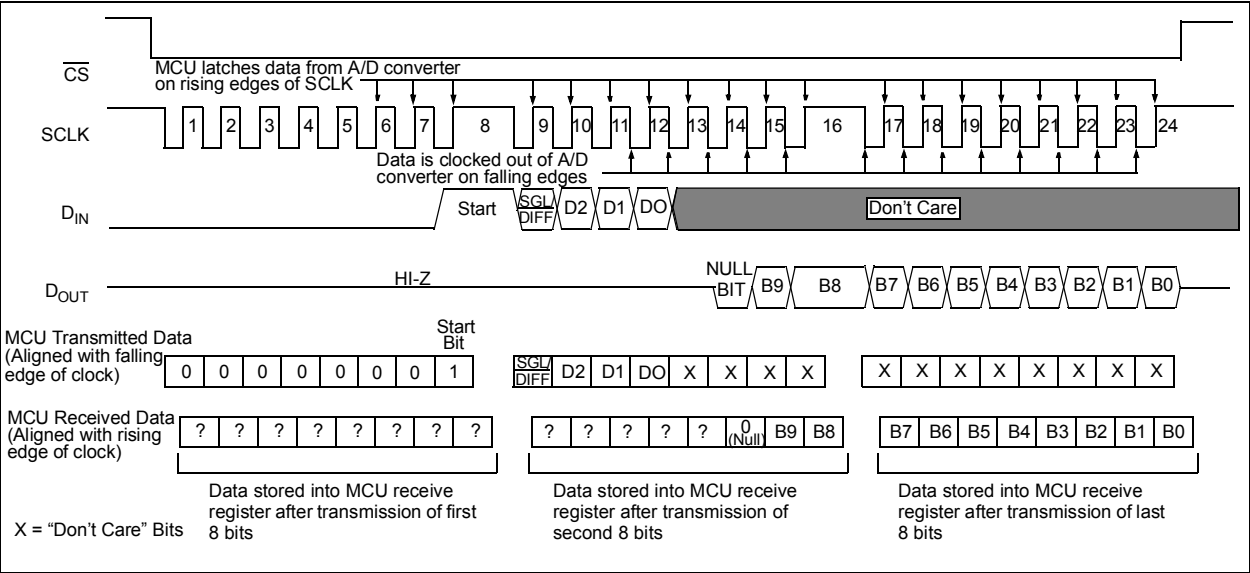


FIGURE 6-2: SPI Communication with the MCP3004/3008 using 8-bit segments (Mode 1,1: SCLK idles high).

6.2 Maintaining Minimum Clock Speed

When the MCP3004/3008 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample capacitor while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 10 data bits have been clocked out must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criterion may introduce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur (see Figure 4-2). It is also recommended that a filter be used to eliminate any signals that may be aliased back in to the conversion results, as is illustrated in Figure 6-3, where an op amp is used to drive, filter and gain the analog input of the MCP3004/3008. This amplifier provides a low impedance source for the converter input, plus a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's free interactive FilterLab™ software. FilterLab will calculate capacitor and resistors values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see AN699, "Anti-Aliasing Analog Filters for Data Acquisition Systems".

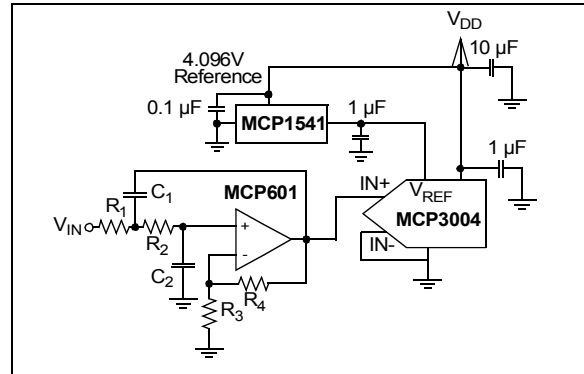


FIGURE 6-3: The MCP601 Operational Amplifier is used to implement a second order anti-aliasing filter for the signal being converted by the MCP3004.

6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1 μF is recommended.

Digital and analog traces should be separated as much as possible on the board, with no traces running underneath the device or bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a "star" configuration can also reduce noise by eliminating return current paths and associated errors (see Figure 6-4). For more information on layout tips when using A/D converters, refer to AN688, "Layout Tips for 12-Bit A/D Converter Applications".

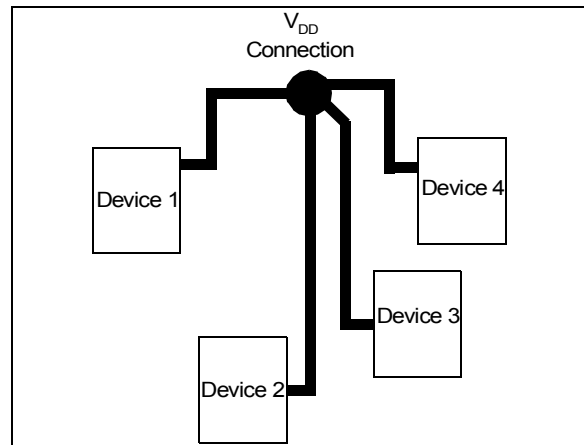


FIGURE 6-4: V_{DD} traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.

MCP3004/3008

6.5 Utilizing the Digital and Analog Ground Pins

The MCP3004/3008 devices provide both digital and analog ground connections to provide additional means of noise reduction. As is shown in Figure 6-5, the analog and digital circuitry is separated internal to the device. This reduces noise from the digital portion of the device being coupled into the analog portion of the device. The two grounds are connected internally through the substrate which has a resistance of 5 - 10 Ω .

If no ground plane is utilized, both grounds must be connected to V_{SS} on the board. If a ground plane is available, both digital and analog ground pins should be connected to the analog ground plane. If both an analog and a digital ground plane are available, both the digital and the analog ground pins should be connected to the analog ground plane. Following these steps will reduce the amount of digital noise from the rest of the board being coupled into the A/D converter.

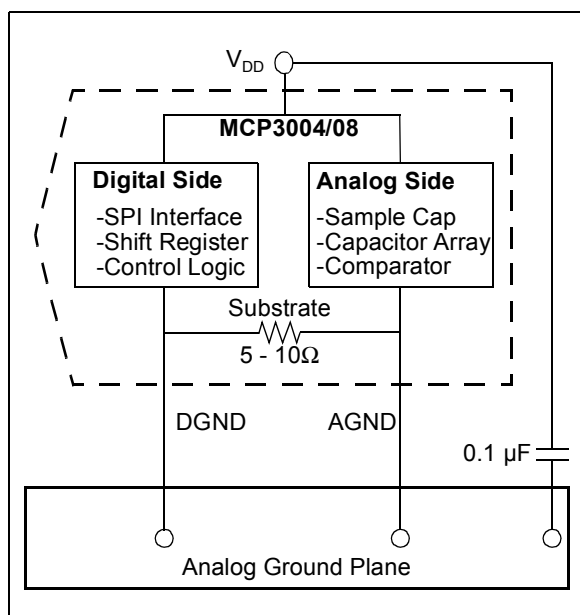
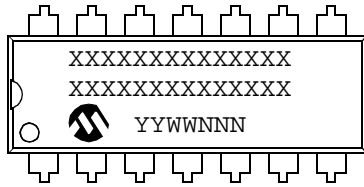


FIGURE 6-5: Separation of Analog and Digital Ground Pins.

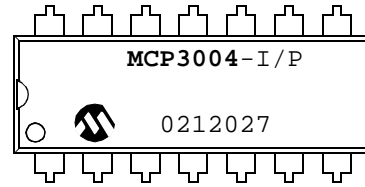
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

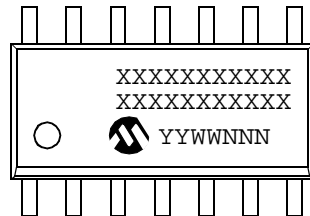
14-Lead PDIP (300 mil)



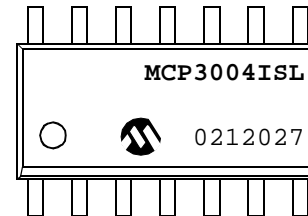
Example:



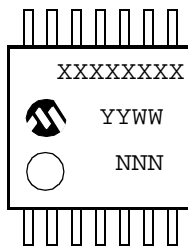
14-Lead SOIC (150 mil)



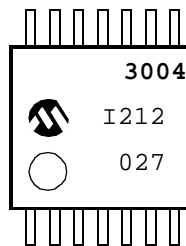
Example:



14-Lead TSSOP (4.4mm) *



Example:



* Please contact Microchip Factory for B-Grade TSSOP devices

Legend: XX...X Customer specific information*

YY Year code (last 2 digits of calendar year)

WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

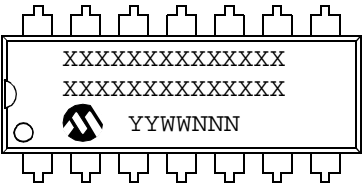
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

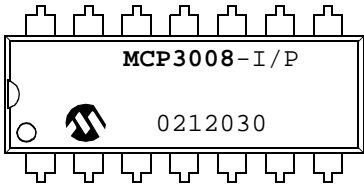
MCP3004/3008

Package Marking Information (Continued)

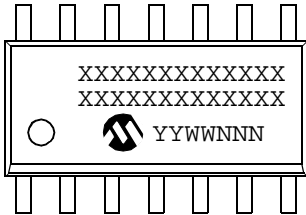
16-Lead PDIP (300 mil) (**MCP3308**)



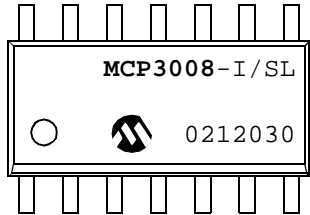
Example:



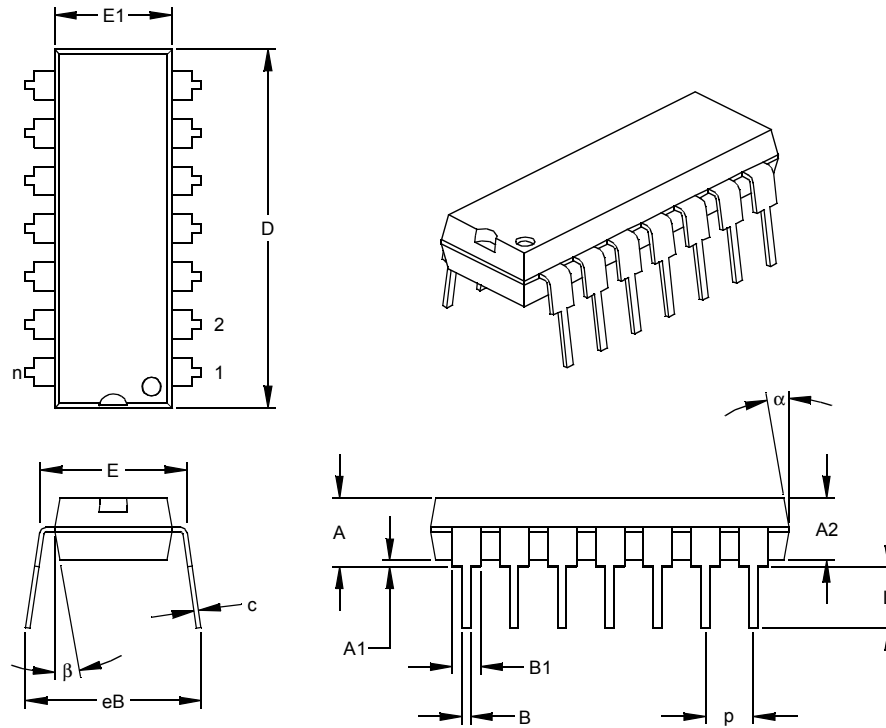
16-Lead SOIC (150 mil) (**MCP3308**)



Example:



14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

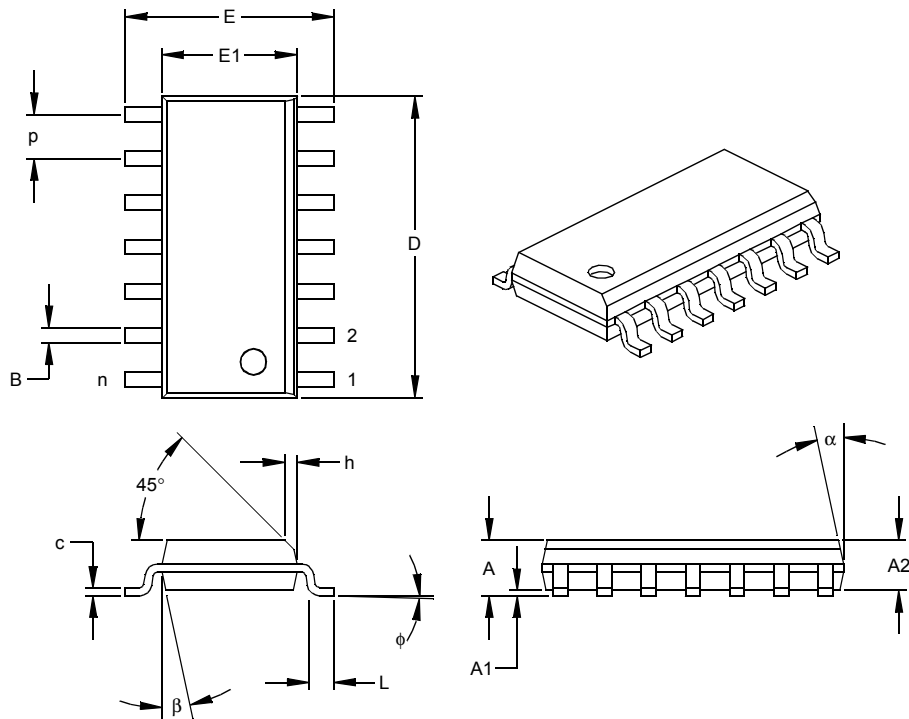
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

MCP3004/3008

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

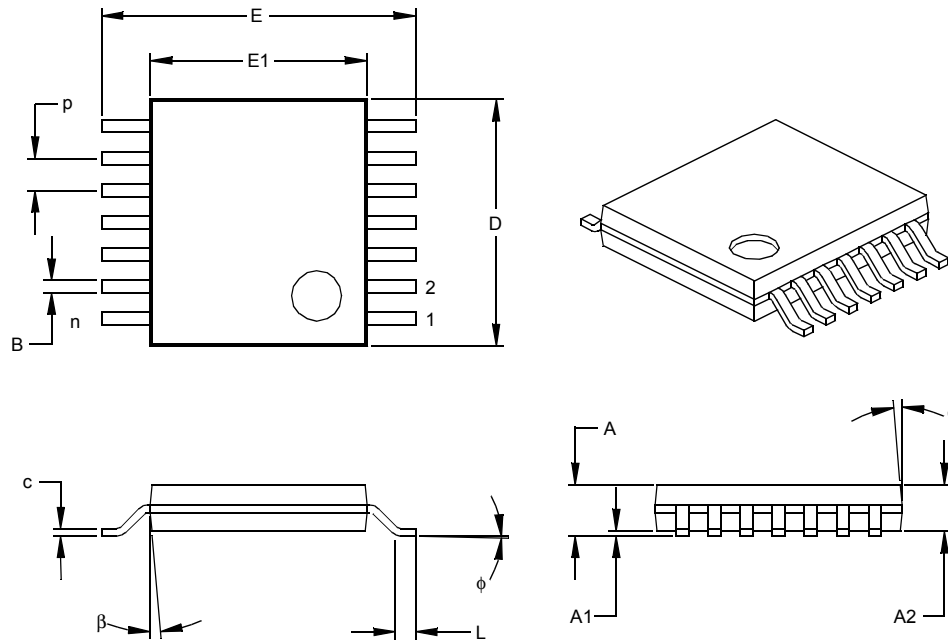
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

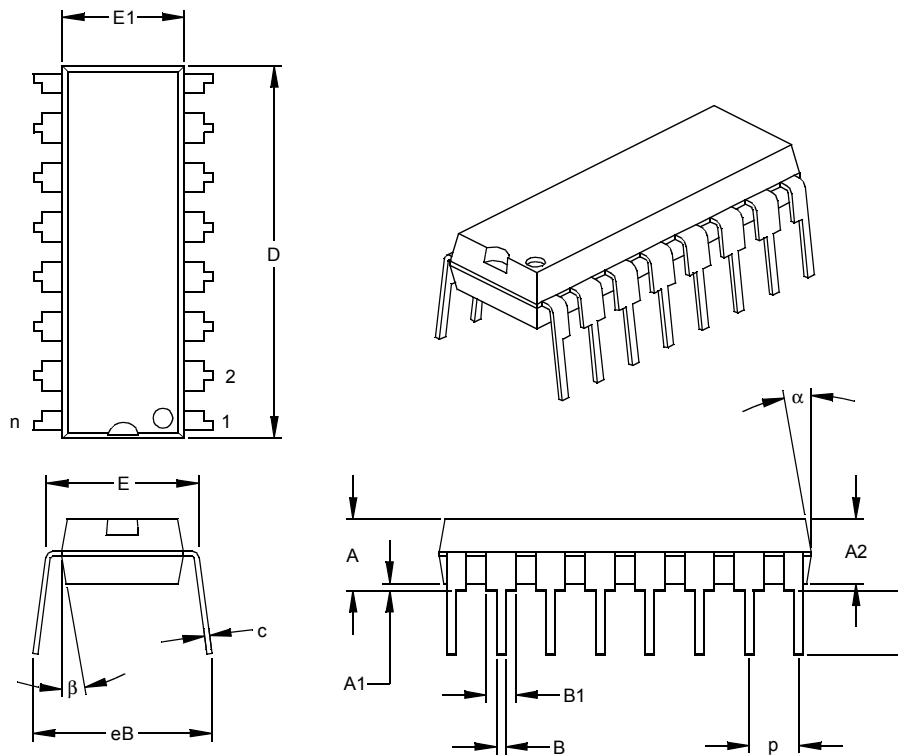
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

MCP3004/3008

16-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		16			16	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	.036	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

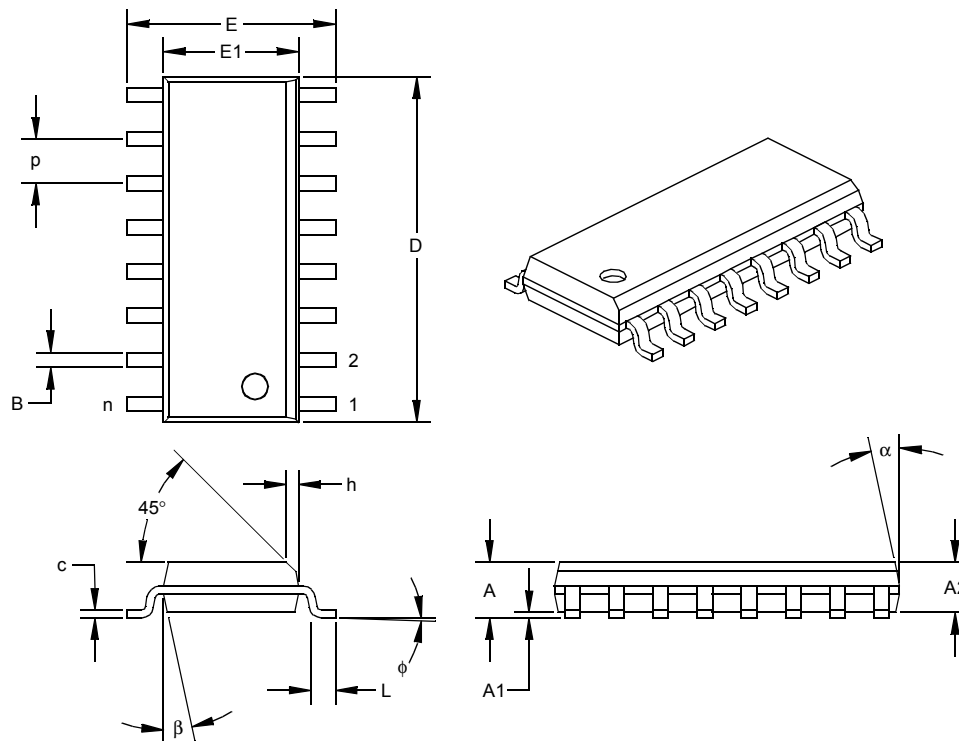
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-017

16-Lead Plastic Small Outline (SL) – Narrow 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		16			16	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.057	.061	1.32	1.44	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.386	.390	.394	9.80	9.91	10.01
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-108

MCP3004/3008

NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

<ftp://ftp.microchip.com>

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

092002

READER RESPONSE

Please list the following information, and use this outline to provide us with your comments about this document.

Total Pages Sent _____

From: Name _____

Address _____

Telephone: (____) _____ - _____ FAX: (____) _____ - _____

Literature Number: DS21295B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
<div>Device: MCP3004: 4-Channel 10-Bit Serial A/D Converter MCP3004T: 4-Channel 10-Bit Serial A/D Converter (Tape and Reel) MCP3008: 8-Channel 10-Bit Serial A/D Converter MCP3008T: 8-Channel 10-Bit Serial A/D Converter (Tape and Reel)</div> <div>Temperature Range: I = -40°C to +85°C</div> <div>Package: P = Plastic DIP (300 mil Body), 14-lead, 16-lead SL = Plastic SOIC (150 mil Body), 14-lead, 16-lead ST = Plastic TSSOP (4.4mm), 14-lead</div>		
<div>Examples:</div> <div>a) MCP3004-I/P: Industrial Temperature, PDIP package.</div> <div>b) MCP3004-I/SL: Industrial Temperature, SOIC package.</div> <div>c) MCP3004-I/ST: Industrial Temperature, TSSOP package.</div> <div>d) MCP3004T-I/ST: Industrial Temperature, TSSOP package, Tape and Reel.</div> <div>a) MCP3008-I/P: Industrial Temperature, PDIP package.</div> <div>b) MCP3008-I/SL: Industrial Temperature, SOIC package.</div>		

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

MCP3004/3008

NOTES:

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, KEELoQ, MPLAB, PIC, PICmicro, PICSTART and PRO MATE are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

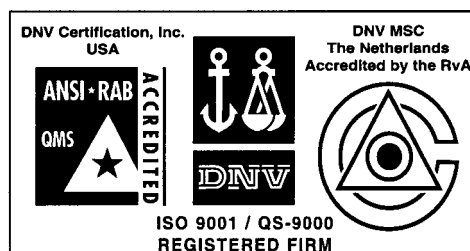
dsPIC, dsPICDEM.net, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICC, PICDEM, PICDEM.net, rPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

China - Hong Kong SAR

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Microchip:](#)

[MCP3004-I/P](#) [MCP3008-I/P](#) [MCP3004-I/SL](#) [MCP3004-I/ST](#) [MCP3008-I/SL](#) [MCP3004T-I/ST](#) [MCP3004T-I/SL](#)
[MCP3008T-I/SL](#) [MCP3004T-I/STVAO](#) [MCP3004-I/STVAO](#) [MCP3004T-I/SLVAO](#) [MCP3008T-I/SLVAO](#)