Name of the Experiment:-

Design and Implementation of 4-bit Parallel Binary Adder.

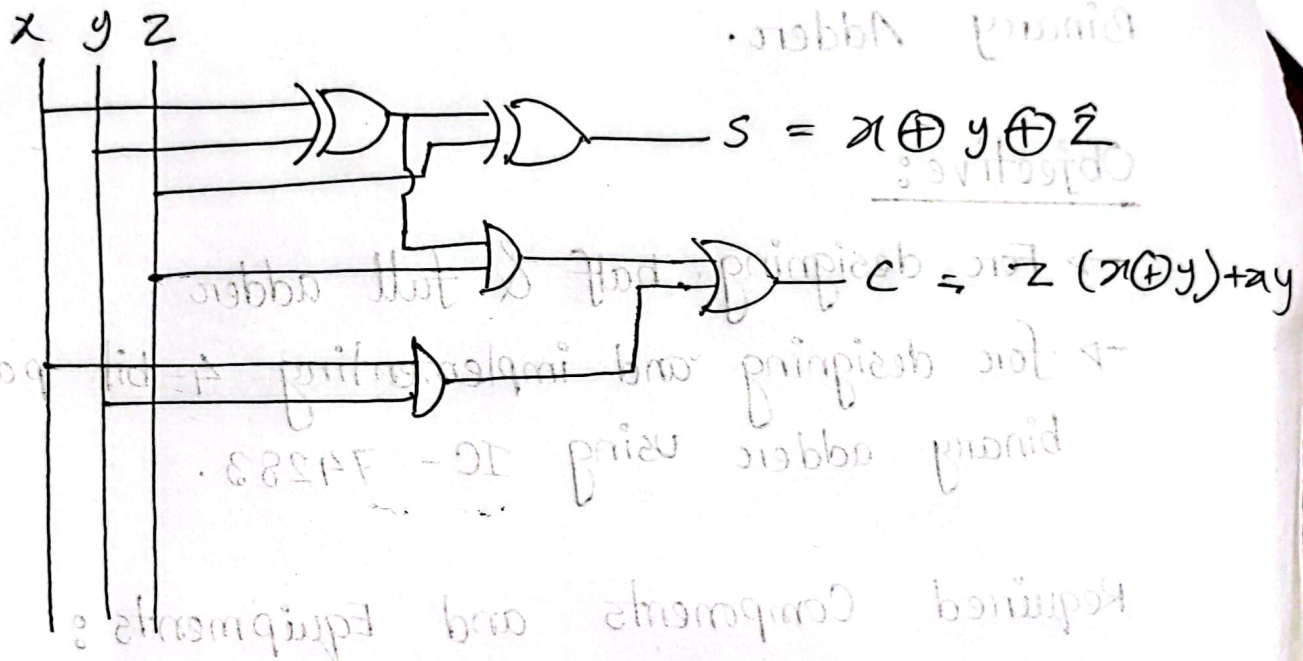
Objective:

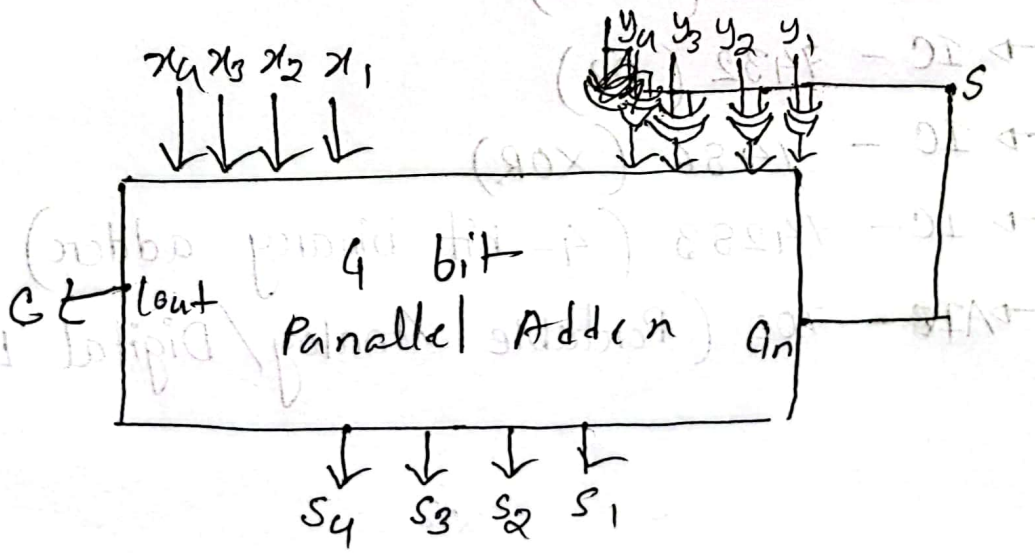
→ For designing half & full adder
→ for designing and implementing 4-bit parallel binary adder using IC- 74283.

Required Components and Equipments:

→ IC - 7408 (AND)
→ IC - 7432 (OR)
→ IC - 7486 (XOR)
→ IC- 74283 (4- bit binary adder)
→ AT - 700 (Portable Analog/Digital Laboratory)

Experimental Setup :





Results and Discussions:

Half Adder:-

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Equation; $S = x \oplus y$

$C = xy$

This half adder is able to add two single binary digits and provide an output and a carry value. One AND gate and one XOR gate is needed to create the circuit of half adder.

Full Adder:-

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Equation:

$S = x \oplus y \oplus z$

$C = z(x \oplus y) + xy$

[P.T.O.]

A full adder is a combinational circuit that forms the arithmatic sum of there input bits. It consists of three inputs and two outputs.

Two of the input variables are denoted by x and y; represent the two significant bits to be added.

The third input 'z' represents the carry of the previous lower significant position.

$S \rightarrow$ gives the value of the least significant sum.

$C \rightarrow$ gives the output carry.

4 bit parallel adder:

A	B	Cin	Sum	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Equation:

$S_i = x_i \oplus y_i \oplus z_{C_i}$

$C_{i+1} = x_i y_i + (x_i \oplus y_i) C_i$

A binary parallel adder is a digital function that produces the arithmetic sum of two binary numbers in parallel. It consists of full adder connected in cascade, with the output carry from one full adder connected to the input of next full adder.