Assignment-03

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Course Code : CSE260

Course Title : Digital Logic Design

Section : 05

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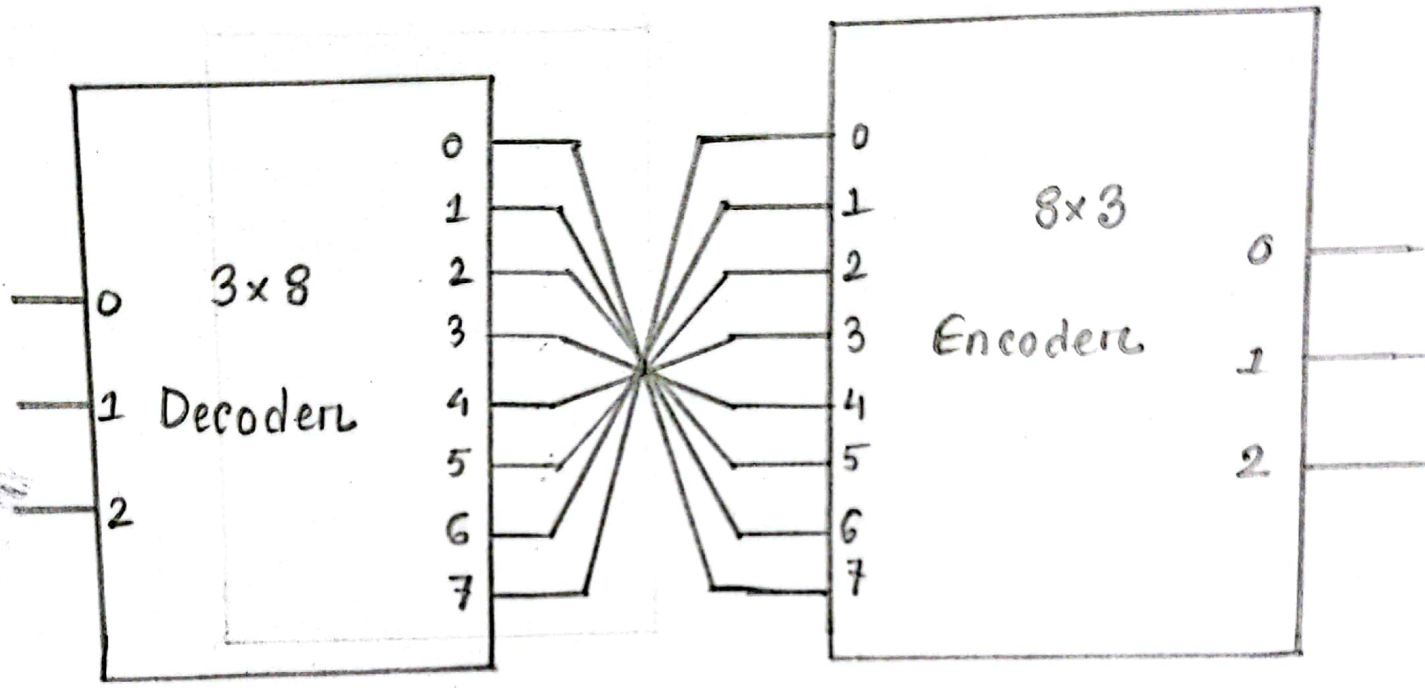
Ans. to the Q. NO - 01



Answer to the Q. NO. - 02 (a)

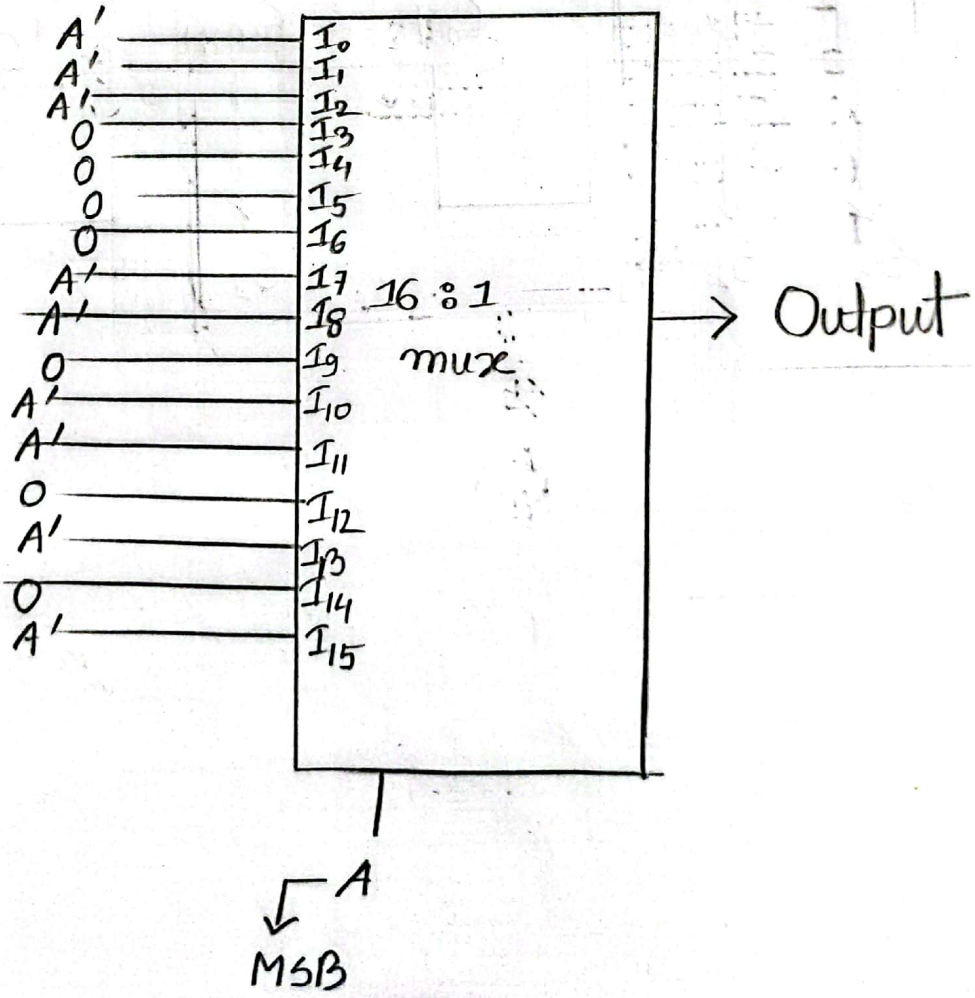
(a) 16 : 1 mux (single)

Given,

$$F(A, B, C, D) = \Sigma(0, 1, 2, 7, 8, 10, 11, 13, 15)$$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}
A'	(0)	(1)	(2)	3	4	5	6	(7)	(8)	9	(10)	(11)	12	(13)	14	(15)	16
A																	

A' A' A' 0 0 0 0 A' A' 0 A' A' 0 A' 0 A' 0

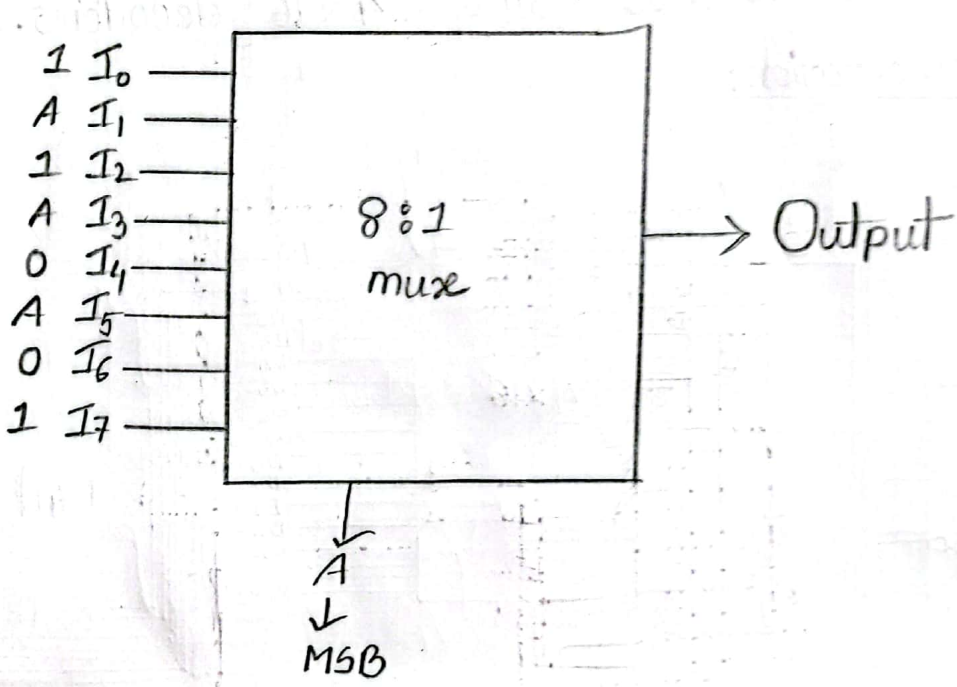


Answer to the Q. NO - 02(b)

(b) single 8:1 mux

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	(0)	(1)	(2)	3	4	5	6	(7)
A	(8)	9	(10)	(11)	12	(13)	14	(15)
	1	A'	1	A	0	A	0	1

Here, $A' + A = 1$



[P.T.O.]

Answer to the Q. NO - 03 (a)

(a) 4 x 16 decoder(s) only:

Here,

4 inputs

16 outputs

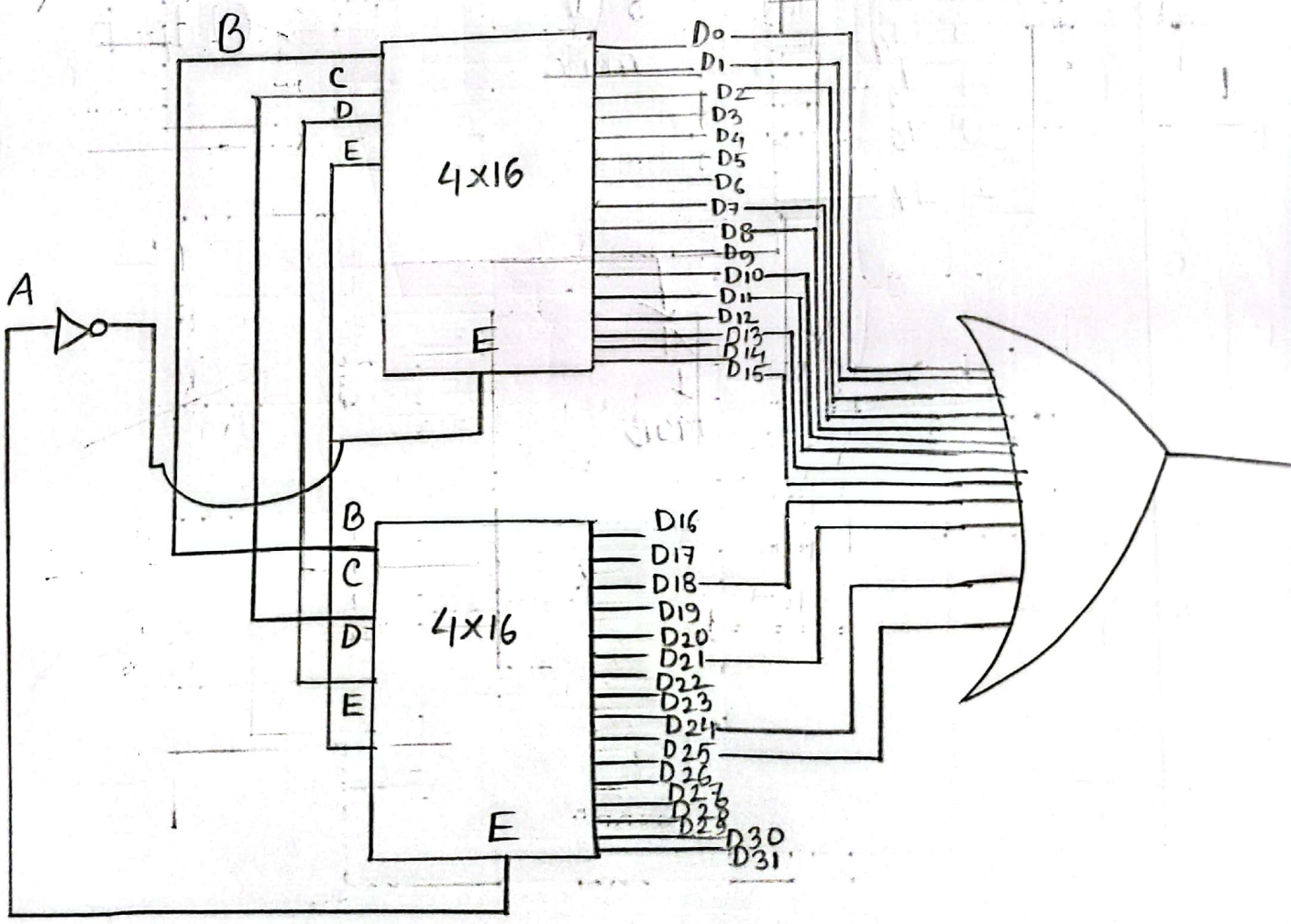
Given, $F(A, B, C, D, E) = \Sigma(0, 1, 2, 7, 8, 10, 11, 13, 15, 18, 21, 24, 25)$

input = 5

$\therefore$ output = $2^5 = 32$

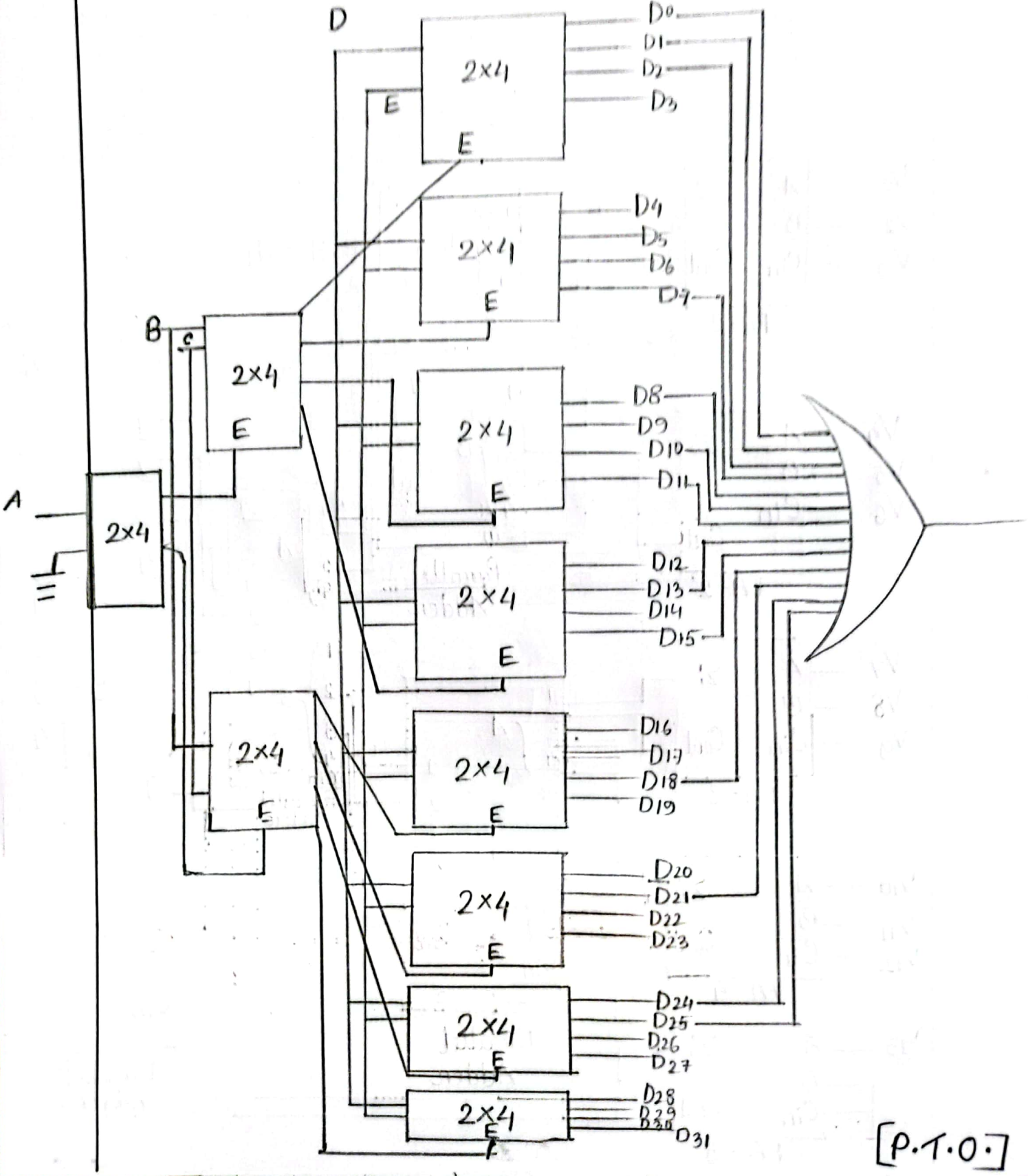
$\therefore$ we need to use two 4 x 16 decoders.

Implementation:



Answer to the Q. NO - 03 (b)

(b) 2×4 decoder(s) only :



[P.T.O.]

Ans. to the Q. NO - 04

Given,

$F(A,B,C,D,E) = \Sigma(0, 2, 5, 8, 11, 15, 18, 19, 23, 26, 29)$

exactly five 3×8 decoders.

for 5 bit → 5 variables.

Here,
- 00000 → 0
- 00010 → 2
- 00101 → 5
- 01000 → 8
- 01011 → 11
- 01111 → 15
- 10010 → 18
- 10011 → 19
- 10111 → 23
- 11010 → 26
- 11101 → 29

MSB A		LSB B	C
0		0	0
0		1	0
1		0	0
1		1	0

here,

2^4 2^3 2^2 2^1 2^0

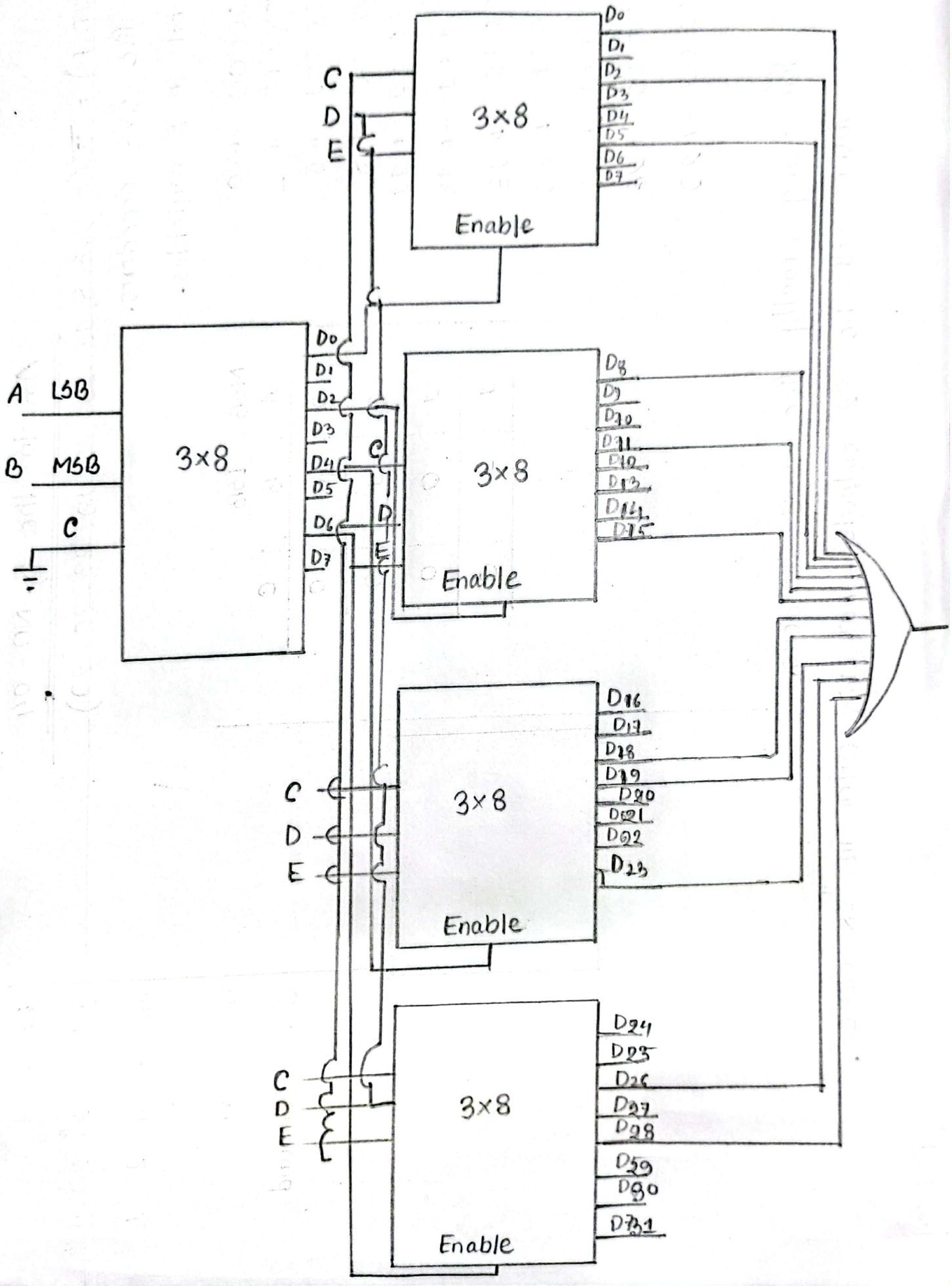
16 8 4 2 1

We Know,

C = 0 = Ground

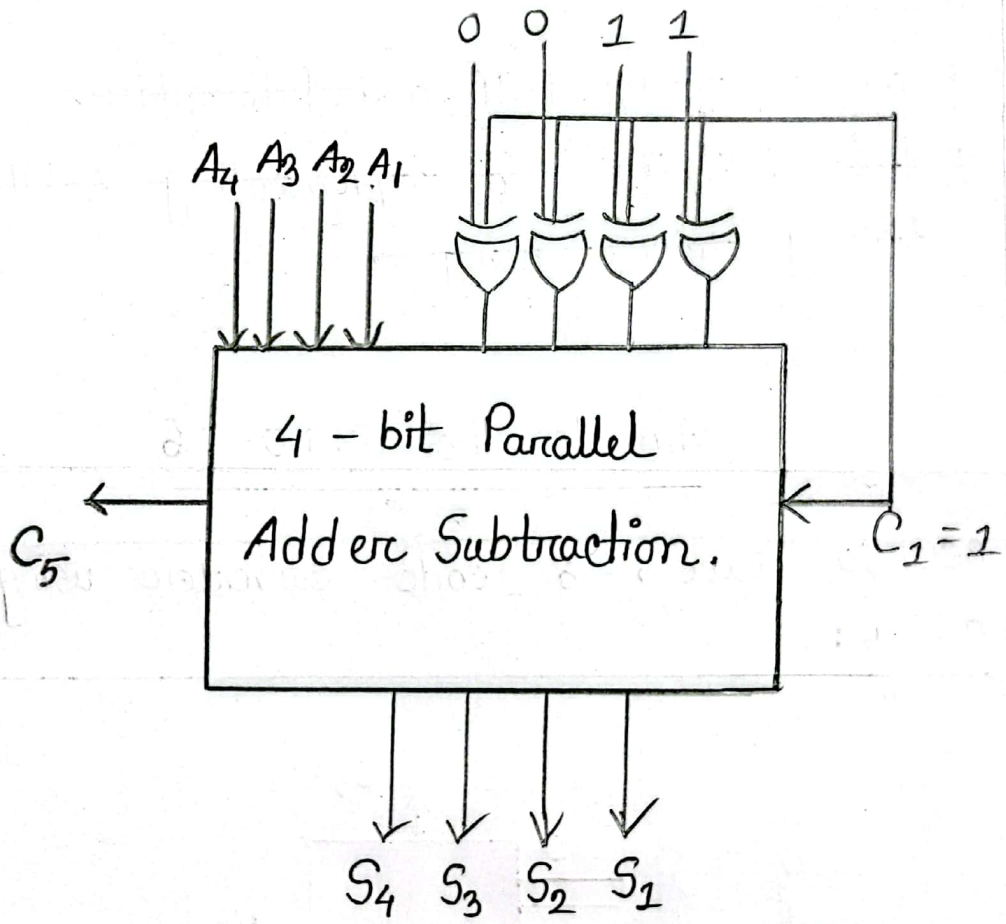
Now, for using exactly five 3×8 decoders, there will be 32 outputs that will enter in "OR Gate".

[P.T.O.]


A LSB
B MSB
C
3×8
D0
D1
D2
D3
D4
D5
D6
D7
C
D
E
Enable
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31

Answer to the Q. NO - 05

Design Implementation of A (a 4 bit number) using a 4 bit parallel adder :



Ans. to the Q. NO - 06

BCD to Excess - 6 code converter using parallel adder :