

Assignment-03

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Course Code : CSE260

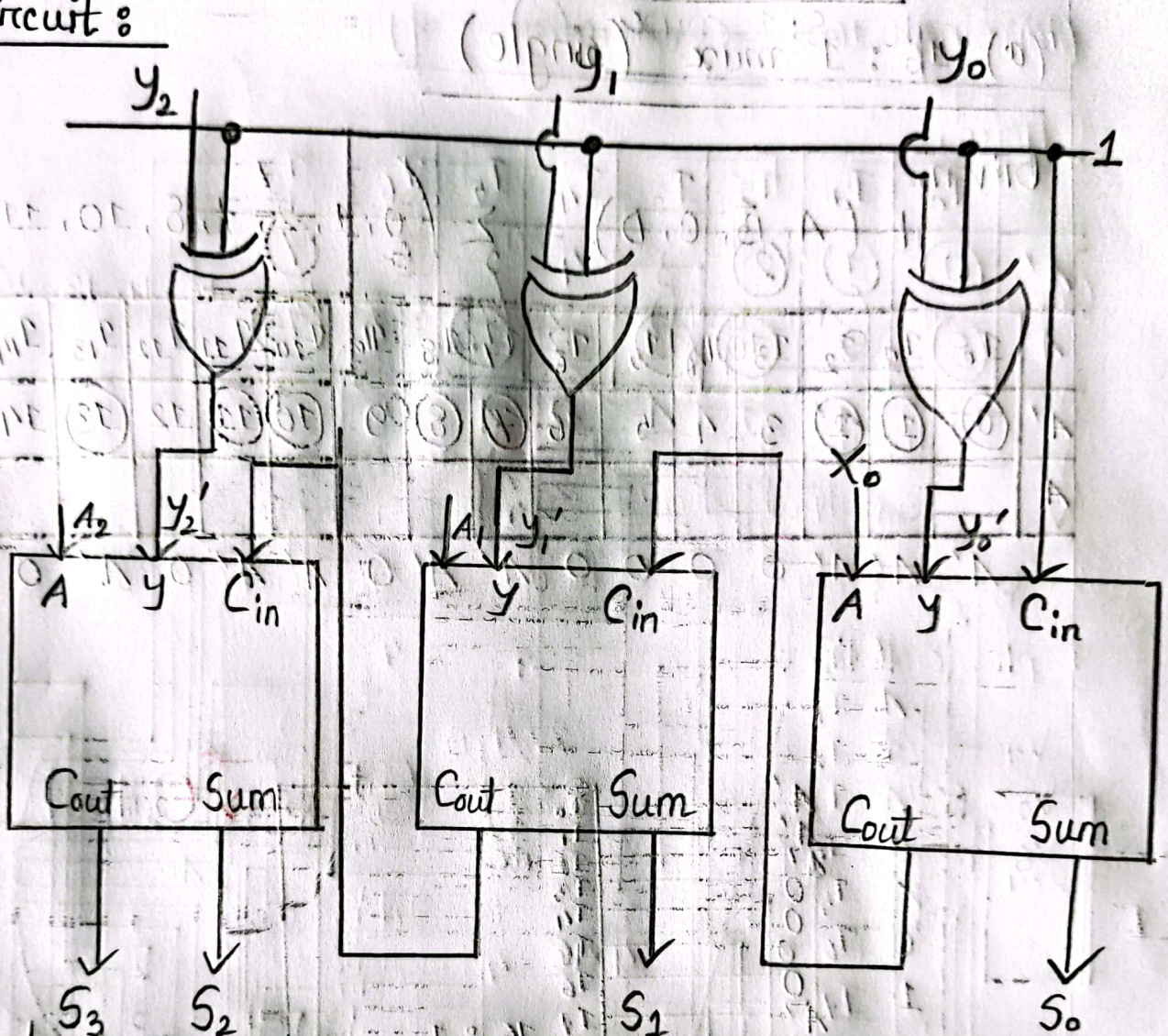
Course Title : Digital Logic Design

Section : 18

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(1) Answer to the Q. NO-01

Circuit :



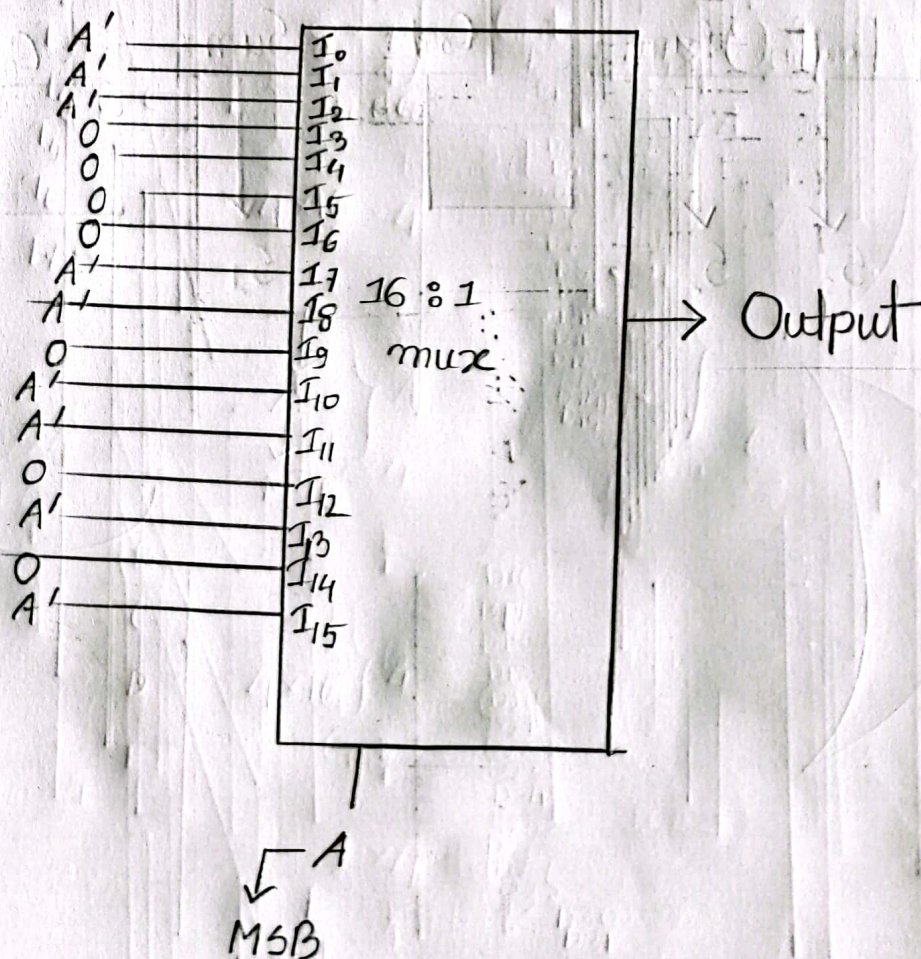
Answer to the Q. NO. - 02 (a)

(a) 16 : 1 mux (single)

Given,

$$F(A, B, C, D) = \sum (0, 1, 2, 7, 8, 10, 11, 13, 15)$$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	I_{16}
A'	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A																	
	A'	A'	A'	0	0	0	0	A'	A'	0	A'	A'	0	A'	0	A'	0

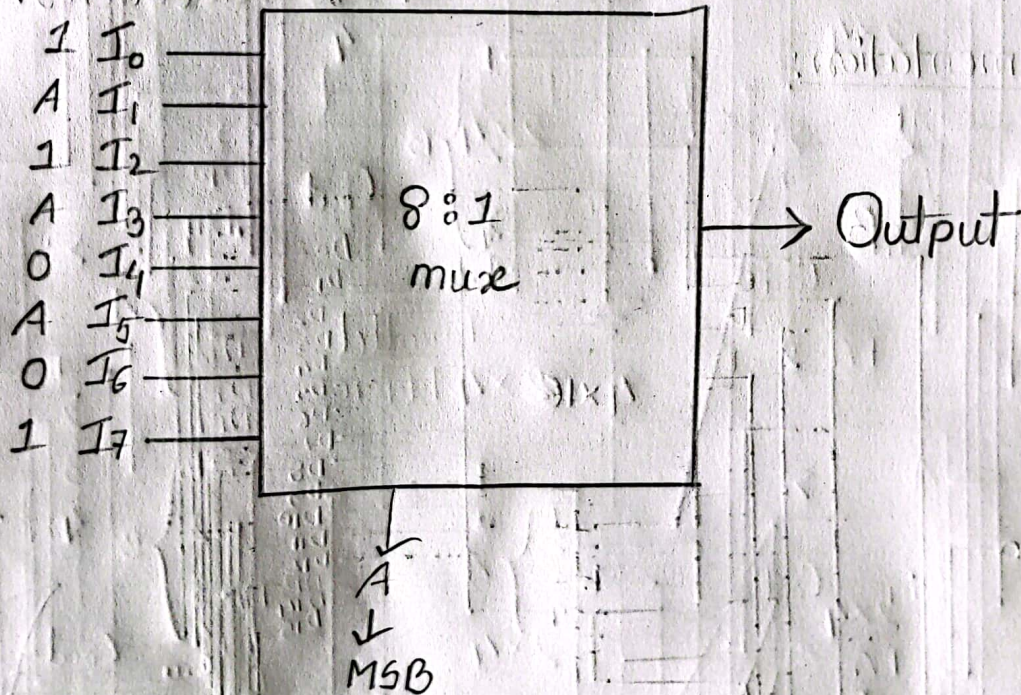


Answer to the Q. NO-02(b)

(b) single 8:1 mux

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	(0)	(1)	(2)	3	4	5	6	(7)
A	(8)	9	(10)	(11)	12	(13)	14	(15)

1 A' 1 A 0 A 0 1



Answer to the Q. NO - 03 (a)

(a) 4 x 16 decoder(s) only:

Here,

4 inputs

16 outputs

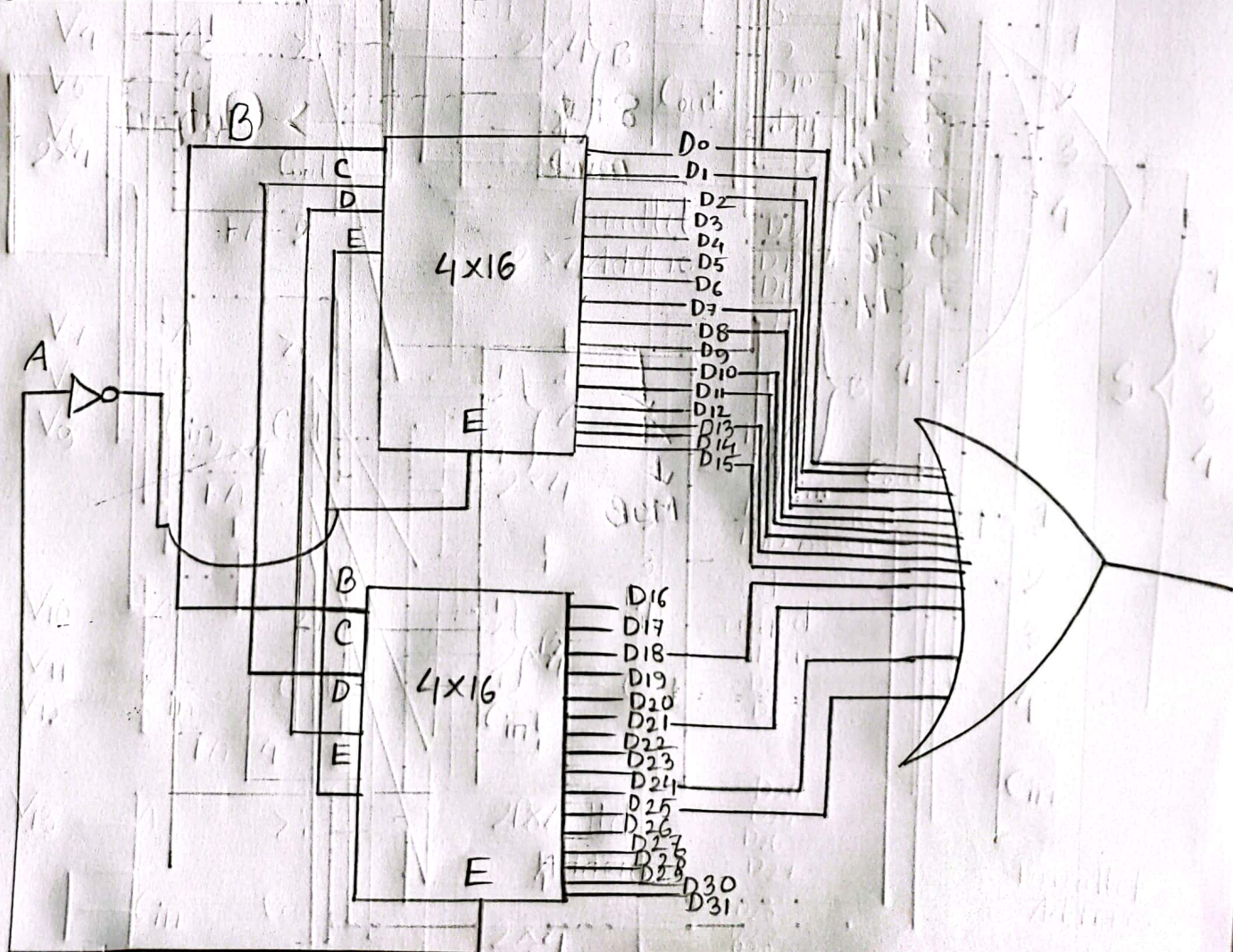
Given, $F(A, B, C, D, E) = \sum (0, 1, 2, 7, 8, 10, 11, 13, 15, 18, 21, 24, 25)$

input = 5

$\therefore \text{output} = 2^5 = 32$

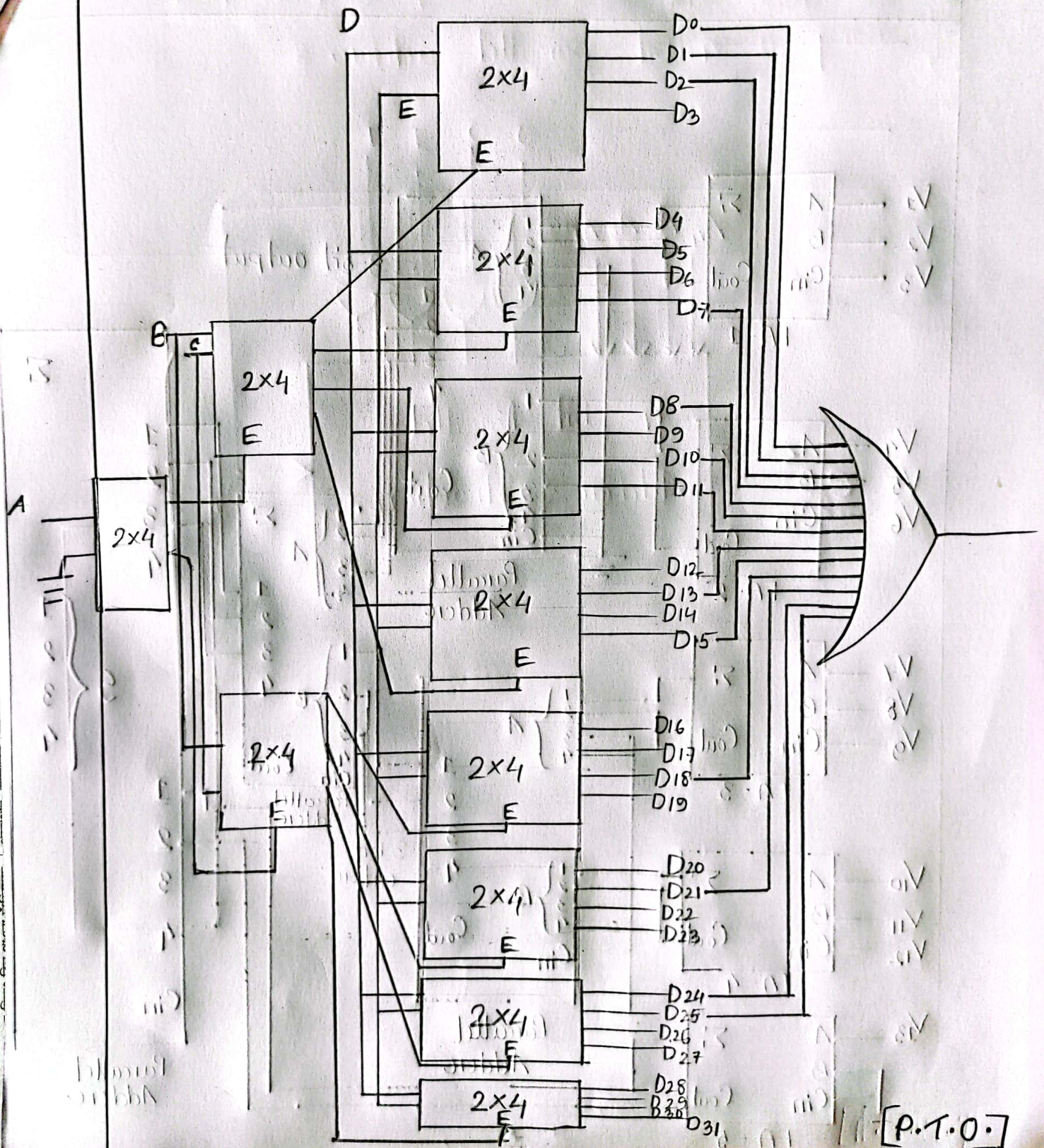
\therefore we need to use two 4 x 16 decoders.

Implementation:



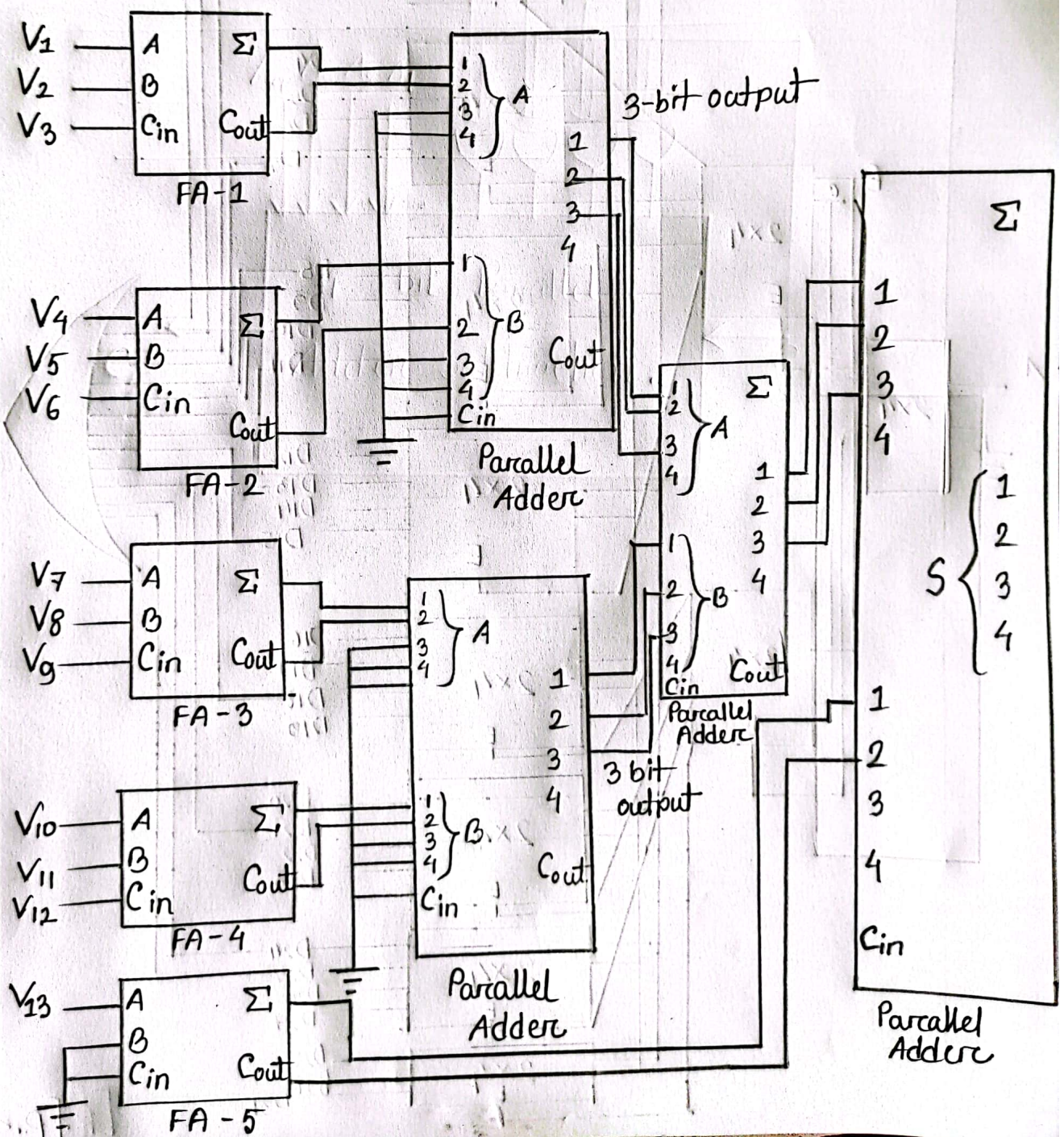
Answer to the Q. NO- 03 (b)

(b) 2x4 decoder(s) only:



Answer to the Q. NO - 04

13 person voter counting system using full and parallel adders :



Answer to the Q. NO - 05

Design Implementation of A (a 4 bit number) using a 4 bit parallel adder :

