







Comment	Description	Designator	Footprint	LibRef	Quantity
EEUFC2A471	Aluminum Electrolytic Capacitors (Radial Lead Type) AEC-Q200 Qualified 470uF ±20% 100V	C1, C4	FP-RAD-TH-D_16_0_5-L_40_2-MFG	CMP-05427-000270-1	2
08051C153KAT2A		C2	CAPC2013X94X50NL20T25	CMP-2007-04180-1	1
150nF	08053C154KAT2A	C3	CAPC2013X140X50LL20T25	CMP-1036-04480-3	1
1N4007 SMD	Rectifier, 1Kv, 1A, Do-214Ac Rohs Compliant: Yes	D1	FP-1N4007_SMD-IPC_C	CMP-12389-000001-1	1
5011	Test Point, Black, Through Hole, RoHS, Bulk	GND	KSTN-5011_V	CMP-1672-00003-4	1
575-4	Banana Jack, Non-Insulated, 1-Pin THD, RoHS, Bulk	GND2, VCC	KSTN-575-4	CMP-2000-05649-1	2
120uH	120uH 2300HT-121-V-RC	L1	IND_2300HT-V_56_42	2300HT-121-V-RC	1
22-28-4033	Male Header, Pitch 2.54 mm, 1 x3 Position, Height 8.38 mm, Tail Length 3.18 mm, RoHS, Bulk	P1	MOLX-22-28-4033_V	CMP-1676-00001-5	1
IPB032N10N5ATMA1	MOSFETN-CH 100V 166A TO263-7	Q1, Q2	FP-PG-TO263-7-MFG	CMP-32901-001276-1	2
0R3J	Jumper 0603 (1608 Metric)	R1, R2, R3	RESC0603(1608)_L	CMP-009-00063-2	3
LM5106MM/NOPB	100V Half-Bridge Gate Driver with Programmable Dead-Time, 10-pin MSOP, Pb-Free	U1	DGS0010A_N	CMP-0063-01354-3	1
5010	Test Point, Red, Through Hole, RoHS, Bulk	VCC	KSTN-5010_V	CMP-1672-00002-4	1
691137710002		VIN, VOUT	691137710002	CMP-1502-03324-2	2

## Design Rules Verification Report

Filename : C:\Users\temp\Documents\WPI\MQP\Github\MPPT\_MQP\_PCB\_DCDC\MQP\_PCB

Warnings 0  
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Clearance Constraint (Gap=10mil) (InComponent("U1")),(All)	0
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=10mil) (Preferred=10mil) (All)	0
Width Constraint (Min=10mil) (Max=50mil) (Preferred=10mil) (All)	0
Width Constraint (Min=10mil) (Max=100mil) (Preferred=10mil) (InNet("SW"))	0
Routing Topology Rule(Topology=Shortest) (All)	0
Power Plane Connect Rule(Direct Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (Disabled)(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=10mil) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=5mil) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=10000mil) (Preferred=5000mil) (InComponent("L1"))	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	0