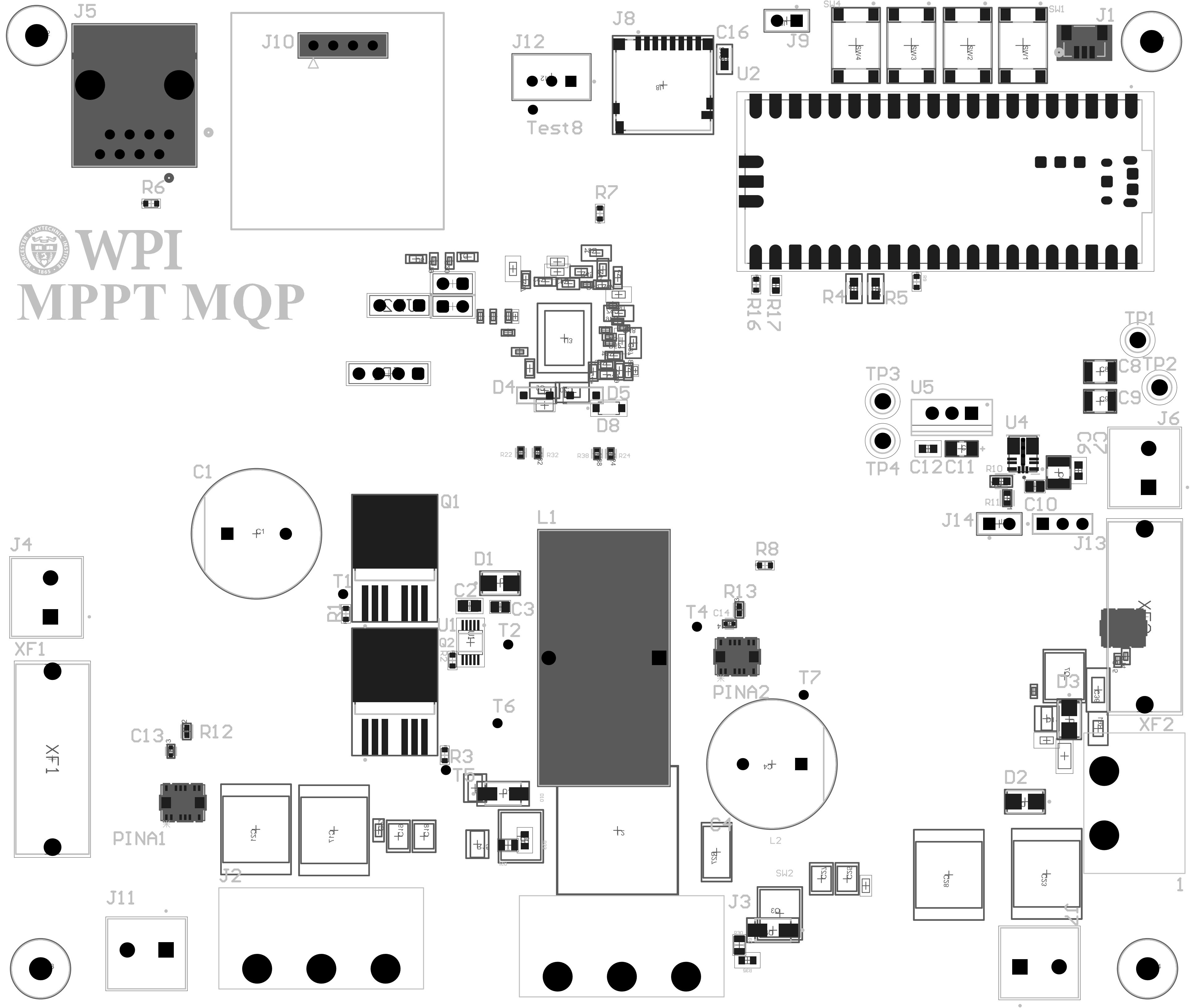
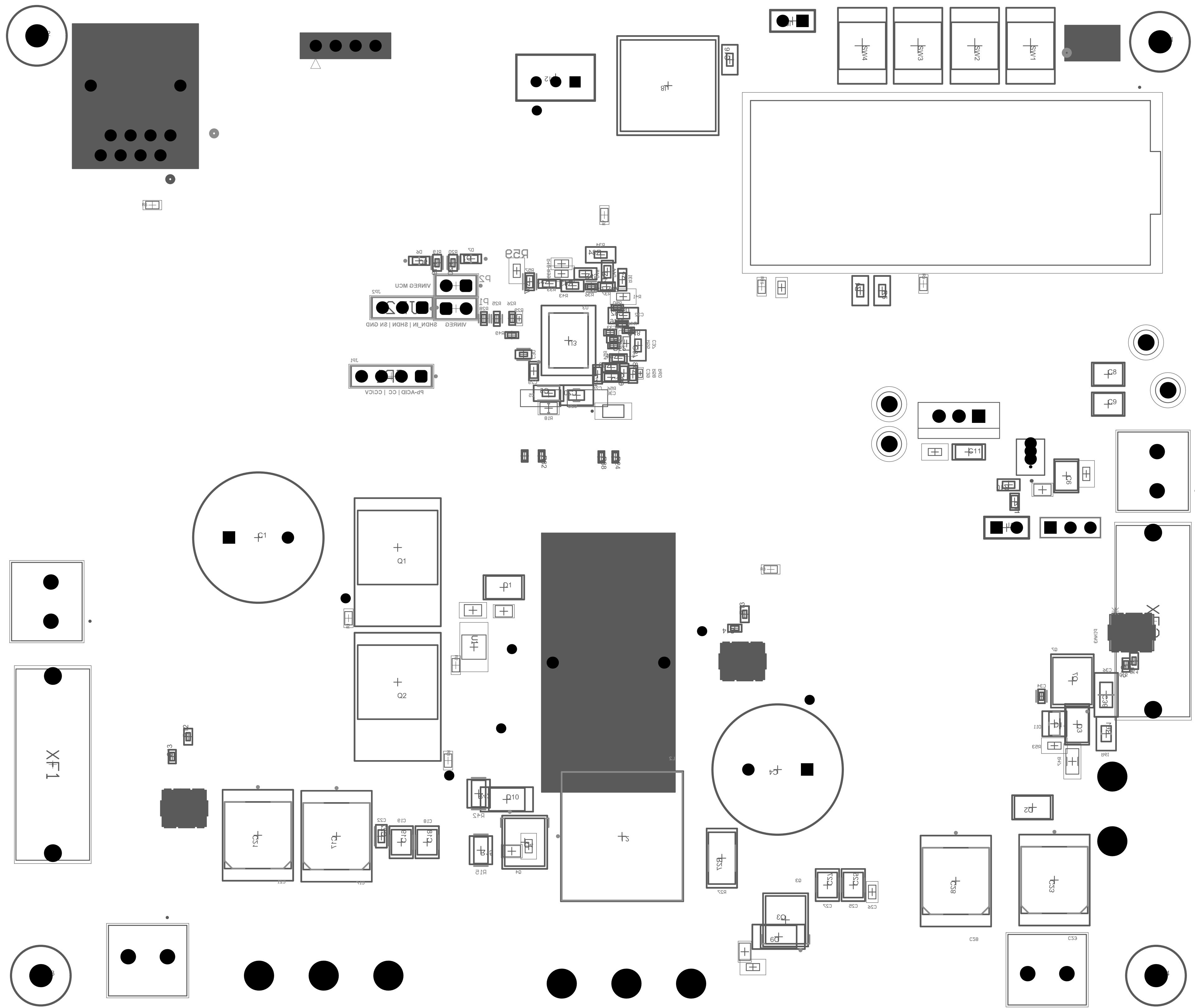


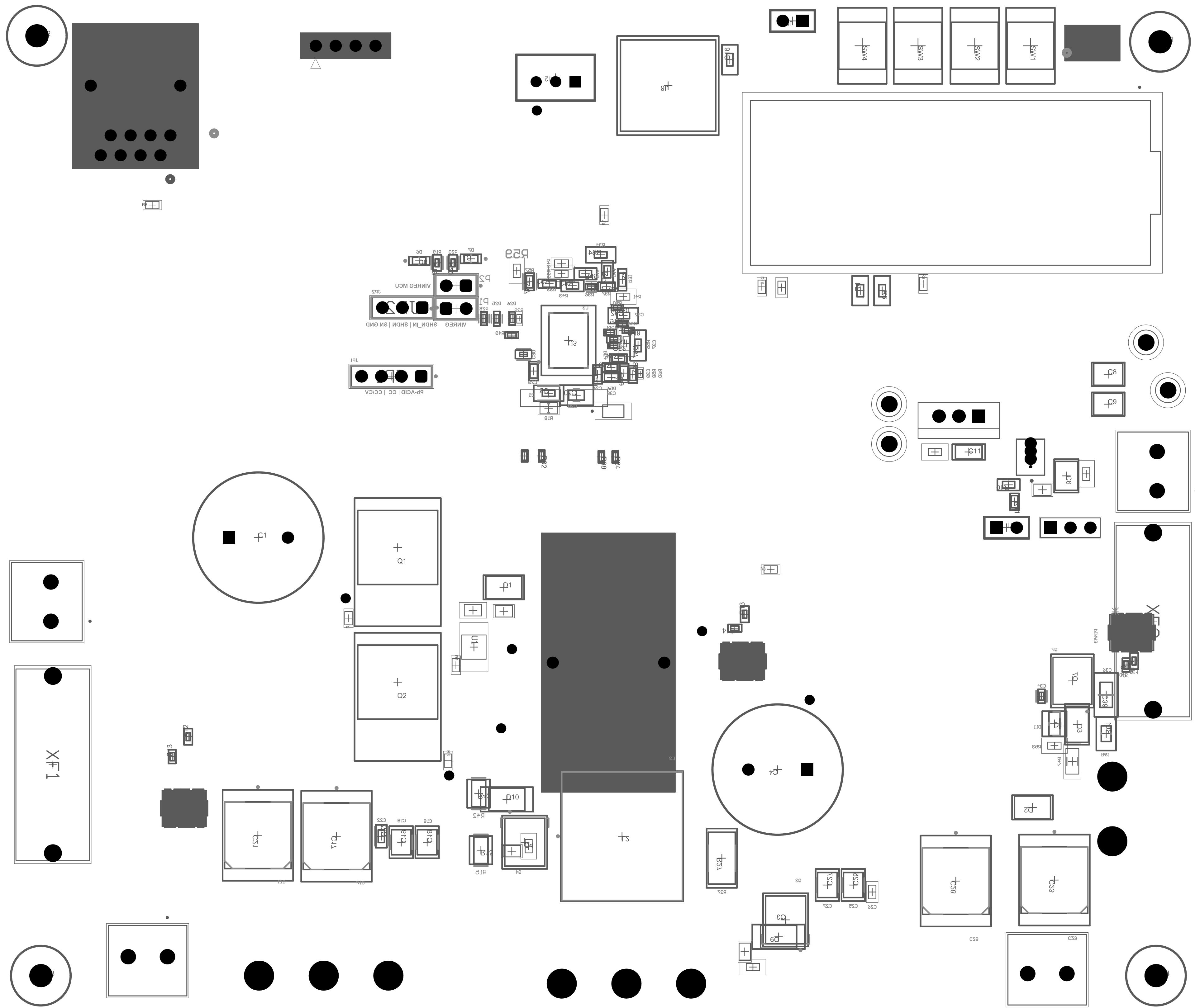
 **WPI**  
**MPPT MQP**

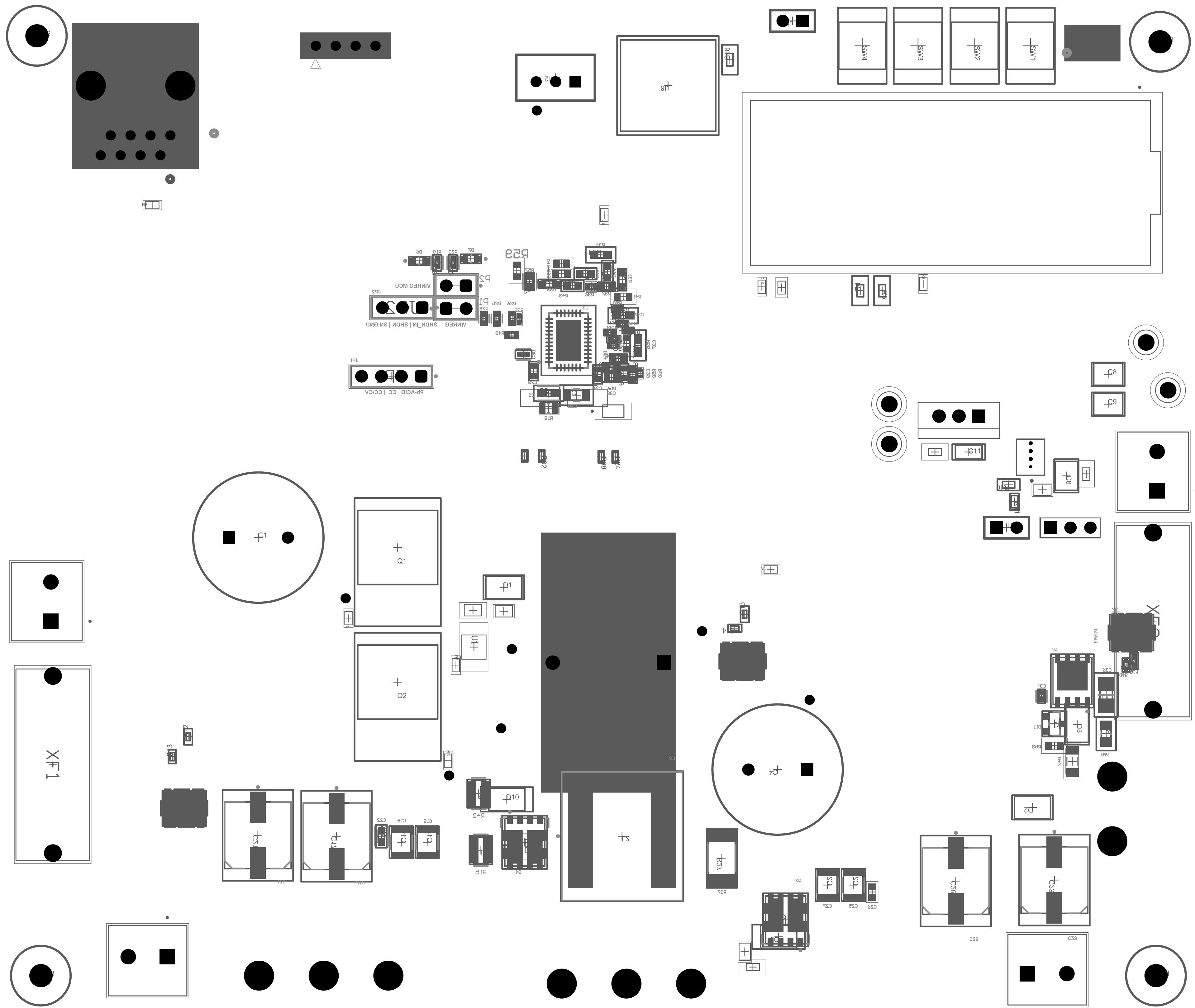


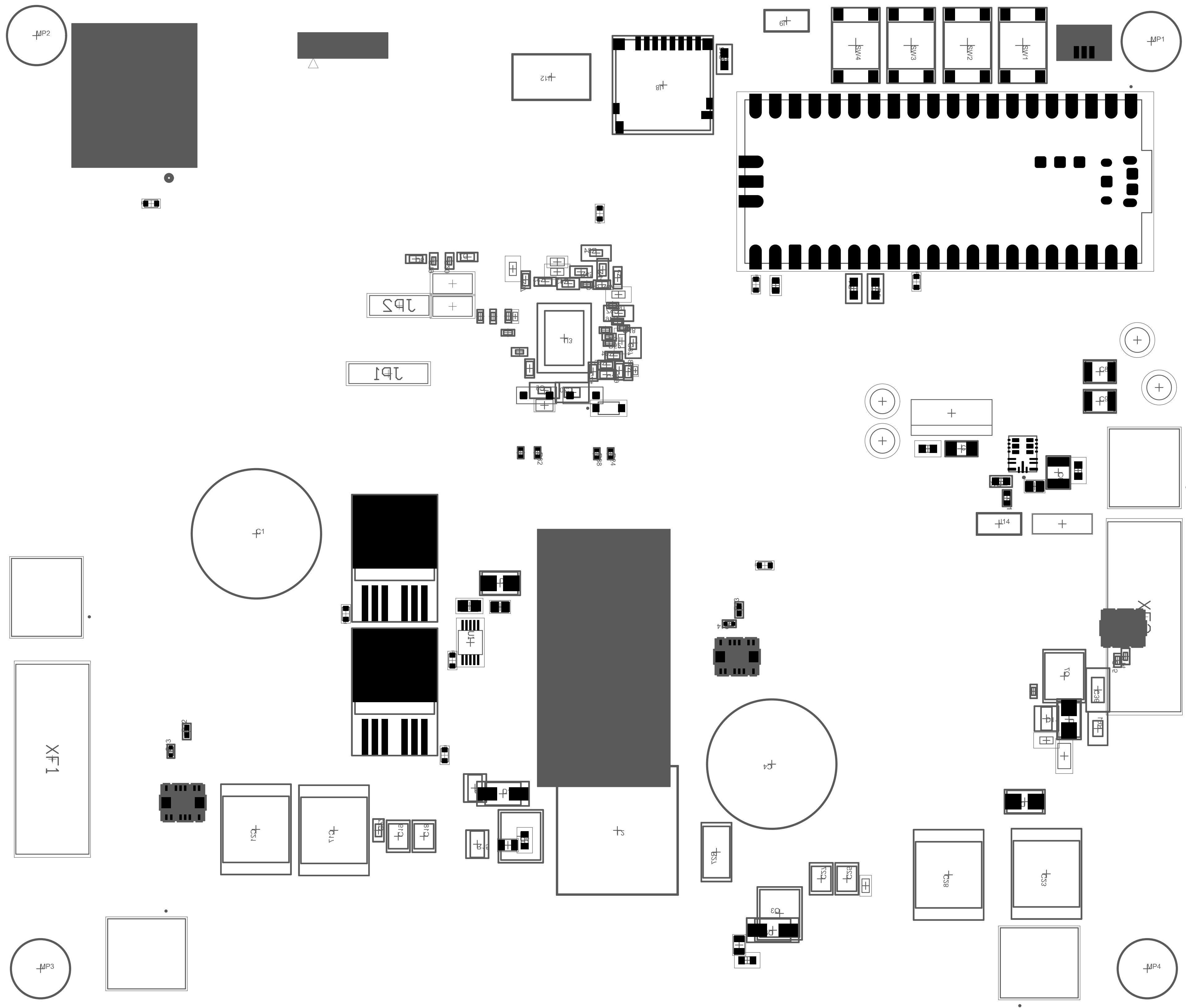
WPI  
MPPT MQP

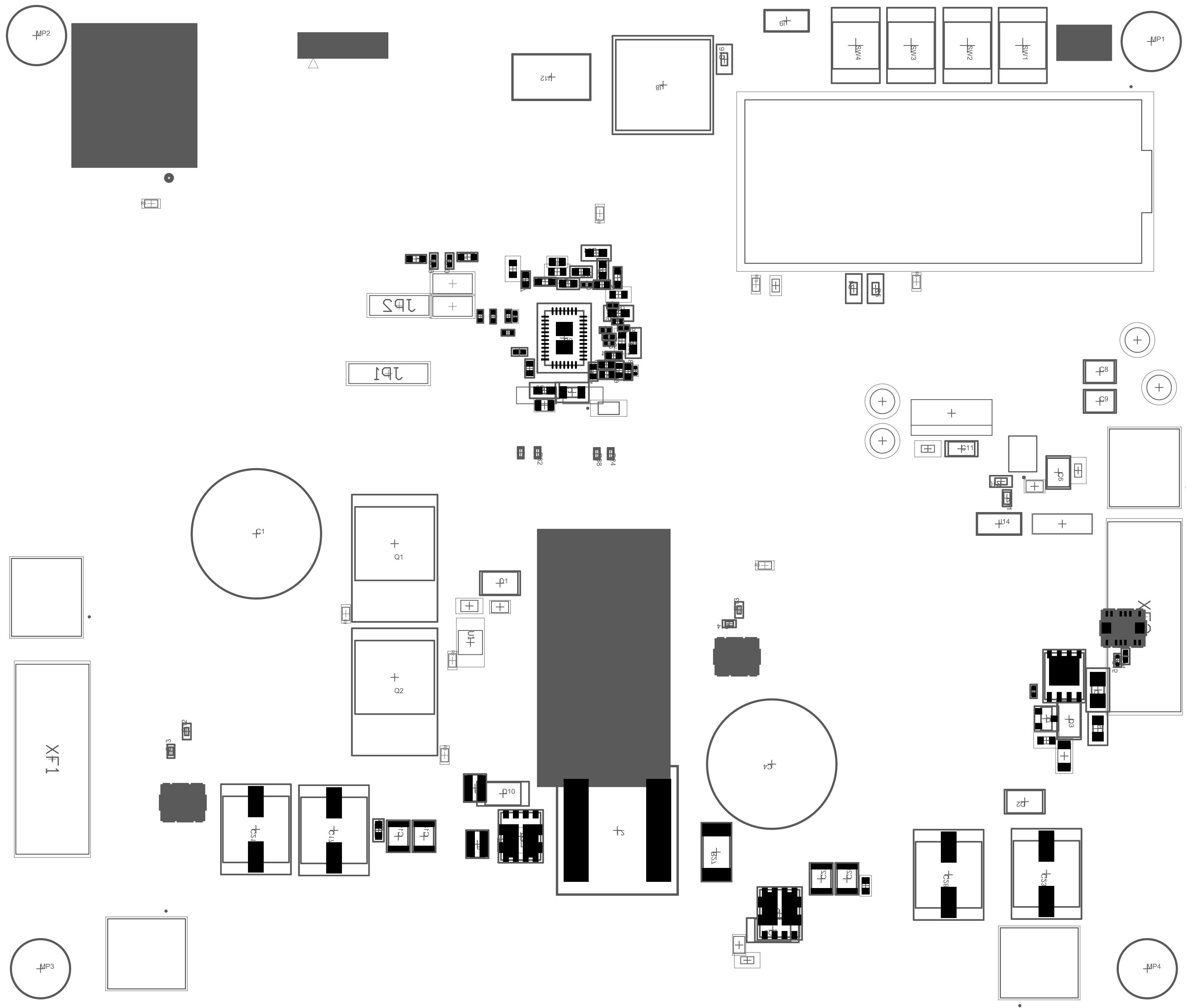


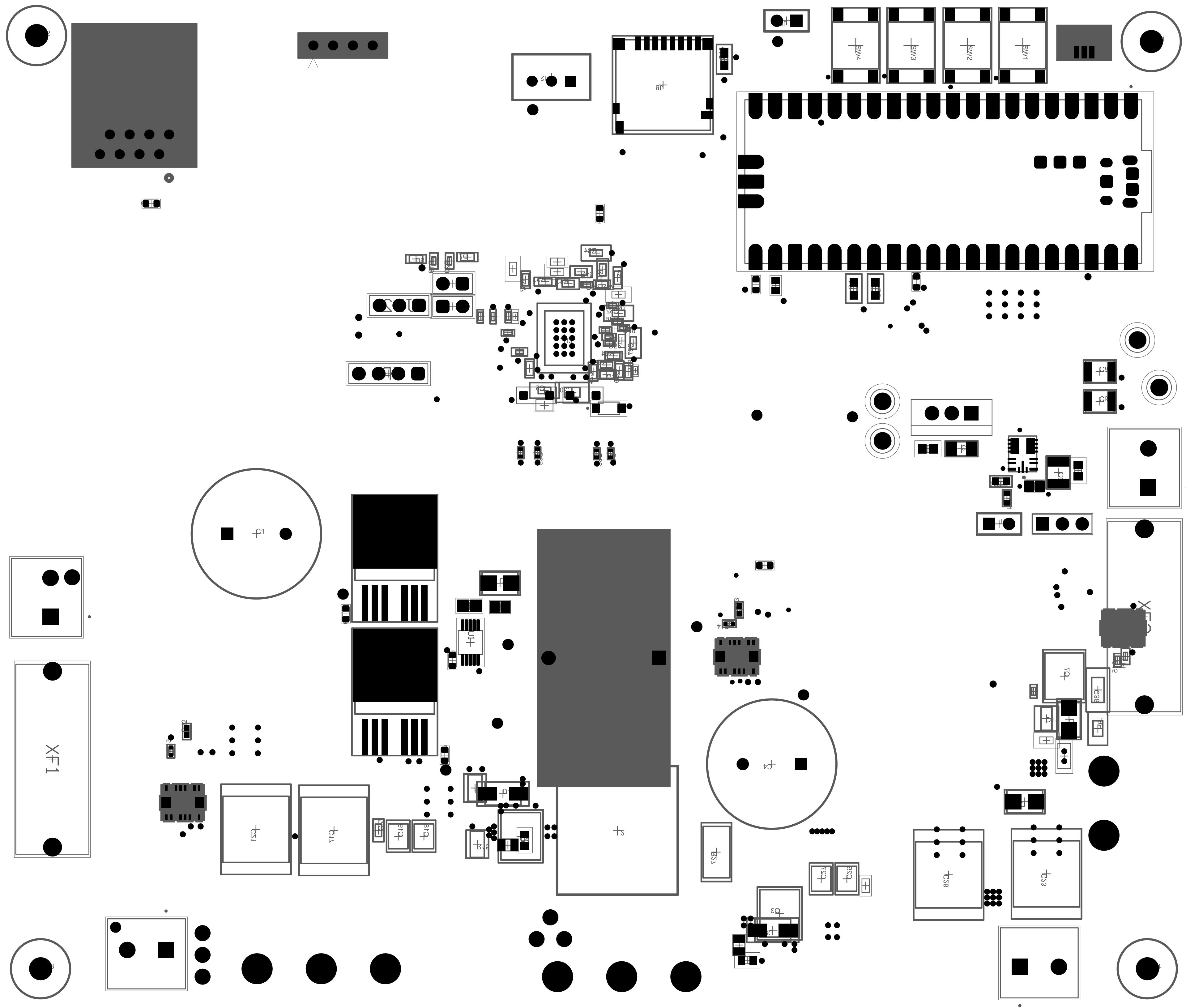


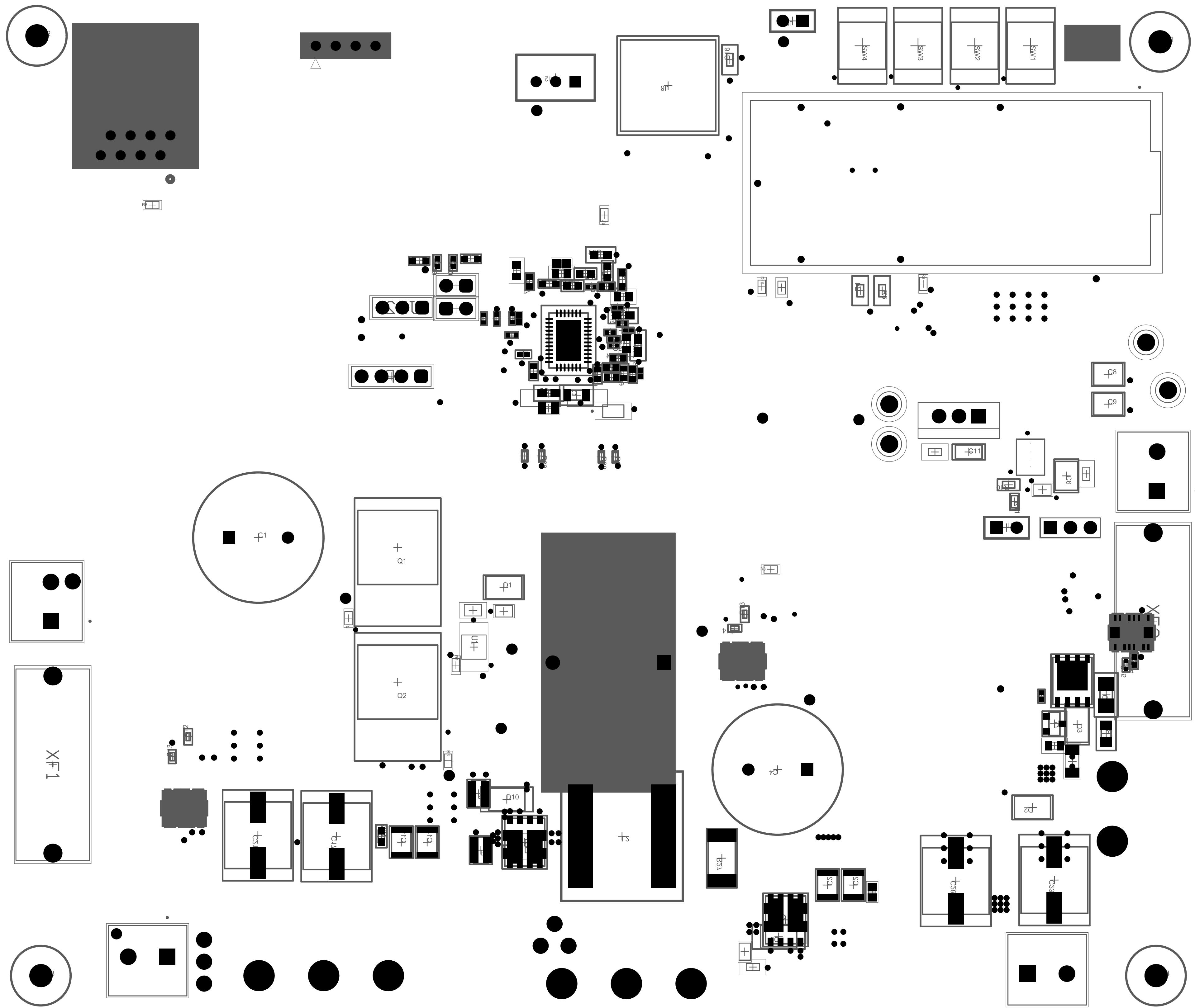


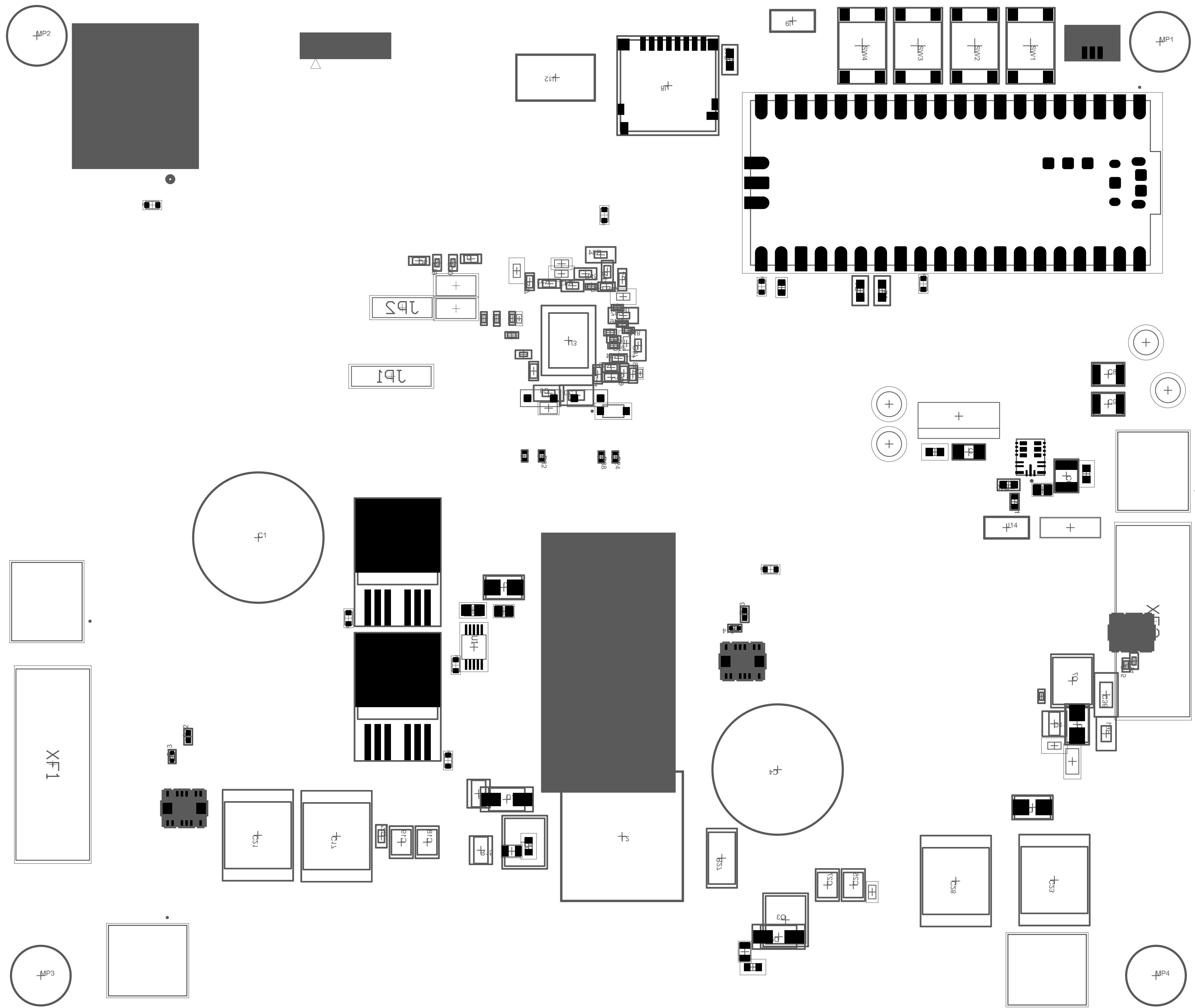


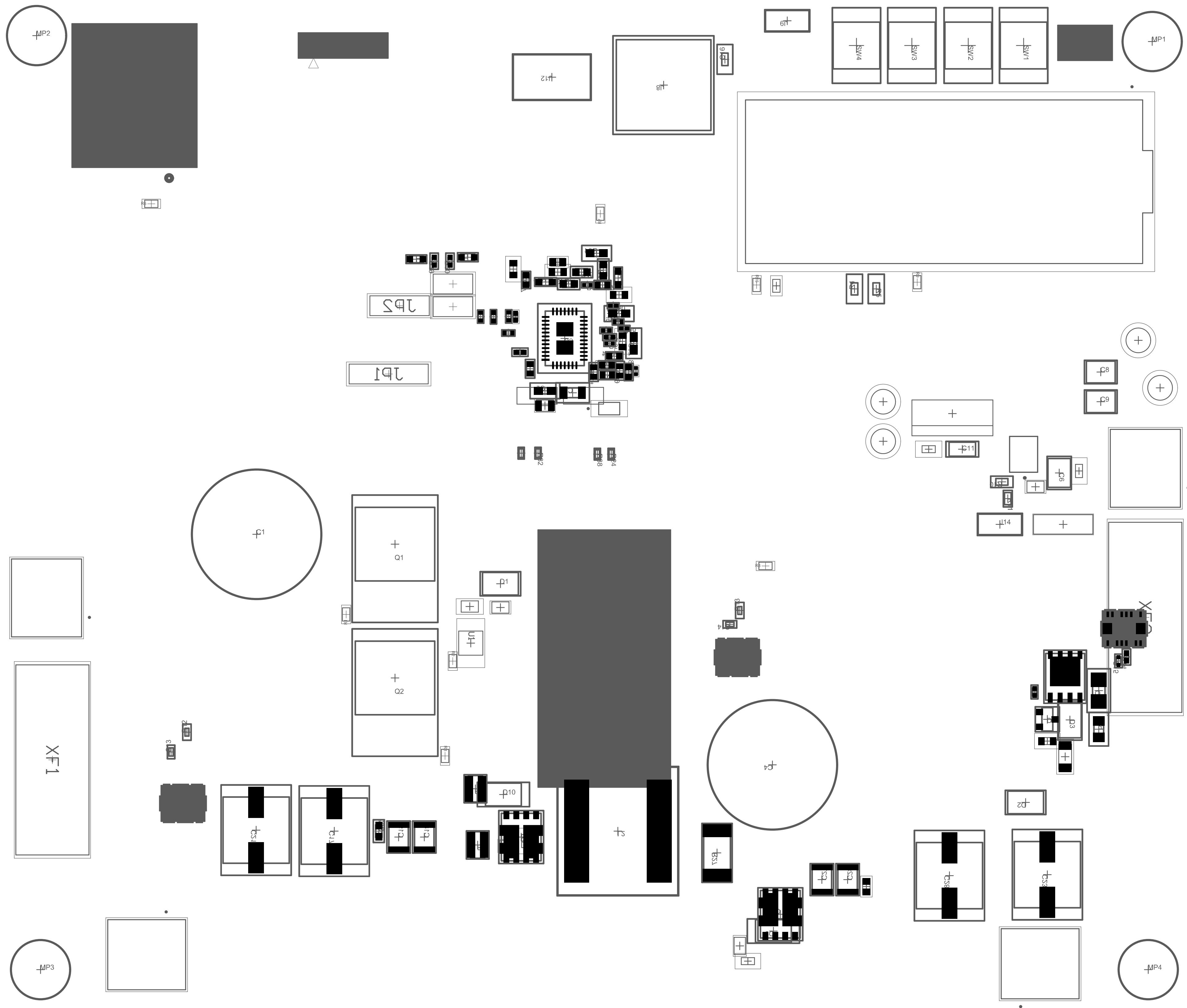


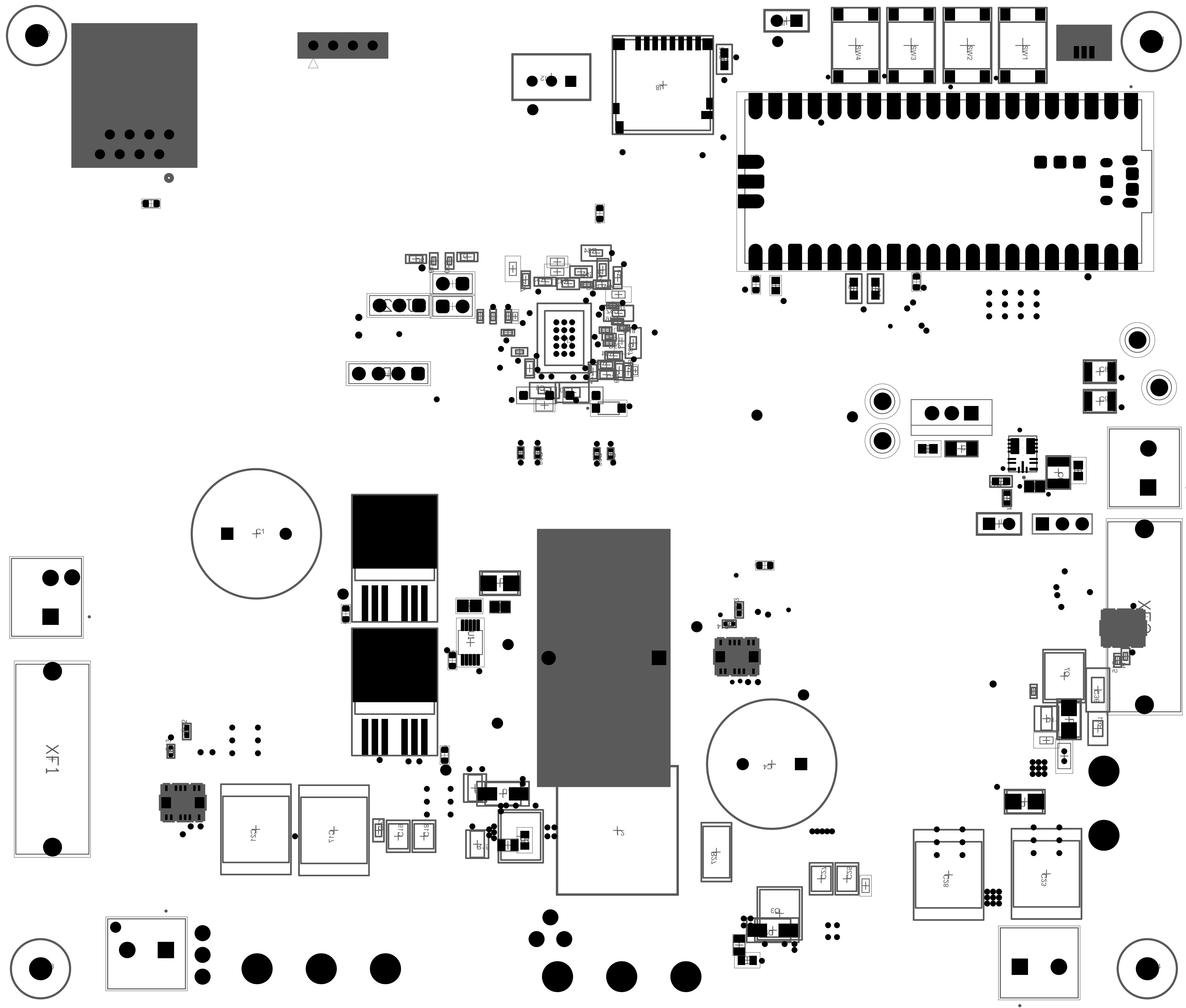


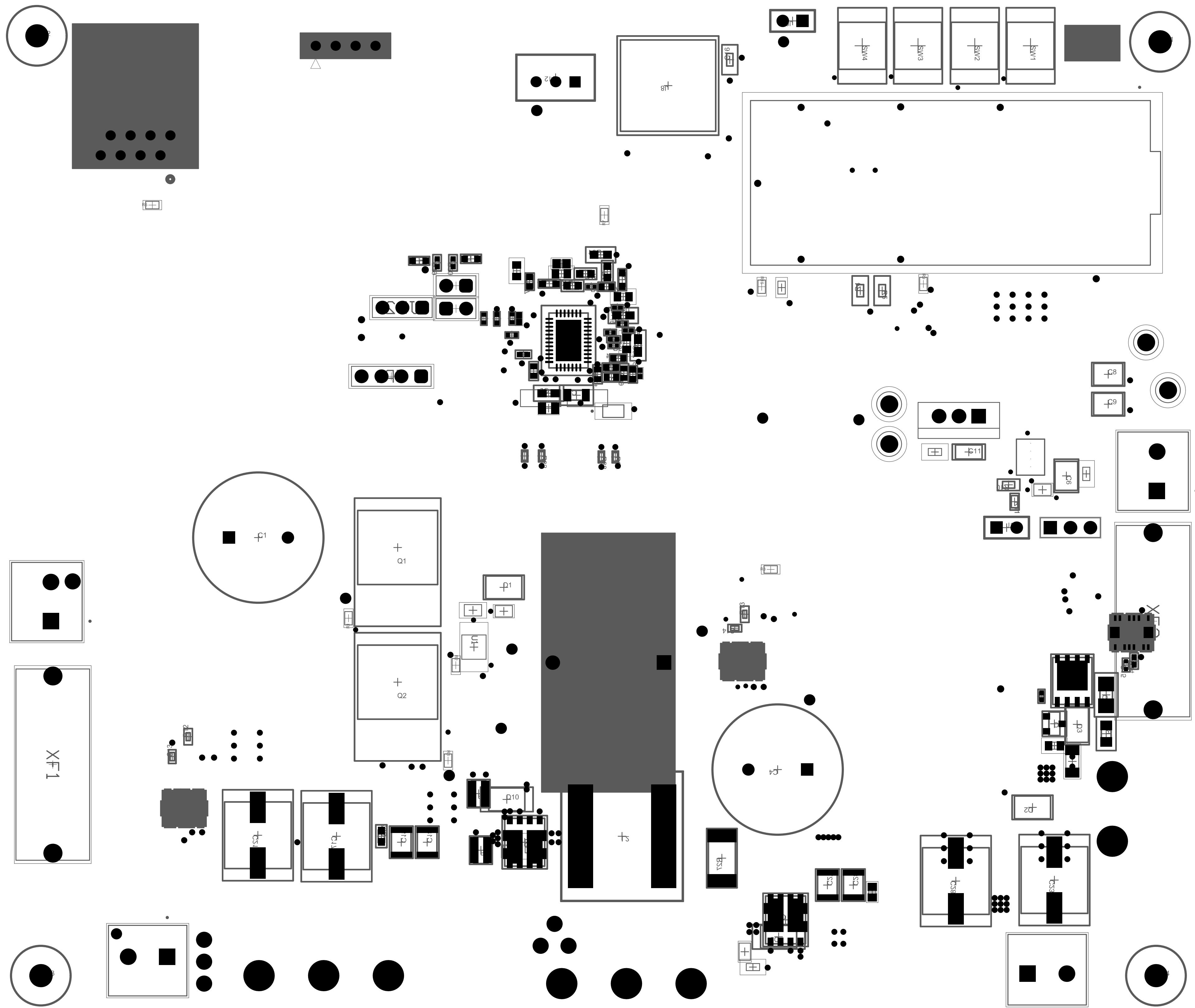














# Design Rules Verification Report

Filename : C:\Users\temp\Documents\WPI\MQP\Github\MPPT\_MQP\_PCB\MQP\_PCB\PCB\_

Warnings 0

Rule Violations 54

Warnings	
Total	0
Rule Violations	
Clearance Constraint (Gap=0mil) (InComponent('U4')), (InComponent('U4'))	0
Clearance Constraint (Gap=10mil) (WithinRoom('CHARGE_ROOM')), (All)	0
Clearance Constraint (Gap=10mil) (WithinRoom('GATE_DRIVER')), (All)	0
Clearance Constraint (Gap=5mil) (InComponent('U3')), (All)	0
Clearance Constraint (Gap=0mil) ((InNetClass('GateDriver') or InNet('GND')) and (Name like	0
Clearance Constraint (Gap=10mil) (All), (All)	0
Clearance Constraint (Gap=10mil) (InComponent('U1')), (All)	0
Clearance Constraint (Gap=10mil) (InComponent('U4')), (All)	0
Clearance Constraint (Gap=10mil) (All), (All)	0
Short-Circuit Constraint (Allowed=Yes)	0
SW(WithinRoom('GND_SIGNAL_SHORT')) (WithinRoom('GND_SIGNAL_SHORT'))	16
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=10mil) (Preferred=10mil) (All)	0
Width Constraint (Min=10mil) (Max=200mil) (Preferred=10mil) (InNet('SW'))	0
Width Constraint (Min=10mil) (Max=50mil) (Preferred=10mil) (All)	0
Routing Topology Rule(Topology=Shortest) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=150mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All), (All)	0
Minimum Solder Mask Sliver (Gap=3mil) (All), (All)	13
Silk To Solder Mask (Clearance=4mil) (IsPad), (All)	16
Silk to Silk (Clearance=6mil) (All), (All)	8
Net Antennae (Tolerance=0mil) (All)	1
Net Antennae (Tolerance=151mil) (WithinRoom('GND_SIGNAL_SHORT'))	0
Room GND_SIGNAL_SHORT (Bounding Region = (3830mil, 4230mil, 3870mil, 4405mil) (False)	0
Room GATE_DRIVER (Bounding Region = (3285mil, 2675mil, 3460mil, 2985mil) (False)	0
Room CHARGE_ROOM (Bounding Region = (3647.284mil, 4187.992mil, 4050mil, 4640mil) (False)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Height Constraint (Min=0mil) (Max=10000mil) (Preferred=5000mil) (InComponent('L1'))	0
Total	54

Short-Circuit Constraint (Allowed=No) (All),(All)
Short-Circuit Constraint: Between Pad J5-10(450mil,4670mil) on Multi-Layer And Polygon Region (134 hole(s)) GND2 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad J5-10(450mil,4670mil) on Multi-Layer And Polygon Region (150 hole(s)) GND1 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad J5-9(900mil,4670mil) on Multi-Layer And Polygon Region (134 hole(s)) GND2 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad J5-9(900mil,4670mil) on Multi-Layer And Polygon Region (150 hole(s)) GND1 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP1-(5820mil,4890mil) on Multi-Layer And Polygon Region (134 hole(s)) GND2 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP1-(5820mil,4890mil) on Multi-Layer And Polygon Region (150 hole(s)) GND1 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP1-(5820mil,4890mil) on Multi-Layer And Polygon Region (75 hole(s)) Bottom Layer Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP2-(180mil,4920mil) on Multi-Layer And Polygon Region (134 hole(s)) GND2 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP2-(180mil,4920mil) on Multi-Layer And Polygon Region (150 hole(s)) GND1 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP2-(180mil,4920mil) on Multi-Layer And Polygon Region (75 hole(s)) Bottom Layer Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP3-(200mil,200mil) on Multi-Layer And Polygon Region (134 hole(s)) GND2 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP3-(200mil,200mil) on Multi-Layer And Polygon Region (150 hole(s)) GND1 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP3-(200mil,200mil) on Multi-Layer And Polygon Region (75 hole(s)) Bottom Layer Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP4-(5800mil,200mil) on Multi-Layer And Polygon Region (134 hole(s)) GND2 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP4-(5800mil,200mil) on Multi-Layer And Polygon Region (150 hole(s)) GND1 Location : [X = 0mil][Y = 0mil]
Short-Circuit Constraint: Between Pad MP4-(5800mil,200mil) on Multi-Layer And Polygon Region (75 hole(s)) Bottom Layer Location : [X = 0mil][Y = 0mil]

Minimum Solder Mask Sliver (Gap=3mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (1.536mil < 3mil) Between Pad D10-2(2618.74mil,1085mil) on Top Layer And Via (2640mil,1135mil) from Top
Minimum Solder Mask Sliver Constraint: (1.52mil < 3mil) Between Pad R25-2(2490mil,3519.669mil) on Bottom Layer And Via (2490mil,3548mil) from Top
Minimum Solder Mask Sliver Constraint: (2.473mil < 3mil) Between Pad R26-2(2567mil,3520.685mil) on Bottom Layer And Via (2566mil,3548mil) from Top
Minimum Solder Mask Sliver Constraint: (1.874mil < 3mil) Between Pad R29-1(2602mil,3482.268mil) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (2.102mil < 3mil) Between Pad R30-1(3735mil,287.52mil) on Top Layer And Pad R35-2(3746.472mil,243mil) on
Minimum Solder Mask Sliver Constraint: (1.873mil < 3mil) Between Pad U1-1(2414.37mil,1937.598mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.873mil < 3mil) Between Pad U1-10(2414.37mil,1762.402mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.875mil < 3mil) Between Pad U1-2(2394.686mil,1937.598mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.873mil < 3mil) Between Pad U1-3(2375mil,1937.598mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.873mil < 3mil) Between Pad U1-4(2355.316mil,1937.598mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.875mil < 3mil) Between Pad U1-6(2335.63mil,1762.402mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.873mil < 3mil) Between Pad U1-7(2355.316mil,1762.402mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.875mil < 3mil) Between Pad U1-8(2375mil,1762.402mil) on Top Layer And Pad
U1-9(2394.686mil,1762.402mil)

Silk To Solder Mask (Clearance=4mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.35mil < 4mil) Between Arc (2700.155mil,3281.732mil) on Bottom Overlay And Pad C29-1(2675mil,3260mil)
Silk To Solder Mask Clearance Constraint: (3.016mil < 4mil) Between Pad C31-2(3093.873mil,3396mil) on Bottom Layer And Text "C31"
Silk To Solder Mask Clearance Constraint: (3.15mil < 4mil) Between Pad C32-1(3157.548mil,3515mil) on Bottom Layer And Text "C32"
Silk To Solder Mask Clearance Constraint: (2.008mil < 4mil) Between Pad D8-C(3010.039mil,3035mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (2.678mil < 4mil) Between Pad PINA1-1(837.322mil,967.166mil) on Top Layer And Text "***"
Silk To Solder Mask Clearance Constraint: (2.785mil < 4mil) Between Pad PINA1-2(860.944mil,967.166mil) on Top Layer And Text "***"
Silk To Solder Mask Clearance Constraint: (2.678mil < 4mil) Between Pad PINA2-1(3641.322mil,1705.166mil) on Top Layer And Text "***"
Silk To Solder Mask Clearance Constraint: (2.785mil < 4mil) Between Pad PINA2-2(3664.944mil,1705.166mil) on Top Layer And Text "***"
Silk To Solder Mask Clearance Constraint: (2.678mil < 4mil) Between Pad PINA3-1(5595.512mil,1995.668mil) on Bottom Layer And Text "***"
Silk To Solder Mask Clearance Constraint: (2.785mil < 4mil) Between Pad PINA3-2(5619.134mil,1995.668mil) on Bottom Layer And Text "***"
Silk To Solder Mask Clearance Constraint: (3.79mil < 4mil) Between Pad R30-2(3735mil,352.48mil) on Top Layer And Text "R30"
Silk To Solder Mask Clearance Constraint: (3.317mil < 4mil) Between Pad R41-1(3095mil,3610mil) on Bottom Layer And Text "R50"
Silk To Solder Mask Clearance Constraint: (2.916mil < 4mil) Between Pad R46-1(3137.716mil,3473mil) on Bottom Layer And Text "R46"
Silk To Solder Mask Clearance Constraint: (2.191mil < 4mil) Between Pad R46-2(3102.284mil,3473mil) on Bottom Layer And Text "R48"
Silk To Solder Mask Clearance Constraint: (1.953mil < 4mil) Between Pad R52-2(3092.833mil,3364mil) on Bottom Layer And Text "R52"
Silk To Solder Mask Clearance Constraint: (1.317mil < 4mil) Between Pad R55-1(3142mil,3404.528mil) on Bottom Layer And Text "C31"

Silk to Silk (Clearance=6mil) (All), (All)
Silk To Silk Clearance Constraint: (Collision < 6mil) Between Arc (2401.968mil,2150mil) on Top Overlay And Text "C2" (2300.016mil,2085.01mil) on Top
Silk To Silk Clearance Constraint: (2.853mil < 6mil) Between Arc (3900mil,1235mil) on Top Overlay And Text "PINA2" (3610.044mil,1570.01mil) on Top
Silk To Silk Clearance Constraint: (3.773mil < 6mil) Between Text "***" (3666.323mil,1653.665mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.773mil < 6mil) Between Text "***" (5620.513mil,2047.169mil) on Bottom Overlay And Track
Silk To Silk Clearance Constraint: (3.773mil < 6mil) Between Text "***" (862.323mil,915.665mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.177mil < 6mil) Between Text "C33" (3084.994mil,3447.502mil) on Bottom Overlay And Text "R48"
Silk To Silk Clearance Constraint: (1.626mil < 6mil) Between Text "R11" (4982.511mil,2545.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.491mil < 6mil) Between Text "R36" (2974.994mil,3612.502mil) on Bottom Overlay And Track

Net Antennae (Tolerance=0mil) (All)
Net Antennae: Via (3930mil,4890mil) from Top Layer to Bottom Layer

## Electrical Rules Check Report

Class	Document	Message
Error	MCU.SchDoc	3.3V contains Output Pin and Power Pin objects (Pin U2-36, Pin J8-4, Pin PINA1-11, Pin PINA2-11, Pin PINA3-11).
Error	Voltage Regulator.SchDoc	Net NetD3_1 contains multiple Input Ports (Port VBAT, Port VBAT).
Error	Connectors.SchDoc	Net NetJ5_3 contains multiple Input Ports (Port I2C1_SCL, Port I2C1_SCL).
Error	FCC Footprint Charge Controller.SchDoc	Net NetP2_1 has only one pin (Pin P2-1)
Error	Power Monitor.SchDoc	Net NetPINA1_6 contains multiple Input Ports (Port I2C0_SCL, Port I2C0_SCL, Port I2C0_SCL).
Error	MCU.SchDoc	Net NetU2_17 has only one pin (Pin U2-17)
Error	Connectors.SchDoc	Net VIN contains multiple Input Ports (Port Charge PV, Port Charge PV).
Warning	DC-DC Converter.SchDoc	Net NetC2_2 has no driving source (Pin C2-2, Pin D1-1, Pin U1-2)
Warning	DC-DC Converter.SchDoc	Net NetQ1_1 has no driving source (Pin Q1-1, Pin R1-2, Pin Test1-IN)
Warning	DC-DC Converter.SchDoc	Net NetQ2_1 has no driving source (Pin Q2-1, Pin R3-2, Pin Test5-IN)
Warning	DC-DC Converter.SchDoc	Net NetR2_2 has no driving source (Pin R2-2, Pin U1-6)
Warning	DC-DC Converter.SchDoc	Net SW has no driving source (Pin C2-1, Pin L1-2, Pin Q1-2, Pin Q1-3, Pin Q1-5, Pin Q1-6, Pin Q1-7, Pin Q2-8, Pin Test6-IN, Pin U1-4)
Warning	Connectors.SchDoc	NetD2_2 contains IO Pin and Input Port objects (Pin J3-3, Port VBAT_Buck).
Warning	Connectors.SchDoc	NetD2_2 contains IO Pin and Output Port objects (Pin J3-3, Port VBAT_Buck).
Warning	Connectors.SchDoc	NetJ2_1 contains IO Pin and Input Port objects (Pin J2-1, Pin J3-1, Port Charge PV).
Warning	Connectors.SchDoc	NetJ2_1 contains IO Pin and Output Port objects (Pin J2-1, Pin J3-1, Port Charge PV, Port Charge PV).
Warning	Connectors.SchDoc	NetJ2_2 contains IO Pin and Input Port objects (Pin J2-2, Port -PV).
Warning	Connectors.SchDoc	NetJ2_3 contains IO Pin and Output Port objects (Pin J2-3, Port PV Buck).
Warning	Connectors.SchDoc	NetJ3_2 contains IO Pin and Input Port objects (Pin J3-2, Port -V_Buck).
Warning	Connectors.SchDoc	NetJ8_2 contains IO Pin and Input Port objects (Pin J8-2, Port SD CS).
Warning	Connectors.SchDoc	NetJ8_3 contains IO Pin and Input Port objects (Pin J8-3, Port SD MOSI).
Warning	Connectors.SchDoc	NetJ8_7 contains IO Pin and Output Port objects (Pin J8-7, Port SD MISO).
Warning	MCU.SchDoc	NetJ12_3 contains Input Port and Unspecified Port objects (Port ADC0, Port ADC0).
Warning	MCU.SchDoc	NetR5_1 contains IO Pin and Output Port objects (Pin U2-27, Port I2C0_SCL).
Warning	MCU.SchDoc	NetTest8_IN contains IO Pin and Input Port objects (Pin U2-31, Port ADC0).
Warning	MCU.SchDoc	NetU2_15 contains IO Pin and Output Port objects (Pin U2-15, Port I2C1_SCL).
Warning	MCU.SchDoc	NetU2_21 contains IO Pin and Input Port objects (Pin U2-21, Port SD MISO).
Warning	MCU.SchDoc	NetU2_22 contains IO Pin and Output Port objects (Pin U2-22, Port SD CS).
Warning	MCU.SchDoc	NetU2_24 contains IO Pin and Output Port objects (Pin U2-24, Port SD SCK).
Warning	MCU.SchDoc	NetU2_25 contains IO Pin and Output Port objects (Pin U2-25, Port SD MOSI).
Warning	MCU.SchDoc	NetU2_32 contains IO Pin and Output Port objects (Pin U2-32, Port GATEDRIVE EN).
Warning	MCU.SchDoc	NetU2_34 contains IO Pin and Output Port objects (Pin U2-34, Port PWM DC).
Warning	FCC Footprint Charge Controller.SchDoc	Off grid Net Label BG1 at 10537.325mil,8600mil
Warning	DC-DC Converter.SchDoc	Off grid Pin Q2-1 at 137.16mm,80.01mm
Warning	DC-DC Converter.SchDoc	Off grid Pin Q2-2 at 147.32mm,69.85mm
Warning	DC-DC Converter.SchDoc	Off grid Pin Q2-3 at 149.86mm,69.85mm
Warning	DC-DC Converter.SchDoc	Off grid Pin Q2-5 at 152.4mm,69.85mm
Warning	DC-DC Converter.SchDoc	Off grid Pin Q2-6 at 154.94mm,69.85mm
Warning	DC-DC Converter.SchDoc	Off grid Pin Q2-7 at 157.48mm,69.85mm
Warning	DC-DC Converter.SchDoc	Off grid Pin Q2-8 at 147.32mm,87.63mm
Warning	DC-DC Converter.SchDoc	Off grid Pin R3-2 at 125.73mm,80.01mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-1 at 59.69mm,91.44mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-2 at 85.09mm,106.68mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-3 at 85.09mm,101.6mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-4 at 85.09mm,96.52mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-5 at 59.69mm,86.36mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-6 at 59.69mm,96.52mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-7 at 59.69mm,101.6mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-8 at 59.69mm,106.68mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-9 at 85.09mm,86.36mm
Warning	DC-DC Converter.SchDoc	Off grid Pin U1-10 at 85.09mm,91.44mm
Warning	Power Monitor.SchDoc	Off grid Port I2C0_SCL at 3210.582mil,2800mil
Warning	Power Monitor.SchDoc	Off grid Port I2C0_SCL at 3210.582mil,4400mil
Warning	Power Monitor.SchDoc	Off grid Port I2C0_SCL at 3210.582mil,5900mil
Warning	MCU.SchDoc	Off grid Port I2C0_SCL at 8110.582mil,2700mil

Class	Document	Message
Warning	MCU.SchDoc	Off grid Port I2C0_SDA at 1894.621mil,2800mil
Warning	Power Monitor.SchDoc	Off grid Port I2C0_SDA at 3194.621mil,2900mil
Warning	Power Monitor.SchDoc	Off grid Port I2C0_SDA at 3194.621mil,4500mil
Warning	Power Monitor.SchDoc	Off grid Port I2C0_SDA at 3194.621mil,6000mil
Warning	MCU.SchDoc	Off grid Port PWM DC at 7939.374mil,3400mil
Warning	Voltage Regulator.SchDoc	Off grid Port VBAT at 856.437mil,6700mil
Warning	MCU.SchDoc	Off grid Power Object GND at 1220.503mil,1100mil
Warning	DC-DC Converter.SchDoc	Off grid Q2 at 137.16mm,80.01mm
Warning	DC-DC Converter.SchDoc	Off grid U1 at 64.77mm,109.22mm
Warning	FCC Footprint Charge Controller.SchDoc	Unconnected line (13200mil,5500mil) To (13200mil,5600mil)
Warning	FCC Footprint Charge Controller.SchDoc	Unconnected line (14200mil,4100mil) To (14300mil,4100mil)
Warning	FCC Footprint Charge Controller.SchDoc	Unconnected line (15500mil,3400mil) To (15500mil,3500mil)

