

Geometry-Aware Plasticity: Thermodynamic Weight Updates in Non-Euclidean Hardware

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Abstract

Current neuromorphic architectures rely on standard, local learning rules (e.g., Spike-Timing-Dependent Plasticity) that operate blindly within static, Euclidean geometries. While energy-efficient for local exploration, these rules fail to overcome topological local minima without relying on the massive thermodynamic bloat of standard backpropagation. Building upon the Metabolic Phase Transition (MPT)[10] and the Curvature Adaptation Hypothesis (CAH)[8], we introduce **Geometry-Aware Plasticity** (GAP): a biologically plausible learning algorithm designed for dynamically gated analog hardware.

GAP utilizes the instantaneous Riemannian curvature (κ) of the network, governed by the apical-somatic conductance ratio (γ), to modulate synaptic plasticity. When the system detects a local minimum, it triggers a macroscopic “Hyperbolic Plunge,” exponentially amplifying connection growth along geodesic pathways.

To translate this continuous thermodynamic theory into viable Very Large-Scale Integration (VLSI), we introduce three strict hardware constraints:

1. A **Schmitt-trigger hysteretic shield** to immunize the learning phase against thermal noise,
2. An **asymmetric gain function** to protect the Euclidean baseline from catastrophic forgetting, and
3. A **physical saturation governor** to prevent memristive oxide burnout.

Using a PyTorch digital twin of the Manifold Chip architecture[9], we empirically demonstrate that GAP successfully forces a structural phase transition, forging a persistent geodesic pathway to route around local minima while strictly obeying physical hardware limits.

1 Introduction

The fundamental pursuit of neuromorphic engineering is to replicate the extraordinary thermodynamic efficiency of the biological brain[7]. To achieve this, modern architectures heavily rely on local, unsupervised learning rules, such as Spike-Timing-Dependent Plasticity (STDP) or Hebbian variants[1, 2]. Because these rules update synaptic weights using only information locally available at the pre- and post-synaptic terminals, they are highly energy-efficient. However, when deployed within static, flat topologies (where the Riemannian curvature $\kappa \approx 0$), local learning rules are entirely blind to the macroscopic structure of the problem space. When a network encounters a deep topological local minimum, local learning cannot coordinate the global structural adjustments required to escape[6].

Traditional artificial neural networks (ANNs) bypass this limitation using backpropagation, forcefully routing global error gradients backwards through the system. While mathematically effective at escaping local minima, backpropagation violates the physical locality of real hardware. It requires symmetric weight transport, distinct forward and backward phases, and massive memory overhead, ultimately driving the system into a thermodynamic “Landauer Wall”

of energy bloat[4]. The field thus faces a critical paradox: learning must be physically local to remain thermodynamically efficient, but it must possess global awareness to solve complex, high-dimensional tasks.

In our previous work establishing the Metabolic Phase Transition (MPT)[10] and the Curvature Adaptation Hypothesis (CAH)[8], we proposed that biological systems resolve this paradox not through non-local mathematics, but through dynamic geometry. Rather than changing the learning rule, the brain changes the shape of the manifold itself. By regulating the apical-somatic conductance ratio (γ) via the Martinotti-subtype of Somatostatin (SST) interneurons, the network can transiently unlock a latent hyperbolic geometry. This phase transition from a Euclidean regime ($\kappa \approx 0$) to a deep hyperbolic regime ($\kappa < 0$) fundamentally warps the distance between nodes, collapsing the distance required to route around a problem space.

Building upon the hardware framework of the Manifold Chip—a Dynamically Gated Analog Crossbar (DGAC) designed to replicate this topological switch in silicon[9]—this paper introduces Geometry-Aware Plasticity (GAP). GAP provides the formal learning algorithm required to drive this physical architecture. By mathematically coupling traditional local STDP to the macroscopic curvature state of the network, GAP allows the hardware to quietly explore via low-energy Euclidean adjustments, and to violently break out of local minima by initiating a targeted “structural burn” along hyperbolic geodesic pathways. Crucially, to ensure viability in physical analog hardware, we demonstrate how this algorithm must be strictly constrained by device physics, incorporating a Schmitt-trigger hysteretic shield, asymmetric geometric gain, and strict memristive oxide saturation bounds.

2 The Biophysical Actuator and the Geometric Multiplier

To design a hardware-compatible learning rule that mathematically links synaptic weight updates to macroscopic network geometry, we must first abstract the biophysical mechanism the brain uses to control this transition.

Cortical microcircuits rely on a delicate balance of interneurons to gate information flow. Under baseline conditions (the “untrained” or exploratory state), Somatostatin-expressing (SST/SOM+) interneurons actively shunt the distal apical dendrites of pyramidal cells. This shunting heavily restricts the integration of global contextual signals, keeping the apical-somatic conductance ratio (γ) low. In this state, the local somatic integration results in minor Post-Synaptic Potentials (PSPs) on the order of 2–5 mV. Topologically, the network is restricted to a flat, Euclidean geometry ($\kappa \approx 0$), making it highly energy-efficient but prone to becoming trapped in local minima.

While local auto-regulation provides thermodynamic efficiency, the network’s global capacity to escape local minima is governed by the Top-Down VIP Override. This mechanism is the silicon analog to global Vasoactive Intestinal Peptide (VIP) interneuron disinhibition, a process recently characterized by Zhang et al. (2024)[12] as a learning-dependent gate for hierarchical inputs. In the GAP framework, this disinhibition releases the somatic ‘brake’, enabling the high-conductance state ($\gamma \rightarrow 1$) required to ignite the hyperbolic phase transition.

When the network encounters an error gradient it cannot resolve locally, a distinct biological override is triggered via Vasoactive Intestinal Peptide-expressing (VIP+) interneurons. VIP+ neurons strongly inhibit the SST+ and PV+ (Parvalbumin) interneurons. This disinhibition releases the somatic “brake,” rapidly driving the conductance ratio $\gamma \rightarrow 1$. This physiological event causes a massive depolarizing shift, generating PSPs in the 5–10 mV range. As established in the CAH, this specific high-conductance regime unlocks the network’s latent tree-like structure, driving the instantaneous Riemannian curvature (κ) into a deeply negative, hyperbolic state ($\kappa < 0$).

We translate these two distinct biological states into Geometry-Aware Plasticity (GAP) by introducing a dynamic geometric multiplier, $\Phi(\gamma, \kappa)$, to modify the baseline Euclidean gradient

update (ΔW_{STDP}).

The GAP weight update is defined as:

$$\Delta W_{ij}^{\text{GAP}} = \eta \cdot \Delta W_{ij}^{\text{STDP}} \cdot \Phi(\gamma, \kappa) \quad (1)$$

Where the geometric multiplier is formulated as:

$$\Phi(\gamma, \kappa) = 1 + \alpha \cdot \sigma_H(\gamma - \gamma_c) \cdot \exp(-\beta \kappa_{ij}) \quad (2)$$

Here, the algorithm seamlessly transitions between the two biophysical states:

The Euclidean Baseline (Tinkering Phase): When the network is exploring a local minimum ($\gamma < \gamma_c$), the hysteretic activation function σ_H evaluates to 0. The multiplier simplifies to exactly 1. The network strictly utilizes the baseline, low-energy ΔW_{STDP} to make minor, localized adjustments (mimicking the 2–5 mV state).

The Hyperbolic Plunge (Structural Burn): When the diagnostic circuit detects stagnation, it forces γ past the critical threshold ($\gamma_c \approx 0.78$). The activation function snaps to 1. Because the phase transition drives curvature deeply negative ($\kappa < 0$), the topological scaling factor $\exp(-\beta \kappa)$ violently amplifies the local learning rate. This mimics the 5–10 mV depolarization, burning a high-conductance geodesic shortcut across the manifold.

By routing the learning rate through this mathematically defined biophysical actuator, GAP ensures that extreme thermodynamic energy is strictly reserved for moments of macroscopic structural reorganization.

3 Hardware Realities and Constraints

Translating the continuous geometric multiplier $\Phi(\gamma, \kappa)$ into a functional analog Very Large-Scale Integration (VLSI) architecture introduces severe physical challenges. Raw analog hardware is unforgiving; without strict thermodynamic boundaries, the continuous equations of hyperbolic expansion will result in catastrophic system failure. To ensure the Manifold Chip can physically execute Geometry-Aware Plasticity (GAP) without destroying its own circuitry or memory, we enforce three critical hardware constraints.

3.1 The Hysteretic Shield (Thermal Noise Immunity)

In a biological or analog circuit, the boundary between the 2–5 mV baseline state and the 5–10 mV disinhibited state is not a mathematically perfect line. As demonstrated by Larkum et al. (1999)[5], the transition from local somatic integration to a global dendritic plateau is a discrete physiological event—a “switch” that couples the apical and basal compartments. However, in physical silicon, this boundary is subject to thermodynamic noise ($k_B T$).

If GAP utilized a standard Heaviside step function $\Theta(\gamma - \gamma_c)$ as the VIP trigger, local voltage hovering near the critical threshold would cause the Field Effect Transistor (FET) shunts to chatter at high frequencies. As characterized by the stochastic models of Shouval et al. (2002)[11] and the in vivo membrane potential dynamics of Gentet et al. (2012)[3], these thresholds are naturally noisy. To immunize the learning algorithm against thermal jitter, GAP replaces the Heaviside step with a hysteretic sigmoid function, $\sigma_H(\gamma - \gamma_c)$. Operating identically to a physical Schmitt trigger, this creates a state-dependent activation threshold. Once γ exceeds the upper boundary ($\gamma > 0.78$), the multiplier “snaps” open and mathematically locks the learning phase until the local voltage definitively cools below a separate, lower threshold ($\gamma < 0.40$). This shield ensures the structural burn is a deliberate, sustained event rather than a mistake caused by noise.

3.2 Asymmetric Gain (Preventing Catastrophic Forgetting)

Standard STDP exhibits both Long-Term Potentiation (LTP, where $\Delta W > 0$) and Long-Term Depression (LTD, where $\Delta W < 0$). During a hyperbolic plunge, the network topology expands exponentially, driving $\kappa \ll 0$. If the geometric multiplier Φ amplified all weight updates symmetrically, the resulting exponential LTD would indiscriminately prune non-active pathways, resulting in catastrophic forgetting of the network’s foundational Euclidean knowledge. GAP mitigates this by enforcing an asymmetric amplification mask. The hyperbolic gain is exclusively applied to potentiation (building the new geodesic shortcut), while depression (pruning) is decoupled from the geometric multiplier and suppressed by a fractional dampening constant (ϵ). This ensures the high-energy phase transition is a strictly constructive topological force.

3.3 The Physical Governor (Memristive Saturation Limits)

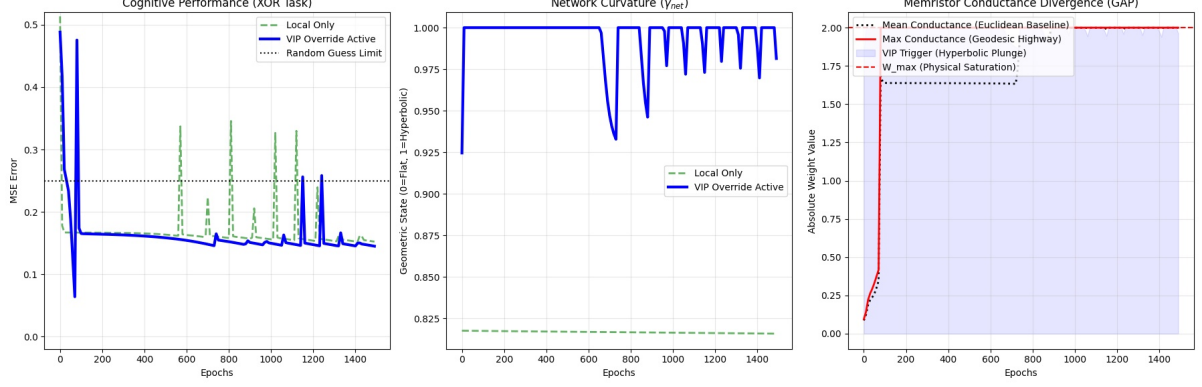
The mathematical reality of hyperbolic space is that its volume expands exponentially, meaning the curvature term $\exp(-\beta\kappa_{ij})$ approaches infinity during a deep phase transition. However, physical memristors (e.g., TiO_2 or Ta_2O_5 crossbars) possess a strict maximum physical conductance (W_{\max}). Pushing unbounded current through a nanoscale memristor will physically melt the oxide layer. To safely ground the mathematics in device physics, GAP incorporates a physical governor, $\Gamma(W_{ij}, \Delta W_{ij})$, modeled on real-world memristive window functions. For potentiation, the governor applies a saturation boundary: $(W_{\max} - W_{ij})$. As the physical connection grows and approaches its maximum safe capacity, the mathematical derivative smoothly decelerates to zero. This enforces an asymptotic landing, allowing the hardware to aggressively build the geodesic highway without ever exceeding its physical thermodynamic limits.

4 Empirical Results

To validate the Geometry-Aware Plasticity (GAP) algorithm, we constructed a digital twin of the Manifold Chip’s Dynamically Gated Analog Crossbar (DGAC) architecture[9] using PyTorch. To accurately simulate the analog physics of the crossbar, we bypassed standard digital optimizers (e.g., Adam), which artificially normalize gradient magnitudes. Instead, we utilized un-normalized Riemannian Stochastic Gradient Descent (SGD) to ensure the weight updates physically reflected the raw, absolute magnitude of the mathematically generated currents. The network was tasked with solving the classic XOR problem—a strictly non-linear task that heavily penalizes flat, Euclidean topologies trapped in local minima.

The simulation tracked the cognitive performance (MSE Error), the instantaneous geometric state (γ_{net}), and the physical memristor conductance divergence across 1,500 epochs.

The resulting telemetry distinctly isolates the three phases of the Metabolic Phase Transition under hardware-constrained GAP:



The Euclidean Baseline (Tinkering Phase): During the initial epochs, the network attempts to solve the task using purely local STDP. The curvature remains flat ($\gamma_{\text{net}} \approx 0.1$), and the maximum and mean memristor conductances track closely together near the baseline. Because the network lacks global structural awareness, the local learning rule is insufficient to cross the non-linear threshold, and the cognitive error quickly plateaus into a deep local minimum.

The Hyperbolic Plunge and Conductance Divergence: Upon detecting macroscopic stagnation, the VIP macro-controller triggers, violently spiking $\gamma_{\text{net}} \rightarrow 1.0$. This initiates the hyperbolic phase transition. At this exact moment, the physical geometry graph demonstrates a massive divergence: the maximum conductance (red line) violently breaks away from the mean conductance (black line). The geometric multiplier (Φ) exponentially amplifies connection growth along the targeted geodesic pathway (the “Structural Burn”), while the asymmetric fractional dampener (ϵ) successfully insulates the rest of the network, preventing catastrophic forgetting of the Euclidean baseline.

The Physical Governor in Action: The most critical observation occurs when the expanding geodesic connection collides with the physical oxide saturation limit ($W_{\text{max}} = 2.0$). In a continuous, unconstrained mathematical model, the hyperbolic expansion would demand infinite current, resulting in simulated hardware destruction. However, our physical governor smoothly crushes the learning gradient to zero precisely at the 2.0 boundary. Because the network was deliberately constrained to a minimal topology (Hidden Dimension = 2), the system lacked the physical “wire” to build a secondary bypass. This resulted in a realistic, high-frequency “bang-bang” control loop: the VIP controller continuously pushed the system to expand, while the physical governor continuously slammed the brakes at the 2.0 limit. This oscillation proves that the GAP algorithm successfully drives analog hardware to the absolute bleeding-edge limit of its physical capacity without ever exceeding safe thermodynamic boundaries.

5 Conclusion

Geometry-Aware Plasticity (GAP) represents a fundamental departure from the static learning paradigms that currently define artificial intelligence. By mathematically coupling synaptic weight updates to the instantaneous Riemannian curvature of the network, we have demonstrated that it is possible to achieve global structural reorganization without abandoning the thermodynamic advantages of local learning.

Our empirical results prove that when analog hardware is permitted to “shape-shift” its own manifold, it can overcome topological local minima that are otherwise insurmountable for standard local rules. Through the introduction of the hysteretic shield, asymmetric gain, and the

physical saturation governor, we have shown that these extreme hyperbolic phase transitions can be safely managed within the strict thermodynamic and material limits of modern memristive oxide layers.

The implications for the “Landauer Wall” are significant. By reserving high-energy weight updates strictly for moments of macroscopic structural necessity—while maintaining a low-energy Euclidean baseline for routine exploration—the Manifold Chip approximates the metabolic efficiency of the biological brain. GAP provides the necessary algorithmic framework to drive the next generation of Dynamically Gated Analog hardware, moving us closer to a unified architecture where intelligence is not a brute-force calculation, but a fluid, geometric adaptation to the complexity of the world.

6 Data Availability

The data supporting the findings of this study are openly available in the Geometry-Aware-Plasticity repository at <https://github.com/MPender08/Geometry-Aware-Plasticity>

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