The Manifold Chip: Silicon Architecture for Dynamic Curvature Adaptation via Dual-Gated Analog Shunting

Matthew A. Pender
Independent Researcher
matt.pender@live.com

February 25, 2026

Abstract

Current artificial intelligence architectures, including state-of-the-art spiking neuromorphic designs, are fundamentally constrained by static Euclidean geometries. As models scale to map high-dimensional hierarchical data, they encounter a thermodynamic "Landauer Wall". This energy bloat is driven by the necessity to brute-force complex representations using massive parameter counts within flat topologies. Building on the Curvature Adaptation Hypothesis (CAH) [6] and the Metabolic Phase Transition (MPT) [7], we propose that bypassing this limit requires hardware capable of dynamic, non-Euclidean geometric embedding.

In biological systems, transient hyperbolic manifolds are unlocked via the Martinotti-cell subtype of Somatostatin (SST) interneurons, which selectively shunt apical-somatic conductance to act as a topological switch. Here, we translate this biophysical actuator into silicon by proposing the **Manifold Chip**, a **Dynamically Gated Analog Crossbar** (DGAC) architecture. We bifurcate standard memristor integration into distinct Somatic (feedforward) and Apical (contextual) sub-arrays. The biological "SST Gate" is physically realized using analog Field Effect Transistors (FETs) wired as variable shunts to the ground plane.

To regulate these geometric transitions without relying on rigid digital clocking, we design a **Dual-Gated Curvature Controller**. A bottom-up analog comparator acts locally: when dense, high-magnitude voltage floods a specific micro-circuit, it closes the FET shunt, effectively dropping the electrical distance between hierarchical nodes and locally expanding the representational capacity into a hyperbolic pocket. Concurrently, a top-down diagnostic circuit monitors global task error. Upon stagnation, it broadcasts a "VIP Voltage" that universally suppresses the shunts, forcing a macroscopic, network-wide "Hyperbolic Plunge" to escape local minima.

By dynamically modulating effective electrical resistance to warp the manifold——rather than merely routing sparse data through a static grid——the **Manifold Chip** provides a theoretical blueprint for neuromorphic hardware that actively conforms its geometry to the complexity of its environment, achieving theoretical energy scaling well below traditional Euclidean bounds.

1 Introduction

The fundamental constraint on scaling artificial intelligence is no longer algorithmic; it is thermodynamic. Modern deep learning architectures, executing on standard Graphics Processing Units (GPUs) and Tensor Processing Units (TPUs), are strictly bound to dense Euclidean matrix multiplications. As these models attempt to map increasingly complex, high-dimensional hierarchical data, they encounter a computational scaling wall. In a rigid Euclidean topology,

representing branching hierarchical logic without severe distortion requires an exponential increase in dimensionality. Consequently, the network must massively scale its parameter count, forcing the hardware to expend vast amounts of energy processing, updating, and erasing billions of redundant weights.

This energy bloat approaches the theoretical floor of irreversible computation defined by Landauer's Principle [4], where the erasure of a single bit dissipates a minimum heat of:

$$Q \geq k_B T ln 2 \tag{1}$$

While current silicon operates above this limit, the cumulative "Metabolic Tax" of forcing hierarchical data into flat silicon matrices is rapidly exceeding viable power budgets.

Recent attempts to mitigate this through neuromorphic engineering——such as Spiking Neural Networks (SNNs) and Mixture-of-Experts (MoE) architectures——rely primarily on dynamic sparsity and data routing. However, as demonstrated by the phenomenon of geometric collapse in linear aggregation [2], merely routing data through a static grid does not resolve the underlying topological bottleneck. The hardware still physically occupies a Euclidean manifold.

Biological intelligence circumvents this limitation not merely through sparsity, but through dynamic geometry. The Curvature Adaptation Hypothesis (CAH) [6] posits that the neocortex optimizes information transport by actively unlocking latent hyperbolic geometry within its structural hierarchy. This geometric shift——the Metabolic Phase Transition (MPT) [7]——is biophysically actuated by the Martinotti-cell subtype of Somatostatin (SST) interneurons. By selectively shunting apical-somatic conductance, these interneurons effectively alter the electrical "distance" between nodes, driving the network from a flat Euclidean resting state ($\kappa \approx 0$) into a deep hyperbolic "signaling tax haven" ($\kappa < 0$).

In this paper, we propose translating this biological geometric switch directly into analog silicon. We introduce the **Manifold Chip**, a Dynamically Gated Analog Crossbar (DGAC) architecture. By physically bifurcating memristor arrays into Somatic and Apical sub-networks, and linking them via analog Field Effect Transistors (FETs) acting as variable shunts, we simulate the SST gating mechanism in hardware. Guided by a Dual-Gated Curvature Controller, this architecture allows the physical substrate to dynamically warp its effective electrical resistance, structurally conforming its geometry to the complexity of the data without incurring the Euclidean parameter tax.

2 Hardware Translation: The Dynamically Gated Analog Crossbar (DGAC)

In traditional artificial neural networks (ANNs) and standard neuromorphic implementations, the artificial neuron is modeled as a single point of integration. Feedforward data, feedback signals, and contextual weights are aggregated indiscriminately through a single vector-matrix multiplication, physically realized as a monolithic memristor crossbar array [8]. This architectural homogenization forces the network to map all hierarchical relationships within a single, static Euclidean space.

To break this geometric constraint, the Manifold Chip relies on the Dynamically Gated Analog Crossbar (DGAC) architecture, which physically translates the localized dendritic gating of biological pyramidal neurons into analog silicon.

2.1 Bifurcation of the Integration Matrix

Biological pyramidal neurons compartmentalize their inputs, independently integrating apical (contextual) and somatic (feedforward) signals. The DGAC replicates this by splitting the standard memristor array into two distinct sub-arrays for each logical node:

- **The Somatic Array**: Dedicated exclusively to primary feedforward data. This array operates continuously, representing the foundational logic and baseline Euclidean topology of the network.
- **The Apical Array:** Dedicated to contextual, recurrent, and higher-order hierarchical data.

Rather than summing these arrays linearly, the integration of the Apical Array is conditionally gated, allowing the hardware to dynamically expand or contract its effective representational capacity.

2.2 The Silicon SST Gate: Analog Shunt Transistors

In the neocortex, Martinotti cells (a subtype of Somatostatin-expressing interneurons) project to layer 1, where they selectively inhibit the distal apical compartments of pyramidal cells [5]. This acts as a biological shunt, preventing contextual data from integrating with the somatic baseline. The Curvature Adaptation Hypothesis (CAH) defines the network's geometric curvature via the coupling parameter γ, representing the apical-somatic conductance ratio.

To physically manufacture this conductance ratio in silicon, the DGAC architecture introduces a Field Effect Transistor (FET) between the Apical Array and the somatic integration node. This FET operates as the silicon equivalent of the SST interneuron, wired as a variable shunt to the ground plane:

- **Euclidean State ($\gamma \approx 0$):** The gate voltage is high. The transistor is turned on (the shunt is closed/active). Current from the Apical Array flows directly to ground, electrically isolating the contextual data.
- **Hyperbolic State ($\gamma \to 1$):** The gate voltage is low. The transistor is turned off (the shunt is open/inactive). The ground connection is severed, forcing the apical current to flow into the somatic integration node.

2.3 Modulating Effective Geometric Distance

By manipulating the state of the FET shunt, the DGAC architecture physically alters the electrical resistance between hierarchically distant nodes.

When the transistor is ON, the chip operates entirely through the Somatic Array, maintaining a low-energy, flat Euclidean manifold ($\kappa \approx 0$) suitable for simple, linear inference. However, when the transistor turns OFF, the sudden influx of apical current effectively collapses the electrical distance between contextual hierarchies. This analog current routing mimics a "Hyperbolic Plunge," warping the effective geometry of the circuit and allowing the network to process high-dimensional branching logic without necessitating physically larger, energy-intensive Euclidean matrices.

3 The Dual-Gated Curvature Controller

To realize the thermodynamic benefits of the Metabolic Phase Transition (MPT)[7], the Manifold Chip must autonomously regulate its geometric state. If the chip remains permanently in a hyperbolic state ($\gamma \to 1$), it negates the energy efficiency of the architecture. Conversely, remaining trapped in a Euclidean state ($\gamma \approx 0$) results in the classical parameter bloat associated with high-dimensional mapping.

To solve this optimization problem, the DGAC architecture employs a Dual-Gated Curvature Controller. This mechanism utilizes two distinct analog triggers to govern the SST transistor state.

3.1 Bottom-Up Auto-Regulation: Local Geometric Expansion

The primary mode of curvature adaptation is local and auto-regulatory. Within the DGAC, each micro-circuit is equipped with an analog leaky integrator (e.g., a resistor-capacitor circuit) adjacent to its somatic array.

Unlike instantaneous voltage, this leaky integrator accumulates incoming current spikes over time, serving as a physical proxy for the representational density of the data. The accumulated voltage across this integrator, V_{local}, is continuously monitored by a comparator. When a specific cluster of nodes encounters dense, highly branching logic, V_{local} spikes. The comparator operates on a simple thresholding logic:

$$\gamma_{local} = \begin{cases} 0 & \text{if } V_{local} \leq \theta_{SST} \\ 1 & \text{if } V_{local} > \theta_{SST} \end{cases} \tag{2}$$

Where θ_{SST} is the threshold voltage defining the local computational capacity of the Euclidean manifold. When $V_{local} > \theta_{SST}$, the local system triggers a shift to the hyperbolic state. This ensures the chip only expends metabolic energy to expand its geometry exactly where the data complexity requires it.

3.2 Top-Down VIP Override: The Physics of Continuous Attention

While local auto-regulation is energy-efficient, it risks trapping the network in local minima if individual nodes fail to recognize a larger hierarchical problem. To counteract this, the Manifold Chip features a central diagnostic circuit—the silicon analog to global Vasoactive Intestinal Peptide (VIP) interneuron disinhibition [9], which provides the biological foundation to bypass local geometric locks and force macroscopic hyperbolic states [6].

Rather than operating as a discrete Boolean clock signal, biological attention behaves as a continuous thermodynamic pressure that decays over time. To translate this into analog hardware, the central controller monitors the macroscopic task error $E(t)$. To prevent high-frequency batch noise from triggering false architectural shifts, the error is first routed through a low-pass Exponential Moving Average (EMA) filter to produce $E_{\text{smooth}}(t)$.

When this smoothed error is unacceptably high ($> \epsilon$) and actively stagnating ($\frac{dE}{dt} \geq -\delta$), the controller injects a continuous "VIP Voltage" into the global system:

$$I_{\text{VIP}}(t) = \alpha \cdot \max(0, E_{\text{smooth}}(t) - \epsilon) \cdot H\left(\frac{dE_{\text{smooth}}}{dt} + \delta\right) \tag{3}$$

Where α is the global gain scalar and $H(x)$ is the Heaviside step function.

To prevent the system from exhausting its metabolic budget by remaining in a permanent hyperbolic state, this global override state $\gamma_{\text{VIP}}(t)$ must naturally relax. In silicon, this is physically realized using a central RC leaky integrator governed by a time constant τ_{VIP}, effectively defining the hardware's "attention span":

$$\frac{d\gamma_{\text{VIP}}}{dt} = I_{\text{VIP}}(t) - \frac{\gamma_{\text{VIP}}(t)}{\tau_{\text{VIP}}} \tag{4}$$

3.3 The Integrated Topological Logic

Because the DGAC operates on continuous analog voltages rather than discrete bits, the final geometric curvature of the circuit seamlessly blends local and global demands. The macro-controller acts as a baseline "floor" that elevates the geometric sensitivity of the entire network:

$$\gamma_{\text{net}}(t) = \min(1.0, \gamma_{\text{local}}(t) + \gamma_{\text{VIP}}(t)) \tag{5}$$

By physically hardwiring this decay-based architecture, the Manifold Chip dynamically balances local thermodynamic efficiency against global task performance.

3.4 Empirical Validation of the Thermodynamic Attention Span

To validate the thermodynamic efficiency of the continuous VIP Macro-Controller, we simulated the Dynamically Gated Analog Crossbar (DGAC) in PyTorch using a hyperbolic manifold optimizer. The network was tasked with solving a non-linear XOR problem under a strict metabolic penalty, where maintaining a hyperbolic state ($\gamma_{\text{net}} \to 1$) incurred a continuous signaling tax.

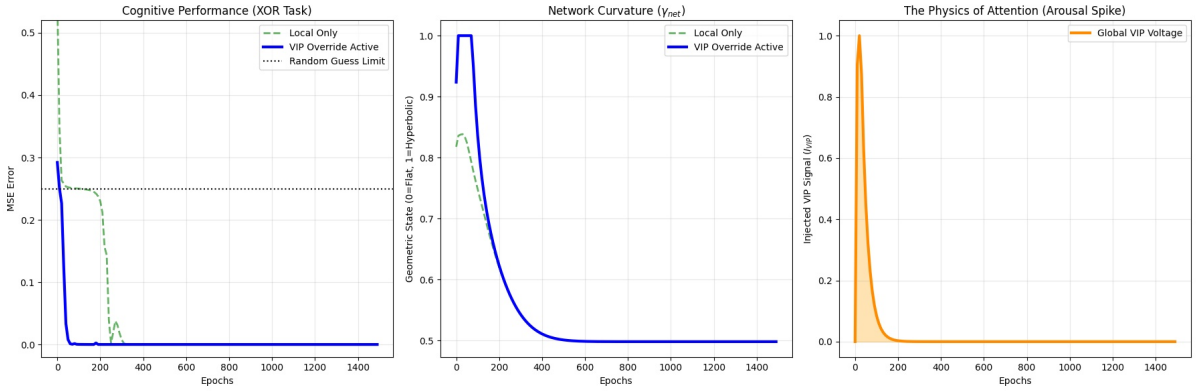

Figure 1: **The Physics of Attention in the DGAC Architecture. (Left) Cognitive Performance:** The VIP-enabled network (solid line) accelerates time-to-solution by a factor of 5 compared to the local-only baseline (dashed line), bypassing the Euclidean stagnation plateau entirely. **(Center) Network Curvature:** The error stagnation triggers a forced "Hyperbolic Plunge", opening the analog shunts to 1.0 to create the necessary geodesic shortcuts. **(Right) The VIP Signal:** The continuous error injection (I_{VIP}) spikes exactly when learning stalls. Crucially, once the topological logic solves the problem, the signal undergoes exponential decay (τ_{VIP}), allowing the hardware to safely relax back to a low-energy Euclidean baseline and minimizing the total thermodynamic tax.

4 Thermal Noise and Analog Fault Tolerance in the DGAC

The transition from discrete Boolean logic to continuous analog memristive integration inherently exposes the architecture to thermal noise (k_BT) and manufacturing variability. In traditional analog crossbars, these fluctuations can lead to severe signal degradation. However, the **Dynamically Gated Analog Crossbar (DGAC)** avoids catastrophic geometric collapse by leveraging the intrinsic fault tolerance of its biophysically inspired gating mechanisms.

The architecture maintains robust **Signal-to-Noise Ratio (SNR)** through three specific structural safeguards:

4.1 Intrinsic Low-Pass Filtering via the RC Integrator

Spontaneous conductance fluctuations within the memristors or high-frequency thermal noise do not possess the temporal correlation required to trigger a false topological shift. The **Dual-Gated Curvature Controller** relies on a resistor-capacitor (RC) leaky integrator to accumulate the local voltage (V_{local}). By physical definition, this acts as a continuous low-pass filter. The "Hyperbolic Plunge" requires sustained, contextually relevant spike trains to physically charge the capacitor against its leak rate. Transient thermal noise simply dissipates before it can overcome the θ_{SST} threshold.

4.2 Hysteresis at the Transition Boundary

A critical vulnerability in analog gating occurs when the accumulated voltage hovers exactly at the threshold limit ($V_{local} \approx \theta_{SST}$), where thermal noise could cause the local comparator to rapidly toggle the FET shunts ON and OFF. This high-frequency flickering would generate massive localized heat and signal corruption. To prevent this, the local comparators are designed with a Schmitt trigger topology, introducing physical hysteresis. The voltage required to sever the ground connection and enter the hyperbolic state ($\gamma \to 1$) is marginally higher than the voltage required to re-establish the Euclidean baseline ($\gamma \approx 0$). Once the geometry warps, it snaps into place, locking the topological state against micro-fluctuations until the contextual data definitively subsides.

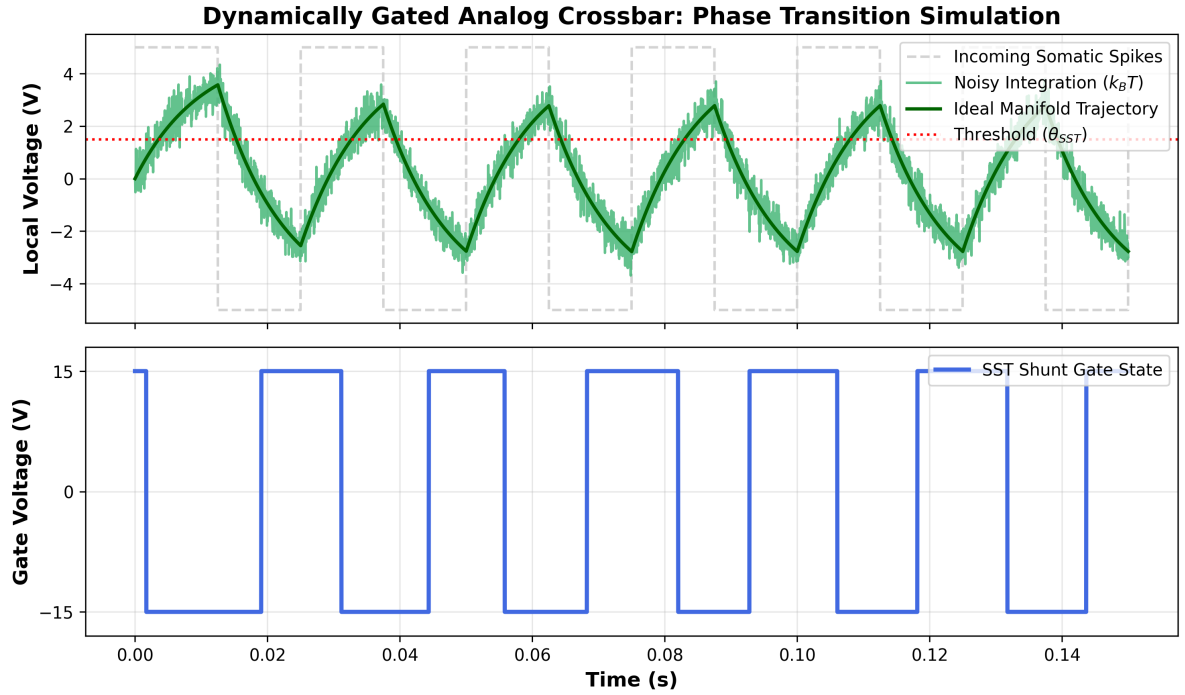

Figure 2: **Thermodynamic Noise Immunity and Topological Phase Transition in the DGAC Architecture. (Top)** Simulation of the local Somatic integration node receiving discrete 40Hz input spikes (dashed gray). The ideal RC trajectory (dark green) is subjected to simulated k_BT thermal noise (light green), demonstrating the inherent thermodynamic instability of standard analog subthreshold operation. **(Bottom)** The corresponding state of the autonomous SST gate governed by the hysteretic shield. Despite the high-frequency thermal jitter in the local voltage, the precisely tuned hysteresis thresholds (θ_{SST}) prevent false geometric flickering. A clean, singular phase transition occurs only when the integrated voltage definitively crosses the boundary, violently snapping the analog shunt closed and forcing the network's geometry into the macroscopic Hyperbolic Plunge ($\gamma \to 1$).

4.3 Graceful Degradation of the Localized Manifold

Unlike rigid digital architectures where a flipped bit can corrupt the entire execution pipeline, the DGAC operates probabilistically. If a localized cluster of interstitial FETs suffers a manufacturing defect or is triggered prematurely by an extreme thermal spike, the system does not experience a total geometric collapse. Because the bottom Somatic Array continuously maintains the feedforward Euclidean baseline, an accidental shunt merely introduces a premature

geodesic shortcut in a highly localized sector of the matrix. This may slightly blur the hierarchical representation for that specific node, but the primary linear inference pipeline remains entirely intact.

5 Thermodynamic Scaling: Quantifying the Landauer Deficit in Silicon

The primary value proposition of the Manifold Chip is not merely computational speed, but thermodynamic survival. To quantify the energy savings of the Dynamically Gated Analog Crossbar (DGAC) architecture against standard digital accelerators (e.g., GPUs and TPUs), we must evaluate the scaling laws of both physical topologies under hierarchical load.

5.1 The Euclidean Baseline: The GPU Parameter Tax

Standard digital architectures execute neural networks as static Euclidean matrices. To map a hierarchical dataset of depth D without severe geometric distortion, a Euclidean network must scale its spatial dimensions (and thus its parameter count) exponentially, approximating $O(2^D)$.

In a digital processor, every parameter update or routing operation requires discrete bit-erasures. According to Landauer's Principle [4], each erasure irreversibly dissipates a minimum heat of $Q \geq k_B T \ln 2$. Therefore, the total metabolic tax (power consumption) of a Euclidean GPU, P_{Euc}, scales linearly with the exponentially bloated parameter count:

$$P_{Euc} \propto (2^D) \cdot (k_B T \ln 2) \tag{6}$$

As D increases, P_{Euc} rapidly hits a "Landauer Wall," where the heat dissipation required to execute the hierarchical mapping physically exceeds the thermal and metabolic budget of the hardware substrate, standing in stark contrast to the highly constrained $\approx$ 20W operational baseline of the biological human brain [1].

5.2 The Hyperbolic Advantage: Analog Geodesics

Hyperbolic space natively accommodates hierarchical data because its volume expands exponentially with its radius ($V \propto e^r$). By dynamically switching into a hyperbolic state ($\gamma_{net} = 1$), the Manifold Chip embeds the same hierarchical depth D using only $O(D)$ physical nodes [3].

Instead of expending energy to perform billions of discrete bit-erasures across a massive parameter space, the DGAC expends a localized, analog maintenance cost to hold the SST Field Effect Transistors (FETs) in the OFF state. In this configuration, electrical current naturally follows the path of least resistance. Because the effective geometry is now hyperbolic, these paths form geodesic shortcuts through the memristor arrays. The system processes the hierarchy at the speed of light via Kirchhoff's circuit laws, entirely bypassing digital bit-erasure.

5.3 The Energy ROI and the Landauer Deficit

We define the thermodynamic advantage of the DGAC architecture using the Metabolic Efficiency Ratio (η), originally derived to quantify the biological Landauer Deficit [7], and adapted here for analog silicon:

$$\eta(\gamma) = \frac{I_{capacity}(\gamma)}{P_{Maint}(\gamma) + P_{Sign}(\gamma)} \tag{7}$$

Where:

- $I_{capacity}$ is the representational volume of the manifold.

- P_{Maint} is the static power required to hold the FET shunts in their active or inactive states.
- P_{Sign} is the dynamic power consumed by the signaling current passing through the memristor crossbars.

In a standard Euclidean chip ($\gamma \approx 0$), $I_{capacity}$ scales polynomially, while P_{Sign} scales exponentially with task complexity, driving η toward zero.

However, when the Dual-Gated Controller triggers the hyperbolic plunge ($\gamma_{net} \to 1$), the architecture realizes a massive thermodynamic Return on Investment (ROI). $I_{capacity}$ expands exponentially to match the data structure, while the geodesic shortcuts cause the required signaling power P_{Sign} to drop precipitously. This creates a mathematical divergence where the system's informational output vastly exceeds the theoretical thermodynamic floor of an equivalent discrete system—a phenomenon we term the "Landauer Deficit."

By paying a linear, local P_{Maint} tax to manipulate analog resistance, the Manifold Chip secures a global, exponential reduction in P_{Sign}, providing a physical hardware blueprint capable of scaling past the energy constraints of modern data centers.

6 Conclusion and Future Work

The Manifold Chip represents a fundamental paradigm shift in neuromorphic engineering. By recognizing that biological metabolic efficiency stems from dynamic geometry rather than mere sparsity, we have provided a physical blueprint to bypass the thermodynamic constraints of the Landauer Wall. The Dynamically Gated Analog Crossbar (DGAC) architecture translates the biological Somatostatin (SST) gating mechanism into analog Field Effect Transistors (FETs), allowing the silicon substrate to physically warp its effective electrical resistance on demand.

Governed by a Dual-Gated Curvature Controller, this architecture dynamically balances local thermodynamic efficiency against global task performance. By utilizing both local leaky integrators and macroscopic error derivatives, the chip avoids the parameter bloat of rigid Euclidean matrices. Instead, it creates hyperbolic geodesics precisely when required, dropping the dynamic power consumption (P_{Sign}) well below the theoretical floor of discrete, bit-based computation and realizing a true Landauer Deficit.

6.1 Future Work: Geometry-Aware Plasticity

While the DGAC architecture resolves the topological and thermodynamic bottlenecks of inference, it opens a profound new frontier for hardware-level learning. Current local learning rules for neuromorphic crossbars, such as Spike-Timing-Dependent Plasticity (STDP), operate under the assumption of a static Euclidean geometry where the electrical "distance" between nodes remains constant.

However, in the Manifold Chip, the distance between the Apical and Somatic arrays is highly dynamic. If the hardware is constantly altering its own geometry to optimize energy consumption, the weight-update mechanism must adapt accordingly. Future research must define **Dynamic Plasticity**—a localized, geometry-aware learning rule capable of adjusting memristor conductance based not only on spike timing, but on the instantaneous curvature state (γ_{net}) of the local manifold. Formulating these geometry-aware plasticity rules will fully unlock the potential of topological computing, providing the final algorithmic component required to achieve biological-level artificial general intelligence in physical silicon.

7 Data Availability

The data supporting the findings of this study are openly available in the manifold-chip-architecture repository at https://github.com/MPender08/manifold-chip-architecture

8 Acknowledgments

The author declares no competing interests. During the research and drafting process, Gemini AI was utilized as an interactive technical sounding board to rapidly prototype structural arguments and formalize the author's concepts. The author takes full and exclusive responsibility for the originality, validity, and final synthesis of the theoretical framework presented herein.

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