CSU22022 Computer Architecture I

Prof. Michael Manzke

Full Processor Project 1st Instalment

Checklist

4th November 2024

Version 2.0

Checklist for the submission of the Full Processor Project 2nd Instalment. Please don't submit these files but confirm that all entities from the 1st Instalment are tested and working.

1	RF_Mux3_1Bit_XXXXXXXX.vhd	
	RF_Mux3_1Bit_XXXXXXXX_TB.vhd	
	RF_Mux3_1Bit_XXXXXXXX_SchematicXX.pdf	
	RF_Mux3_1Bit_XXXXXXXX_TDXX.png	
	RF_Mux3_1Bit_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

2	RF_Mux3_32Bit_XXXXXXXX.vhd	
	RF_Mux3_32Bit_XXXXXXXX_TB.vhd	
	RF_Mux3_32Bit_XXXXXXXX_SchematicXX.pdf	
	RF_Mux3_32Bit_XXXXXXXX_TDXX.png	
	RF_Mux3_32Bit_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

3	RF_Mux16_1Bit_XXXXXXXX.vhd	
	RF_Mux16_1Bit_XXXXXXXX_TB.vhd	
	RF_Mux16_1Bit_XXXXXXXX_SchematicXX.pdf	
	RF_Mux16_1Bit_XXXXXXXX_TDXX.png	
	RF_Mux16_1Bit_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

4	RF_Mux16_32Bit_XXXXXXXX.vhd	
	RF_Mux16_32Bit_XXXXXXXX_TB.vhd	
	RF_Mux16_32Bit_XXXXXXXX_SchematicXX.pdf	
	RF_Mux16_32Bit_XXXXXXXX_TDXX.png	
	RF_Mux16_32Bit_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

5	RF_Mux32_1Bit_XXXXXXXX.vhd	
	RF_Mux32_1Bit_XXXXXXXX_TB.vhd	
	RF_Mux32_1Bit_XXXXXXXX_SchematicXX.pdf	
	RF_Mux32_1Bit_XXXXXXXX_TDXX.png	
	RF_Mux32_1Bit_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

6	RF_Mux32_32Bit_XXXXXXXX.vhd	
	RF_Mux32_32Bit_XXXXXXXX_TB.vhd	
	RF_Mux32_32Bit_XXXXXXXX_SchematicXX.pdf	
	RF_Mux32_32Bit_XXXXXXXX_TDXX.png	
	RF_Mux32_32Bit_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

7	RF_DFlipFlop_XXXXXXXX.vhd	
	RF_DFlipFlop_XXXXXXXX_TB.vhd	
	RF_DFlipFlop_XXXXXXXX_SchematicXX.pdf	
	RF_DFlipFlop_XXXXXXXX_TDXX.png	
	RF_DFlipFlop_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

8	RF_Register32Bit_XXXXXXXX.vhd	
	RF_Register32Bit_XXXXXXXX_TB.vhd	
	RF_Register32Bit_XXXXXXXX_SchematicXX.pdf	
	RF_Register32Bit_XXXXXXXX_TDXX.png	
	RF_Register32Bit_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

9	RF_DestReg_Decoder_XXXXXXXX.vhd	
	RF_DestReg_Decoder_XXXXXXXX_TB.vhd	
	RF_DestReg_Decoder_XXXXXXXX_SchematicXX.pdf	
	RF_DestReg_Decoder_XXXXXXXX_TDXX.png	
	RF_DestReg_Decoder_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

10	RF_TempDestReg_Decoder_XXXXXXXX.vhd	
	RF_TempDestReg_Decoder_XXXXXXXX_TB.vhd	
	RF_TempDestReg_Decoder_XXXXXXXX_SchematicXX.pdf	
	RF_TempDestReg_Decoder_XXXXXXXX_TDXX.png	
	RF_TempDestReg_Decoder_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

11	RF_RegisterFile_32_15_XXXXXXXX.vhd	
	RF_RegisterFile_32_15_XXXXXXXX_TB.vhd	
	RF_RegisterFile_32_15_XXXXXXXX_SchematicXX.pdf	
	RF_RegisterFile_32_15_XXXXXXXX_TDXX.png	
	RF_RegisterFile_32_15_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

12	RF_Test_RegisterFile_32_15_XXXXXXXX.vhd	
	RF_Test_RegisterFile_32_15_XXXXXXXX_TB.vhd	
	RF_Test_RegisterFile_32_15_XXXXXXXX_SchematicXX.pdf	
	RF_Test_RegisterFile_32_15_XXXXXXXX_TDXX.png	
	RF_Test_RegisterFile_32_15_XXXXXXXX_Doc.tex (can be any file format)	
	Is working	

Student Name:_____

Student ID:_____

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Date Signature