Case	CLK	RW	DR	SA	SB	TA	TB	TD	D	A	B
1	1	1	0	0	0	0	0	0	0164a69e	0164a69e	0164a69e
2	1	1	1	1	1	0	0	0	0164a69f	0164a69f	0164a69f
3	1	1	2	2	2	0	0	0	0164a6A0	0164a6A0	0164a6A0
....	....	....	....	....	....	....	....	....	....	....	....
32	1	1	31	31	31	0	0	0	0164a6Be	0164a6Be	0164a6Be
33	1	1	0	0	0	1	1	1	0164a6Bf	0164a6Bf	0164a6Bf
34	1	1	0	0	0	2	2	2	0164a6C0	0164a6C0	0164a6C0
....	....	....	....	....	....	....	....	....	....	....	....
45	1	1	0	0	0	13	13	13	0164a6cB	0164a6cB	0164a6cB
46	1	1	0	0	0	14	14	14	0164a6cC	0164a6cC	0164a6cC
47	1	1	0	0	0	15	15	15	0164a6cD	0164a6cD	0164a6cD

The propagation delay I measured for my register file was 94 ns, measuring at the start of a rising clock.