CSU22022 Computer Architecture I

Prof. Michael Manzke

Full Processor Project 2nd Instalment

Checklist

4th November 2024

Version 1.0

All files must be submitted to Blackboard as individual files, no zip-files. With one exception: the "Processor_XXXXXXXX.srcs" must be a zip-file. Submit only entities that are working and are fully tested. You must follow the entity order on the checklist. You cannot skip entities.

The entities must be programmed and tested in the following order. Please confirm by ticking all the boxes, next to the items, that all required files are available on Blackboard and that the entity is fully working. You must print this checklist, tick the boxes, sign it, and submit it with your milestone assignment to Blackboard.

All files must be submitted in the checklist order:

DP_FullAdder_XXXXXXXX.vhd
DP_FullAdder_XXXXXXXX_TB.vhd
DP_FullAdder_XXXXXXXX_SchematicXX.pdf
DP_FullAdder_XXXXXXXX_TDXX.png
DP_FullAdder_XXXXXXXX_Doc. txt (can be any file format)
DP_RippleCarryAdder32Bit_XXXXXXXX.vhd
DP_RippleCarryAdder32Bit_XXXXXXXX_TB.vhd
DP_RippleCarryAdder32Bit_XXXXXXXX_SchematicXX.pdf
DP_RippleCarryAdder32Bit_XXXXXXXX_TDXX.png
DP_RippleCarryAdder32Bit_XXXXXXXX_Doc.txt (can be any file format)

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00	My submission complies with the “Instructions for the Blackboard Submission of the Assignment” (CSU22022 Full Processor Project 2nd Instalment 2024-2025 Instruction V1.0.pdf)	
01	DP_FullAdder_XXXXXXXX.vhd	
	DP_FullAdder_XXXXXXXX _TB.vhd	
	DP_FullAdder_XXXXXXXX _SchematicXX.pdf	
	DP_FullAdder_XXXXXXXX _TDXX.png	
	DP_FullAdder_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

02	DP_RippleCarryAdder32Bit_XXXXXXXX.vhd	
	DP_RippleCarryAdder32Bit_XXXXXXXX_TB.vhd	
	DP_RippleCarryAdder32Bit_XXXXXXXX_SchematicXX.pdf	
	DP_RippleCarryAdder32Bit_XXXXXXXX_TDXX.png	
	DP_RippleCarryAdder32Bit_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

03	DP_SingleBit_B_Logic_XXXXXXXX.vhd	
	DP_SingleBit_B_Logic_XXXXXXXX_TB.vhd	
	DP_SingleBit_B_Logic_XXXXXXXX_SchematicXX.pdf	
	DP_SingleBit_B_Logic_XXXXXXXX_TDXX.png	
	DP_SingleBit_B_Logic_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

04	DP_32Bit_B_Logic_XXXXXXXX.vhd	
	DP_32Bit_B_Logic_XXXXXXXX_TB.vhd	
	DP_32Bit_B_Logic_XXXXXXXX_SchematicXX.pdf	
	DP_32Bit_B_Logic_XXXXXXXX_TDXX.png	
	DP_32Bit_B_Logic_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

05	DP_SingleBit_LogicCircuit_XXXXXXXX.vhd	
	DP_SingleBit_LogicCircuit_XXXXXXXX_TB.vhd	
	DP_SingleBit_LogicCircuit_XXXXXXXX_SchematicXX.pdf	
	DP_SingleBit_LogicCircuit_XXXXXXX _TDXX.png	
	DP_SingleBit_LogicCircuit_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

06	DP_32Bit_LogicCircuit_XXXXXXXX.vhd	
	DP_32Bit_LogicCircuit _XXXXXXXX_TB.vhd	
	DP_32Bit_LogicCircuit _XXXXXXXX_SchematicXX.pdf	
	DP_32Bit_LogicCircuit _XXXXXXXX_TDXX.png	
	DP_32Bit_LogicCircuit _XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

07	CPU_Mux2_32Bit _XXXXXXXX.vhd	
	CPU_Mux2_32Bit _XXXXXXXX_TB.vhd	
	CPU_Mux2_32Bit _XXXXXXXX_SchematicXX.pdf	
	CPU_Mux2_32Bit _XXXXXXXX_TDXX.png	
	CPU_Mux2_32Bit _XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

08	DP_ArithmeticLogicUnit _XXXXXXXX.vhd	
	DP_ArithmeticLogicUnit _XXXXXXXX_TB.vhd	
	DP_ArithmeticLogicUnit _XXXXXXXX_SchematicXX.pdf	
	DP_ArithmeticLogicUnit _XXXXXXXX_TDXX.png	
	DP_ArithmeticLogicUnit _XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

09	DP_Mux3_1Bit_XXXXXXXX.vhd	
	DP_Mux3_1Bit_XXXXXXXX_TB.vhd	
	DP_Mux3_1Bit_XXXXXXXX_SchematicXX.pdf	
	DP_Mux3_1Bit_XXXXXXXX_TDXX.png	
	DP_Mux3_1Bit_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

10	DP_ShifterCFlagMux2_1Bit_XXXXXXXX.vhd	
	DP_ShifterCFlagMux2_1Bit_XXXXXXXX _TB.vhd	
	DP_ShifterCFlagMux2_1Bit_XXXXXXXX _SchematicXX. pdf	
	DP_ShifterCFlagMux2_1Bit _XXXXXXXX _TDXX.png	
	DP_ShifterCFlagMux2_1Bit _XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

11	DP_Shifter_XXXXXXXX.vhd	
	DP_Shifter_XXXXXXXX _TB.vhd	
	DP_Shifter_XXXXXXXX _SchematicXX. Pdf	
	DP_Shifter_XXXXXXXX _TDXX.png	
	DP_Shifter_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

12	DP_CFlagMux2_1Bit_XXXXXXXX.vhd	
	DP_CFlagMux2_1Bit_XXXXXXXX _TB.vhd	
	DP_CFlagMux2_1Bit_XXXXXXXX _SchematicXX. pdf	
	DP_CFlagMux2_1Bit_XXXXXXXX _TDXX.png	
	DP_CFlagMux2_1Bit_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

13	DP_ZeroDetection_XXXXXXXX.vhd	
	DP_ZeroDetection_XXXXXXXX _TB.vhd	
	DP_ZeroDetection_XXXXXXXX _SchematicXX.pdf	
	DP_ZeroDetection_XXXXXXXX _TDXX.png	
	DP_ZeroDetection_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

14	DP_FunctionalUnit_XXXXXXXX.vhd	
	DP_FunctionalUnit_XXXXXXXX _TB.vhd	
	DP_FunctionalUnit_XXXXXXXX _SchematicXX.pdf	
	DP_FunctionalUnit_XXXXXXXX _TDXX.png	
	DP_FunctionalUnit_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

15	Processor_XXXXXXXX.srcs (including all subdirectories and files)	
	Processor_XXXXXXXX.xpr	

16	CSU22022 Full Processor Project 1st Instalment 2024-2025 Checklist V2.0	

Student Name: _____

Student ID: _____

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Date Signature