

Case	CLK	Reset	D	Q
1		1	1	0
2		1	0	0
3		1	0	0
4		1	0	1
5		1	0	0
6		1	0	1
7		1	0	0
8		1	1	0

The propagation delay for this and the 32 bit register are identical at 20 ns for a reset and 26 ns for loading a value