CSU22022 Computer Architecture I

Prof. Michael Manzke

Full Processor Project 2nd Instalment

Checklist

11th November 2024

Version 2.0

Checklist for the submission of the Full Processor Project 3rd Instalment. Please don't submit these files but confirm that all entities from the 2nd Instalment are tested and working.

01	DP_FullAdder_XXXXXXXX.vhd	
	DP_FullAdder_XXXXXXXX _TB.vhd	
	DP_FullAdder_XXXXXXXX _SchematicXX.pdf	
	DP_FullAdder_XXXXXXXX _TDXX.png	
	DP_FullAdder_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

02	DP_RippleCarryAdder32Bit_XXXXXXXX.vhd	
	DP_RippleCarryAdder32Bit_XXXXXXXX_TB.vhd	
	DP_RippleCarryAdder32Bit_XXXXXXXX_SchematicXX.pdf	
	DP_RippleCarryAdder32Bit_XXXXXXXX_TDXX.png	
	DP_RippleCarryAdder32Bit_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

03	DP_SingleBit_B_Logic_XXXXXXXX.vhd	
	DP_SingleBit_B_Logic_XXXXXXXX_TB.vhd	
	DP_SingleBit_B_Logic_XXXXXXXX_SchematicXX.pdf	
	DP_SingleBit_B_Logic_XXXXXXXX_TDXX.png	
	DP_SingleBit_B_Logic_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

04	DP_32Bit_B_Logic_XXXXXXXX.vhd	
	DP_32Bit_B_Logic_XXXXXXXX_TB.vhd	
	DP_32Bit_B_Logic_XXXXXXXX_SchematicXX.pdf	
	DP_32Bit_B_Logic_XXXXXXXX_TDXX.png	
	DP_32Bit_B_Logic_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

05	DP_SingleBit_LogicCircuit_XXXXXXXX.vhd	
	DP_SingleBit_LogicCircuit_XXXXXXXX_TB.vhd	
	DP_SingleBit_LogicCircuit_XXXXXXXX_SchematicXX.pdf	
	DP_SingleBit_LogicCircuit_XXXXXXX _TDXX.png	
	DP_SingleBit_LogicCircuit_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

06	DP_32Bit_LogicCircuit_XXXXXXXX.vhd	
	DP_32Bit_LogicCircuit _XXXXXXXX_TB.vhd	
	DP_32Bit_LogicCircuit _XXXXXXXX_SchematicXX.pdf	
	DP_32Bit_LogicCircuit _XXXXXXXX_TDXX.png	
	DP_32Bit_LogicCircuit _XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

07	CPU_Mux2_32Bit _XXXXXXXX.vhd	
	CPU_Mux2_32Bit _XXXXXXXX_TB.vhd	
	CPU_Mux2_32Bit _XXXXXXXX_SchematicXX.pdf	
	CPU_Mux2_32Bit _XXXXXXXX_TDXX.png	
	CPU_Mux2_32Bit _XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

08	DP_ArithmeticLogicUnit _XXXXXXXX.vhd	
	DP_ArithmeticLogicUnit _XXXXXXXX_TB.vhd	
	DP_ArithmeticLogicUnit _XXXXXXXX_SchematicXX.pdf	
	DP_ArithmeticLogicUnit _XXXXXXXX_TDXX.png	
	DP_ArithmeticLogicUnit _XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

09	DP_Mux3_1Bit_XXXXXXXX.vhd	
	DP_Mux3_1Bit_XXXXXXXX_TB.vhd	
	DP_Mux3_1Bit_XXXXXXXX_SchematicXX.pdf	
	DP_Mux3_1Bit_XXXXXXXX_TDXX.png	
	DP_Mux3_1Bit_XXXXXXXX_Doc.txt (can be any file format)	
	Is working	

10	DP_ShifterCFlagMux2_1Bit_XXXXXXXX.vhd	
	DP_ShifterCFlagMux2_1Bit_XXXXXXXX _TB.vhd	
	DP_ShifterCFlagMux2_1Bit_XXXXXXXX _SchematicXX. pdf	
	DP_ShifterCFlagMux2_1Bit _XXXXXXXX _TDXX.png	
	DP_ShifterCFlagMux2_1Bit _XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

11	DP_Shifter_XXXXXXXX.vhd	
	DP_Shifter_XXXXXXXX _TB.vhd	
	DP_Shifter_XXXXXXXX _SchematicXX. pdf	
	DP_Shifter_XXXXXXXX _TDXX.png	
	DP_Shifter_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

12	DP_CFlagMux2_1Bit_XXXXXXXX.vhd	
	DP_CFlagMux2_1Bit_XXXXXXXX _TB.vhd	
	DP_CFlagMux2_1Bit_XXXXXXXX _SchematicXX. pdf	
	DP_CFlagMux2_1Bit_XXXXXXXX _TDXX.png	
	DP_CFlagMux2_1Bit_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

13	DP_ZeroDetection_XXXXXXXX.vhd	
	DP_ZeroDetection_XXXXXXXX _TB.vhd	
	DP_ZeroDetection_XXXXXXXX _SchematicXX.pdf	
	DP_ZeroDetection_XXXXXXXX _TDXX.png	
	DP_ZeroDetection_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

14	DP_FunctionalUnit_XXXXXXXX.vhd	
	DP_FunctionalUnit_XXXXXXXX _TB.vhd	
	DP_FunctionalUnit_XXXXXXXX _SchematicXX.pdf	
	DP_FunctionalUnit_XXXXXXXX _TDXX.png	
	DP_FunctionalUnit_XXXXXXXX _Doc.txt (can be any file format)	
	Is working	

Student Name: _____

Student ID: _____

_____ _____

Date Signature