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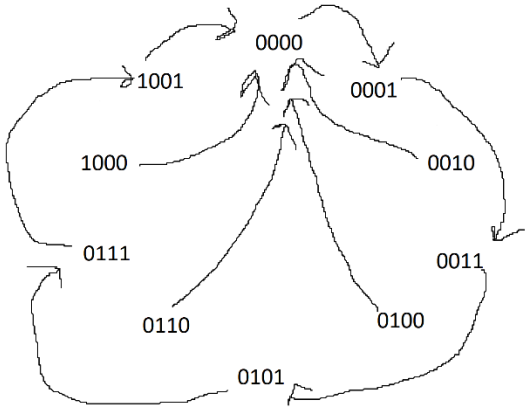
EECE.2650 Logic Design

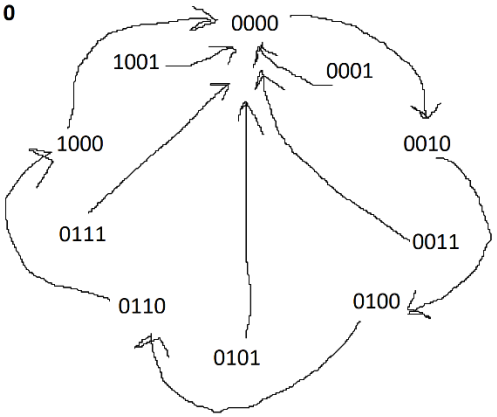
Assignment 4

State Diagram:

even_odd = 1



even_odd = 0



10-15 are don’t-care conditions

State/Transition Table:

PS ($Q_3Q_2Q_1Q_0$)	NS ($Q_3^+Q_2^+Q_1^+Q_0^+$)	
	even_odd = 0	even_odd = 1
0 0 0 0	0 0 1 0	0 0 0 1
0 0 0 1	0 0 0 0	0 0 1 1
0 0 1 0	0 1 0 0	0 0 0 1
0 0 1 1	0 0 0 0	0 1 0 1
0 1 0 0	0 1 1 0	0 0 0 1
0 1 0 1	0 0 0 0	0 1 1 1
0 1 1 0	1 0 0 0	0 0 0 1
0 1 1 1	0 0 0 0	1 0 0 1
1 0 0 0	0 0 0 0	0 0 0 1
1 0 0 1	0 0 0 0	0 0 0 1
1 0 1 0	0000 (Don't care)	0001 (Don't care)
1 0 1 1	0000 (Don't care)	0001 (Don't care)
1 1 0 0	0000 (Don't care)	0001 (Don't care)
1 1 0 1	0000 (Don't care)	0001 (Don't care)
1 1 1 0	0000 (Don't care)	0001 (Don't care)
1 1 1 1	0000 (Don't care)	0001 (Don't care)

$Q_3^+{}_{even\_odd = 0}$ = SUMOF m(6) + d(14)

$Q_3^+{}_{even\_odd = 1}$ = SUMOF m(7) + d(15)

$Q_2^+{}_{even\_odd = 0}$ = SUMOF m(2, 4) + d(10, 12)

$Q_2^+{}_{even\_odd = 1}$ = SUMOF m(3, 5) + d(11, 13)

$Q_1^+{}_{even\_odd = 0}$ = SUMOF m(0, 4)

$Q_1^+{}_{even\_odd = 1}$ = SUMOF m(1, 5)

$Q_0^+{}_{even\_odd = 0}$ = 0

$Q_0^+{}_{even\_odd = 1}$ = SUMOF m(0, 1, 2, 3, 4, 5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15) = 1

KMAPS:

Q_3^+

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	0	1
11	d	d	d	d
10	0	0	d	d

even_odd = 0

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	d	d	d	d
10	0	0	d	d

even_odd = 1

Q_2^+

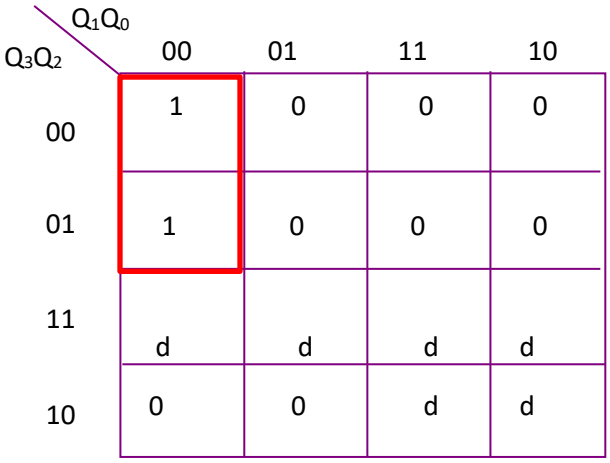
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	1
01	1	0	0	0
11	d	d	d	d
10	0	0	d	d

even_odd = 0

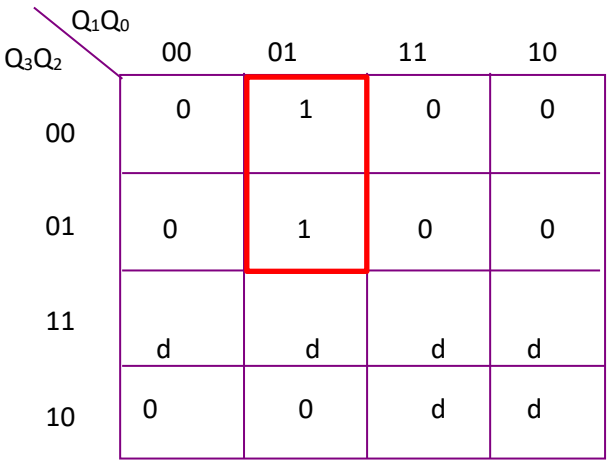
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	1	0
01	0	1	0	0
11	d	d	d	d
10	0	0	d	d

even_odd = 1

Q_1^+

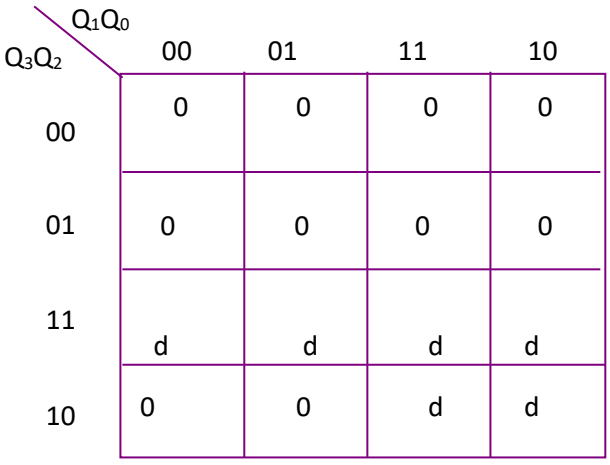


even_odd = 0

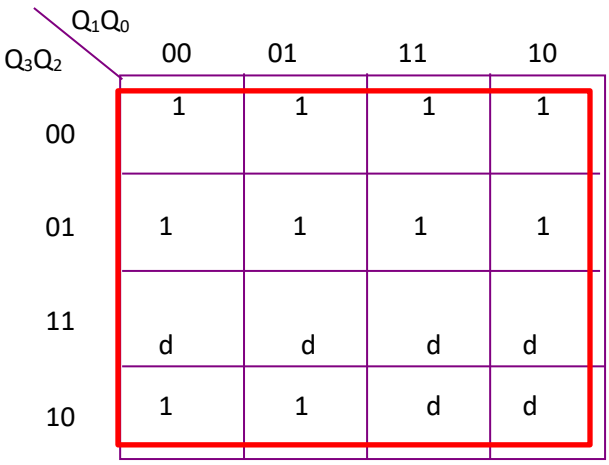


even_odd = 1

Q_0^+



even_odd = 0



even_odd = 1

Minimal SOP for DFFs:

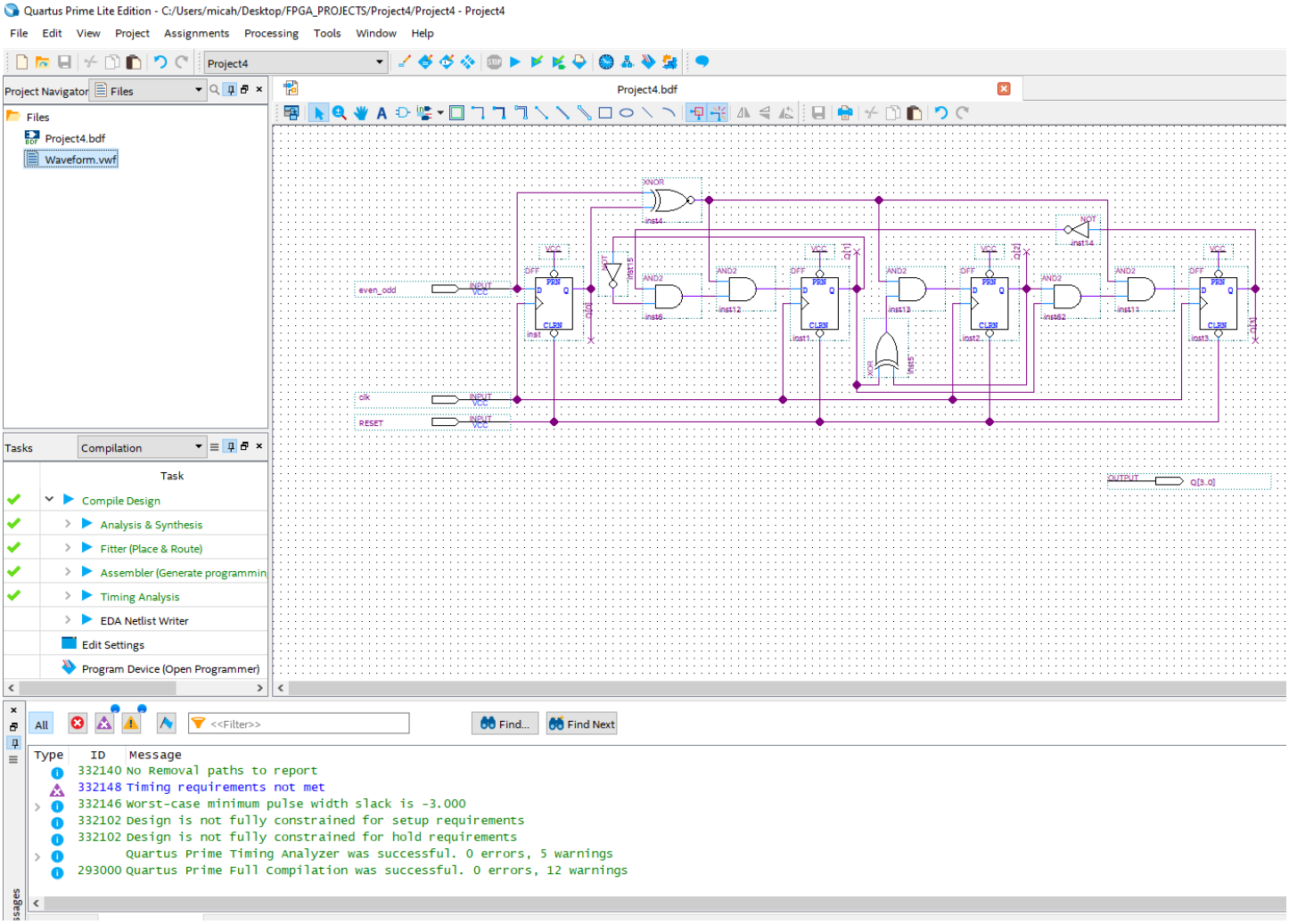
Q_3^+ = **(Q2 AND Q1) AND (even_odd XNOR Q0)**

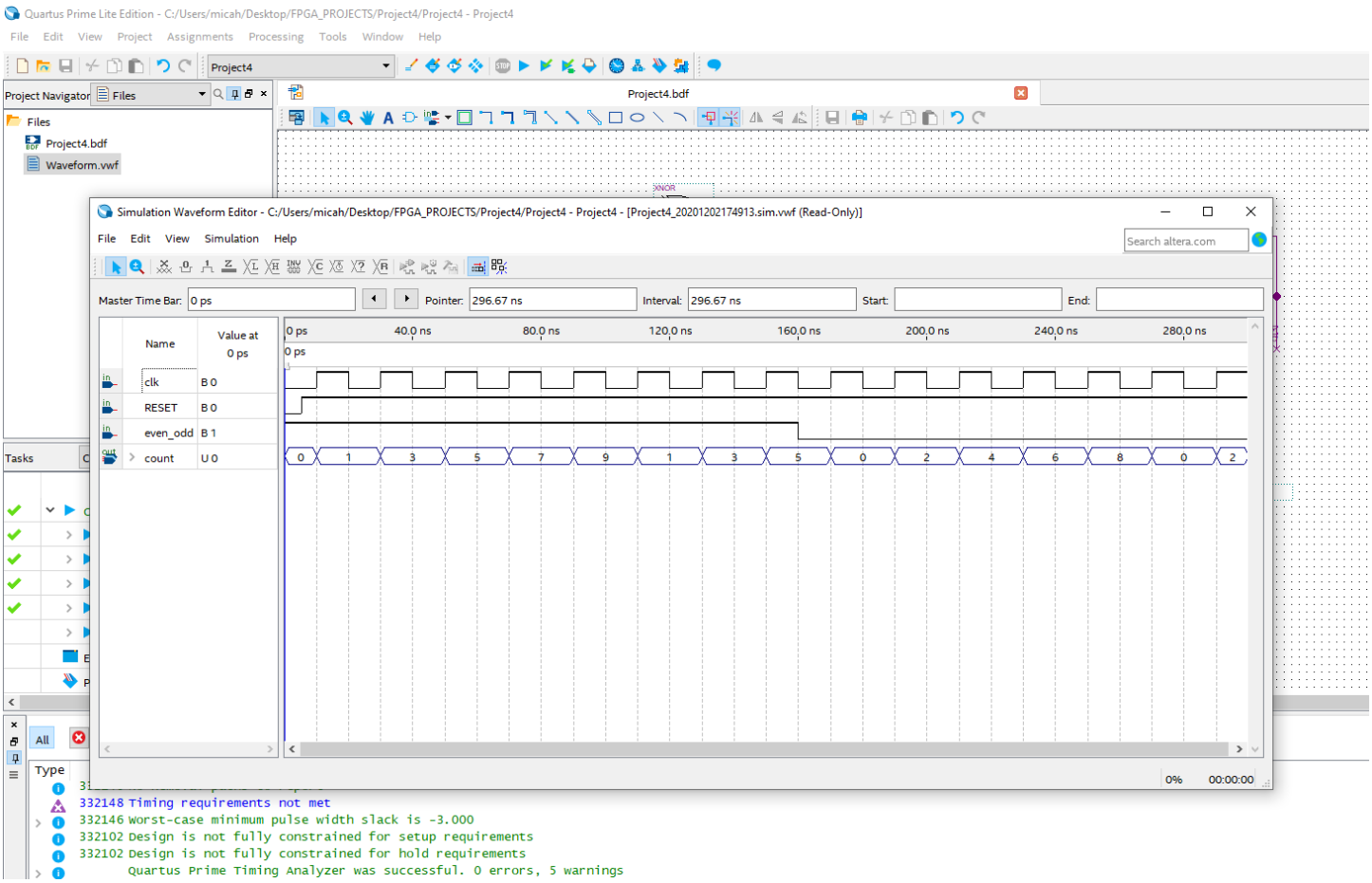
Q_2^+ = **(Q2 XOR Q1) AND (even_odd XNOR Q0)**

Q_1^+ = **(NOT(Q3) AND NOT(Q1)) AND (even_odd XNOR Q0)**

Q_0^+ = **even_odd**

Block Diagram and Simulation Result: (make sure your filename path is readable in your screenshots)




Quartus Prime Lite Edition - C:/Users/micah/Desktop/FPGA_PROJECTS/Project4/Project4 - Project4
File Edit View Project Assignments Processing Tools Window Help
Project4
Project Navigator
Files
Project4.bdf
Waveform.vwf
Simulation Waveform Editor - C:/Users/micah/Desktop/FPGA_PROJECTS/Project4/Project4 - Project4 - [Project4_20201202174913.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 296.67 ns
Interval: 296.67 ns
Start:
End:
Name
Value at 0 ps
clk B 0
RESET B 0
even_odd B 1
count U 0
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
0 1 3 5 7 9 1 3 5 0 2 4 6 8 0 2
0%
00:00:00
Tasks
All
Type
332148 Timing requirements not met
332146 Worst-case minimum pulse width slack is -3.000
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings