**LAB NOTE**

**Subject: Digital Design Principles**

**Topic: And Gate**

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# Objectives

* To be familiar with Quartus.
* To write a VHDL and Verilog code for And Gate.
* Push the code to SCEMA5F31C6N board.

# Theory

## Theory

AND gate is a simple gate that has 2 inputs and 1 output. The outputs will be true (1) only if all its inputs are true (1).

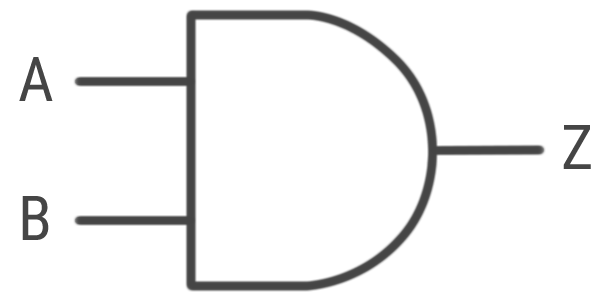


Figure 2‑1: And Gate

## Truth table

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Table 2‑1: Truth table for And Gate

## Boolean expression

# VHDL and Verilog

## VHDL code

library ieee;

use ieee.std\_logic\_1164.all; --should be same through all the lab, except comparator.

-- declaring input and output

entity MTran\_Lab1\_VHDL\_AndGate is

port

-- a,b are SW1 and SW2, output is LEDR0

(

a, b : in std\_logic;

output : out std\_logic --end of declaration no more ';'

);

end MTran\_Lab1\_VHDL\_AndGate;

-- describing the relationship between output and input

architecture behavioral of MTran\_Lab1\_VHDL\_AndGate is --'behavioral' is a block name (must not same name in library)

begin

output <= a and b; -- <=: assigning variable 'output'

end behavioral;

## Verilog code

module MTran\_Lab1\_Verilog\_AndGate(a,b,y);

input a,b;

output y;

and (y,a,b);

endmodule

# Pin Planner

## Input and Output

A close-up of a circuit board

Description automatically generated

Figure 4‑1: SCEMA5F31C6N board

Assigning:

a: SW0

b: SW1

output: LEDR0

From the DE1\_SoC\_User\_Manual,

SW0: Pin\_AB12

SW1: Pin\_AC12

LEDR0: Pin\_V6

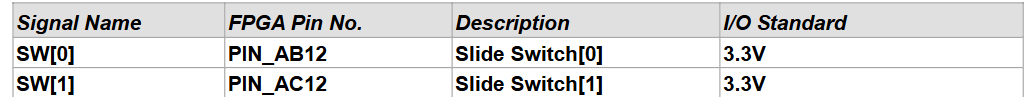
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Figure 4‑2: SW0 and SW1 Pin No

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Figure 4‑3: LEDR0's Pin No

A screenshot of a computer

Description automatically generated

Figure 4‑4: Quartus's Pin Planner

# Result

**REFERENCES**