**LAB NOTE**

**Subject: Digital Design Principles**

**Topic: Magnitude Comparator**

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# Objectives

* Design a Magnitude Comparator using Quartus software.
* Write a VHDL and Verilog code from the design.
* Push the code and run to the SCEMA5F31C6N board.

# Theory and Design

## Theory

Magnitude Comparator is a circuit that compare 2 inputs A and B and give out either 3 output ‘100’, ‘010’ and ‘001’ which should represent Greater Than, Equal, Less Than.

## Requirement

* Use VHDL and Verilog to implement a Magnitude Comparator and display to LED [0:2].
* Introduction to the VHDL Case statement.
* **Above and beyond:** Adding mode: Clock count up from 00:00:00 to 23:59:59 with 2 speed normal speed and 100x speed.

## Solution

To design this system, first need to identify input and output:

* Input will be from SW0 to SW7.
* Output will be LED[2:0].

Then identify what the output will be, from the 2 inputs,

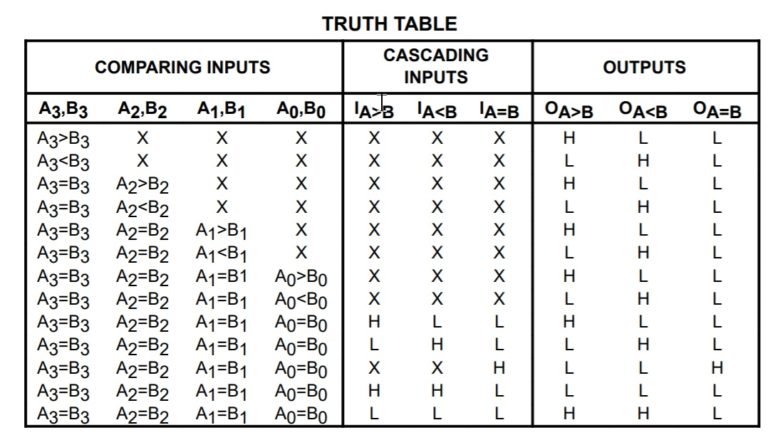


Figure 2‑1: Magnitude Comparator’s Truth Table

# VHDL and Verilog

## VHDL code

### Top entity

**library** ieee;

**use** ieee.std\_logic\_1164.**ALL**;

**use** IEEE.NUMERIC\_STD.**ALL**;

**entity** MTran\_Lab7\_VHDL\_MagnitudeComparator **is**

**port**

(

-- Inputs

CLOCK\_50 : **in** std\_logic;

A : **in** std\_logic\_vector (3 **downto** 0);

B : **in** std\_logic\_vector (3 **downto** 0);

mode : **in** std\_logic;

-- Outputs

LED : **out** std\_logic\_vector (2 **downto** 0);

HEX0 : **out** std\_logic\_vector (6 **downto** 0);

HEX1 : **out** std\_logic\_vector (6 **downto** 0);

HEX2 : **out** std\_logic\_vector (6 **downto** 0);

HEX3 : **out** std\_logic\_vector (6 **downto** 0);

HEX4 : **out** std\_logic\_vector (6 **downto** 0);

HEX5 : **out** std\_logic\_vector (6 **downto** 0)

);

**end** **entity**;

**architecture** Behavioral **of** MTran\_Lab7\_VHDL\_MagnitudeComparator **is**

-- Module declaration

**component** MTran\_Lab7\_VHDL\_Timer **is**

**port**

(

-- Inputs

Clk : **in** std\_logic;

Enable : **in** std\_logic;

-- Outputs

Seconds : **inout** integer;

Minutes : **inout** integer;

Hours : **inout** integer

);

**end** **component**;

-- Singal declaration

**signal** intA : integer := 0;

**signal** intB : integer := 0;

**signal** Enable : std\_logic;

**signal** Seconds : integer := 0;

**signal** Minutes : integer := 0;

**signal** Hours : integer := 0;

-- Function

**function** SevenSegmentDisplay(Number : integer) **return** std\_logic\_vector **is**

**begin**

**case** (Number) **is**

**when** 0 => **return** "1000000";

**when** 1 => **return** "1111001";

**when** 2 => **return** "0100100";

**when** 3 => **return** "0110000";

**when** 4 => **return** "0011001";

**when** 5 => **return** "0010010";

**when** 6 => **return** "0000010";

**when** 7 => **return** "1111000";

**when** 8 => **return** "0000000";

**when** 9 => **return** "0010000";

**when** **others** => **return** "1111111";

**end** **case**;

**end** SevenSegmentDisplay;

-- Main code

**begin**

-- Module instatiate

module\_timer: MTran\_Lab7\_VHDL\_Timer

**port** **map**

(

Clk => CLOCK\_50,

Enable => Enable,

Seconds => Seconds,

Minutes => Minutes,

Hours => Hours

);

-- Process

**process**(CLOCK\_50, Seconds, Minutes, Hours, A, B) **is**

**begin**

**if** mode = '0' **then**

-- Disable Timer

Enable <= '0';

-- Reset HEX2

HEX2 <= "1111111";

-- Convert A and B from std\_logic to integer

intA <= to\_integer(unsigned(A));

intB <= to\_integer(unsigned(B));

-- Display A and B in decimal

-- A

HEX0 <= SevenSegmentDisplay(intA **mod** 10);

HEX1 <= SevenSegmentDisplay(intA / 10);

-- B

HEX4 <= SevenSegmentDisplay(intB **mod** 10);

HEX5 <= SevenSegmentDisplay(intB / 10);

-- Compare A and B

**if** intA > intB **then**

LED <= "100";

HEX3 <= "0100111";

**elsif** intA = intB **then**

LED <= "010";

HEX3 <= "0110111";

**else**

LED <= "001";

HEX3 <= "0110011";

**end** **if**;

**else**

Enable <= '1';

LED <= "000";

-- Display Second

HEX0 <= SevenSegmentDisplay(Seconds **mod** 10);

HEX1 <= SevenSegmentDisplay(Seconds / 10);

-- Display Minute

HEX2 <= SevenSegmentDisplay(Minutes **mod** 10);

HEX3 <= SevenSegmentDisplay(Minutes / 10);

-- Display Hour

HEX4 <= SevenSegmentDisplay(Hours **mod** 10);

HEX5 <= SevenSegmentDisplay(Hours / 10);

**end** **if**;

**end** **process**;

**end** **architecture**;

### Component Timer

**library** ieee;

**use** ieee.std\_logic\_1164.**ALL**;

**entity** MTran\_Lab7\_VHDL\_Timer **is**

**port**

(

-- Inputs

Clk : **in** std\_logic;

Enable : **in** std\_logic;

-- Outputs

Seconds : **inout** integer := 0;

Minutes : **inout** integer := 0;

Hours : **inout** integer := 0

);

**end** **entity**;

**architecture** RTL **of** MTran\_Lab7\_VHDL\_Timer **is**

-- Signal Declaration

**signal** Ticks : integer := 0;

-- Procedure

**procedure** Increment( **signal** Counter : **inout** integer;

**constant** MaxValue : **in** integer;

**variable** ResetFlag : **out** boolean) **is**

**begin**

**if** Counter = MaxValue - 1 **then**

-- Reset Counter

Counter <= 0;

ResetFlag := True;

**else**

Counter <= Counter + 1;

ResetFlag := False;

**end** **if**;

**end** **procedure**;

**begin**

**process**(Clk, Enable) **is**

-- Variable Declaring

**variable** SecondsFlag : boolean := false;

**variable** MinutesFlag : boolean := false;

**variable** HoursFlag : boolean := false;

**constant** MaxSeconds : integer := 60;

**constant** MaxMinutes : integer := 60;

**constant** MaxHours : integer := 24;

**constant** ClockFrequency : integer := 50000000;

-- Main

**begin**

**if** Enable = '1' **then**

**if** rising\_edge(Clk) **then**

-- Increment Ticks

Increment(Ticks, ClockFrequency, SecondsFlag);

-- Increment Seconds whenever Ticks reach Clock Frequency

**if** SecondsFlag **then**

Increment(Seconds, MaxSeconds, MinutesFlag);

**end** **if**;

-- Increment Minute whenever 60 seconds

**if** SecondsFlag **and** MinutesFlag **then**

Increment(Minutes, MaxMinutes, HoursFlag);

**end** **if**;

-- Increment Hours whenever 60 minutes

**if** SecondsFlag **and** MinutesFlag **and** HoursFlag **then**

Increment(Hours, MaxHours, HoursFlag);

**end** **if**;

**end** **if**;

**end** **if**;

**end** **process**;

**end** **architecture**;

## Verilog code

### Top Module

**module MTran\_Lab7\_Verilog\_MagnitudeComparator**

(

**input** wire CLOCK\_50,

input wire [3:0] A,

input wire [3:0] B,

input mode,

input speed,

output reg [2:0] LED,

output reg [6:0] HEX0,

output reg [6:0] HEX1,

output reg [6:0] HEX2,

output reg [6:0] HEX3,

output reg [6:0] HEX4,

output reg [6:0] HEX5

)**;**

// Signals declaration

**reg** [31:0] intA**;**

**reg** [31:0] intB**;**

**reg** Enable**;**

**wire** [31:0] Seconds1**;**

**wire** [31:0] Minutes1**;**

**wire** [31:0] Hours1**;**

**wire** [31:0] Seconds2**;**

**wire** [31:0] Minutes2**;**

**wire** [31:0] Hours2**;**

// Module Instantiation

MTran\_Lab7\_Verilog\_Timer

#(

.MAXSECONDS(60),

.MAXMINUTES(60),

.MAXHOURS(24),

.CLKFREQUENCY(500000) // 500kHz => Clock 10 times faster

)

Tim1

(

.Clk(CLOCK\_50),

.Enable(Enable),

.Seconds(Seconds1),

.Minutes(Minutes1),

.Hours(Hours1)

);

MTran\_Lab7\_Verilog\_Timer

#(

.MAXSECONDS(60),

.MAXMINUTES(60),

.MAXHOURS(24),

.CLKFREQUENCY(50000000) // 50 MHz => Normal Clk

)

Tim2

(

.Clk(CLOCK\_50),

.Enable(Enable),

.Seconds(Seconds2),

.Minutes(Minutes2),

.Hours(Hours2)

);

// Function for Seven Segment Display

function [6:0] SevenSegmentDisplay;

**input** [3:0] Number**;**

**begin**

**case** **(**Number**)**

4'h0**:** SevenSegmentDisplay = 7'b1000000**;**

4'h1**:** SevenSegmentDisplay = 7'b1111001**;**

4'h2**:** SevenSegmentDisplay = 7'b0100100**;**

4'h3**:** SevenSegmentDisplay = 7'b0110000**;**

4'h4**:** SevenSegmentDisplay = 7'b0011001**;**

4'h5**:** SevenSegmentDisplay = 7'b0010010**;**

4'h6**:** SevenSegmentDisplay = 7'b0000010**;**

4'h7**:** SevenSegmentDisplay = 7'b1111000**;**

4'h8**:** SevenSegmentDisplay = 7'b0000000**;**

4'h9**:** SevenSegmentDisplay = 7'b0010000**;**

**default:** SevenSegmentDisplay = 7'b1111111**;**

**endcase**

**end**

endfunction

**always** @(posedge CLOCK\_50)

**begin**

**if** (mode == 1'b0)

**begin**

// Disable Timer

Enable = 1'b0;

// Reset HEX2

HEX2 = 7'b1111111;

// Convert A and B from std\_logic to integer

intA = A;

intB = B;

// Display A and B in decimal

// A

HEX0 = SevenSegmentDisplay(intA % 10);

HEX1 = SevenSegmentDisplay(intA / 10);

// B

HEX4 = SevenSegmentDisplay(intB % 10);

HEX5 = SevenSegmentDisplay(intB / 10);

// Compare A and B

**if** (intA > intB)

**begin**

LED = 3'b100;

HEX3 = 7'b0100111;

**end**

**else** **if** (intA == intB)

**begin**

LED = 3'b010;

HEX3 = 7'b0110111;

**end**

**else**

**begin**

LED = 3'b001;

HEX3 = 7'b0110011;

**end**

**end**

**else**

**begin**

Enable = 1'b1;

LED = 3'b000;

**if** (speed == 1'b0) //normal mode

**begin**

// Display Second

HEX0 = SevenSegmentDisplay(Seconds2 % 10);

HEX1 = SevenSegmentDisplay(Seconds2 / 10);

// Display Minute

HEX2 = SevenSegmentDisplay(Minutes2 % 10);

HEX3 = SevenSegmentDisplay(Minutes2 / 10);

// Display Hour

HEX4 = SevenSegmentDisplay(Hours2 % 10);

HEX5 = SevenSegmentDisplay(Hours2 / 10);

**end**

**else** **if** (speed == 1'b1)

**begin**

// Display Second

HEX0 = SevenSegmentDisplay(Seconds1 % 10);

HEX1 = SevenSegmentDisplay(Seconds1 / 10);

// Display Minute

HEX2 = SevenSegmentDisplay(Minutes1 % 10);

HEX3 = SevenSegmentDisplay(Minutes1 / 10);

// Display Hour

HEX4 = SevenSegmentDisplay(Hours1 % 10);

HEX5 = SevenSegmentDisplay(Hours1 / 10);

**end**

**end**

**end**

endmodule

### Module Timer

**module MTran\_Lab7\_Verilog\_Timer**

#(

**parameter** MAXSECONDS = 60,

parameter MAXMINUTES = 60,

parameter MAXHOURS = 24,

parameter CLKFREQUENCY = 50000000

)

(

input wire Clk,

input wire Enable,

inout reg [31:0] Seconds,

inout reg [31:0] Minutes,

inout reg [31:0] Hours

)**;**

// Signal Declaration

**reg** [31:0] Ticks = 0**;**

// Main Logic

**always** @(posedge Clk)

**begin**

**if** (Enable)

**begin**

// Increment Ticks

Ticks = Ticks + 1;

**if** (Ticks == CLKFREQUENCY - 1)

**begin**

Ticks = 0;

Seconds = Seconds + 1;

**end**

**if** (Seconds == MAXSECONDS)

**begin**

Seconds = 0;

Minutes = Minutes + 1;

**end**

**if** (Minutes == MAXMINUTES)

**begin**

Minutes = 0;

Hours = Hours + 1;

**end**

**if** (Hours == MAXHOURS)

**begin**

Hours = 0;

**end**

**end**

**end**

endmodule

# Pin Planner

## Input and Output

A close-up of a circuit board

Description automatically generated

Figure 4‑1: SCEMA5F31C6N board

Assigning:

SW[0]: SW0

SW[1]: SW1

SW[2]: SW2

Mode[0]: SW7

Mode[1]: SW8

EN: SW9

LED[0]: LEDR0

LED[1]: LEDR1

LED[2]: LEDR2

LED[3]: LEDR3

LED[4]: LEDR4

LED[5]: LEDR5

LED[6]: LEDR6

LED[7]: LEDR7

HEX0[0]: HEX0[0]

HEX0[1]: HEX0[1]

HEX0[2]: HEX0[2]

HEX0[3]: HEX0[3]

HEX0[4]: HEX0[4]

HEX0[5]: HEX0[5]

HEX0[6]: HEX0[6]

From the DE1\_SoC\_User\_Manual,

A screenshot of a slide switch

Description automatically generated

Figure 4‑2: SW0 and SW1 Pin No

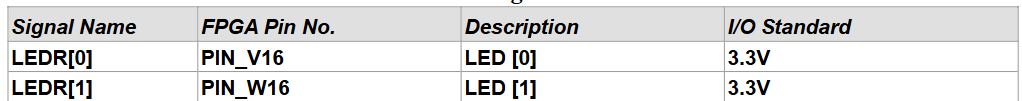


Figure 4‑3: LEDR0's Pin No

 A group of black text

Description automatically generated

Figure 4‑4: HEX's Pin No

# Result

A computer chip on a desk

Description automatically generated

Figure 5‑1: When input = ‘000’.

SW2 = 0, SW1 = 0, SW0 = 0 which should be 0, **LED0** asserted and the 7 segment LED displaying **0**.

A close up of a computer

Description automatically generated

Figure 5‑2: When input = ‘111’

SW2 = 1, SW1 = 1, SW0 = 1 which should be 7, **LED7** asserted and the 7 segment LED displaying **7**.

A close up of a computer chip

Description automatically generated

Figure 5‑3: When input ‘101’

SW2 = 1, SW1 = 0, SW0 = 1 which should be 5, **LED5** asserted and the 7 segment LED displaying **5**.

**Different mode:**

* **Complement mode:**

A close up of a computer

Description automatically generated

Figure 5‑4: Input ‘101’ with Complement mode

In this mode, rather than LED5 assert, all other LED except LED5 asserted. To activate this mode SW [8:7] = ‘01’.

* **Multiline Mode:**

A close up of a circuit board

Description automatically generated

Figure 5‑5: Input ‘101’ with Multiline mode

In this mode, when input is ‘101’ which is **5**, LED0 to LED5 lit up. To activate this mode SW [8:7] = ‘10’.

* **Complement Multiline Mode:**

A close up of a circuit board

Description automatically generated

Figure 5‑6: Result for adding them up

In this mode, it take the output of Multiline Mode and complemented it. To activate this mode SW [8:7] = ‘11’

**REFERENCES**