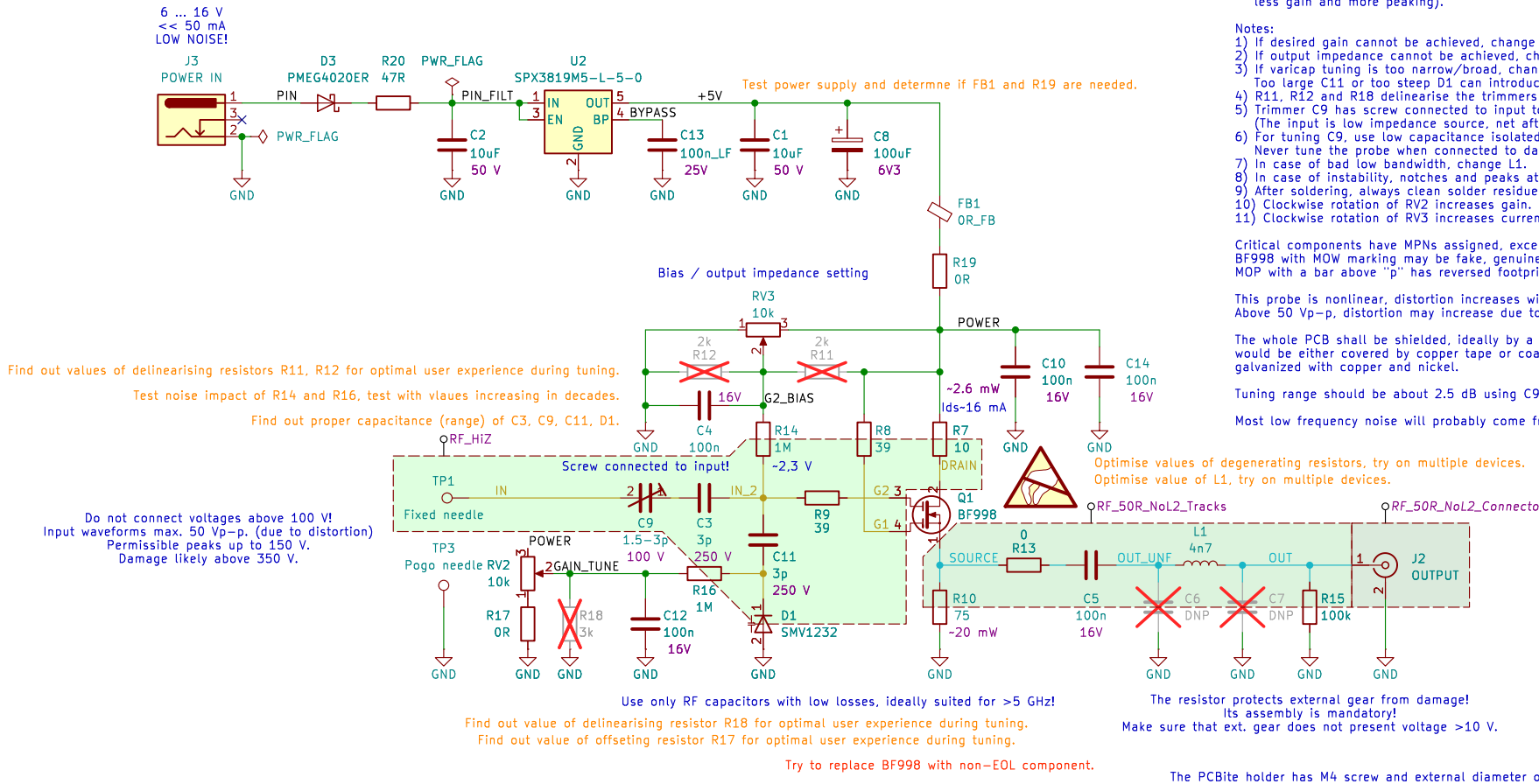

Calibration process:
1) Perform this calibration in ESD safe environment!
   Short the input, power up the probe (with VNA disconnected).
   Not shorting the input may affect the measurement.
2) Connect VNA, measure output impedance of the probe.
   Tune the bias on gate 2 to get 50 Ohm output.
3) Disconnect VNA, reconnect it to measure S21 of the probe.
   (If varicap tuning is assembled, set it to highest possible voltage.)
   Tune the input capacitor to get 10:1 (–20 dB) response.
4) (If assembled, use the varicap tuning to fine–tune the gain).
   If varicap tuning is not used, change bias to fine–tune gain.
5) Re–measure the output impedance. If out of spec, repeat these steps.
   This is needed because the parameters are not fully independent.
   G2 bias has effect on peaking around roll–off (lower voltage =
   less gain and more peaking).

Notes:
1) If desired gain cannot be achieved, change C3.
2) If output impedance cannot be achieved, change R10.
3) If varicap tuning is too narrow/broad, change C11.
   Too large C11 or too steep D1 can introduce non–linearity.
4) R11, R12 and R18 delinearise the trimmers to make tuning easier.
5) Trimmer C9 has screw connected to input to make tuning easier.
   (The input is low impedance source, net after the capacitor is not.)
6) For tuning C9, use low capacitance isolated tuning screwdriver.
   Never tune the probe when connected to dangerous voltages!
7) In case of bad low bandwidth, change L1.
8) In case of instability, notches and peaks at >500 MHz, change R7–9.
9) After soldering, always clean solder residue!
10) Clockwise rotation of RV2 increases gain.
11) Clockwise rotation of RV3 increases current, decreases impedance.

Critical components have MPNs assigned, except for BF998 (look on eBay).
BF998 with MOW marking may be fake, genuine are MOs or MOp :–)
MOP with a bar above "p" has reversed footprint!

This probe is nonlinear, distortion increases with measured amplitude.
Above 50 Vp–p, distortion may increase due to protective diodes on G2.

The whole PCB shall be shielded, ideally by a 3D printed cover which would be either covered by copper tape or coated with carbon and galvanized with copper and nickel.

Tuning range should be about 2.5 dB using C9 and 1 dB using D1.

Most low frequency noise will probably come from thermal noise of R14.

The PCBite holder has M4 screw and external diameter of 13 mm.
Impedance controlled traces are designed for JLC PCB JLC04161H–3313 stackup.
50R traces need to have L2 removed and coupled to L3.

Version	Previous version	Description of change	Drawn by	Checked by
1.0.0	N/A	Initial version	Petr Polášek	Petr Polášek

Author: Petr Polášek

Sheet: /
File: LowCapacitanceProbe.kicad_sch

Title: Low Capacitance (<1 pF) 10:1 AC 1+ GHz Probe

Size: A4	Date: 2025–04–11	**Rev: 1.0.0**
KiCad E.D.A. 9.0.1–193–gcc69f8b9ae		Id: 1/1