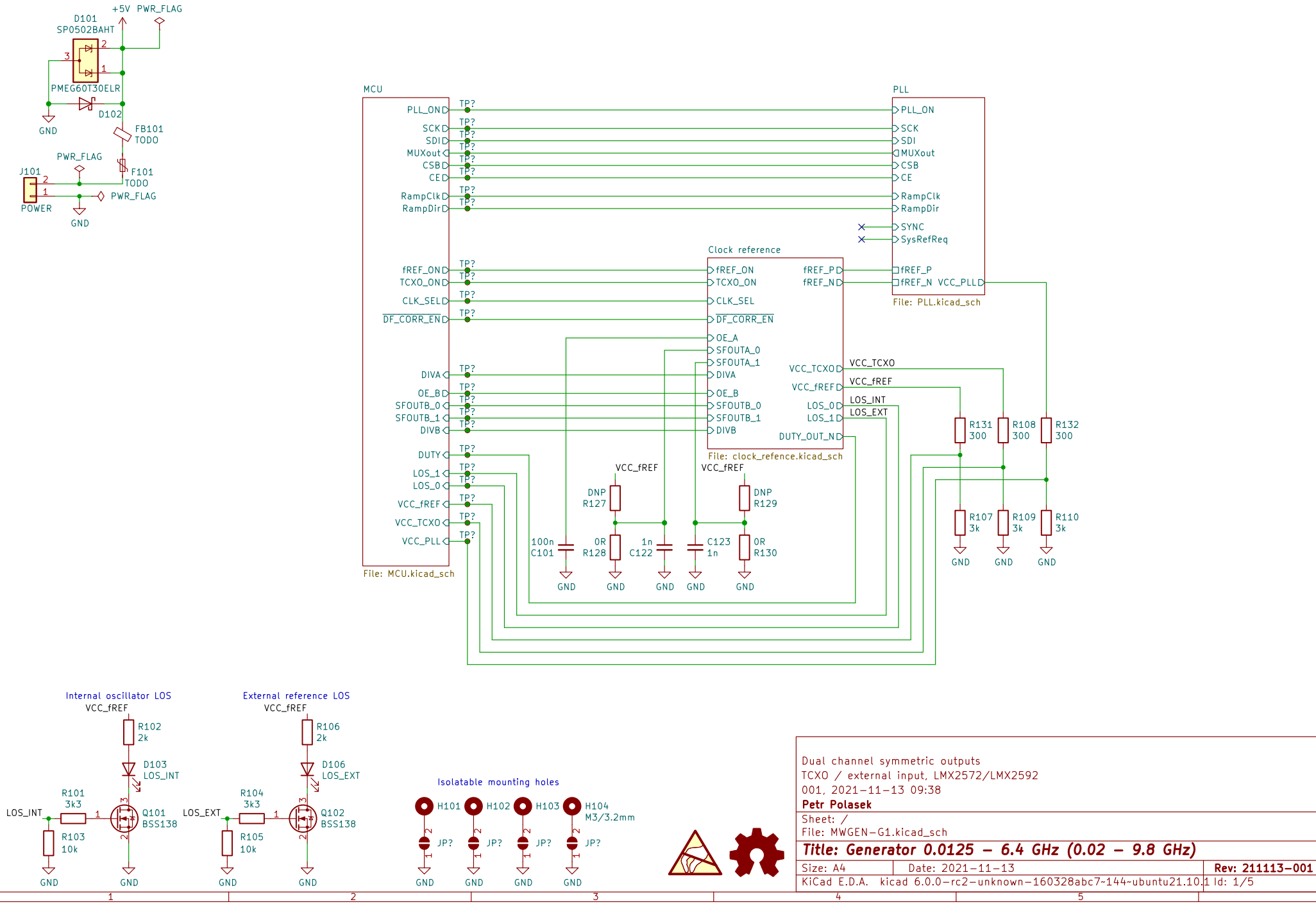
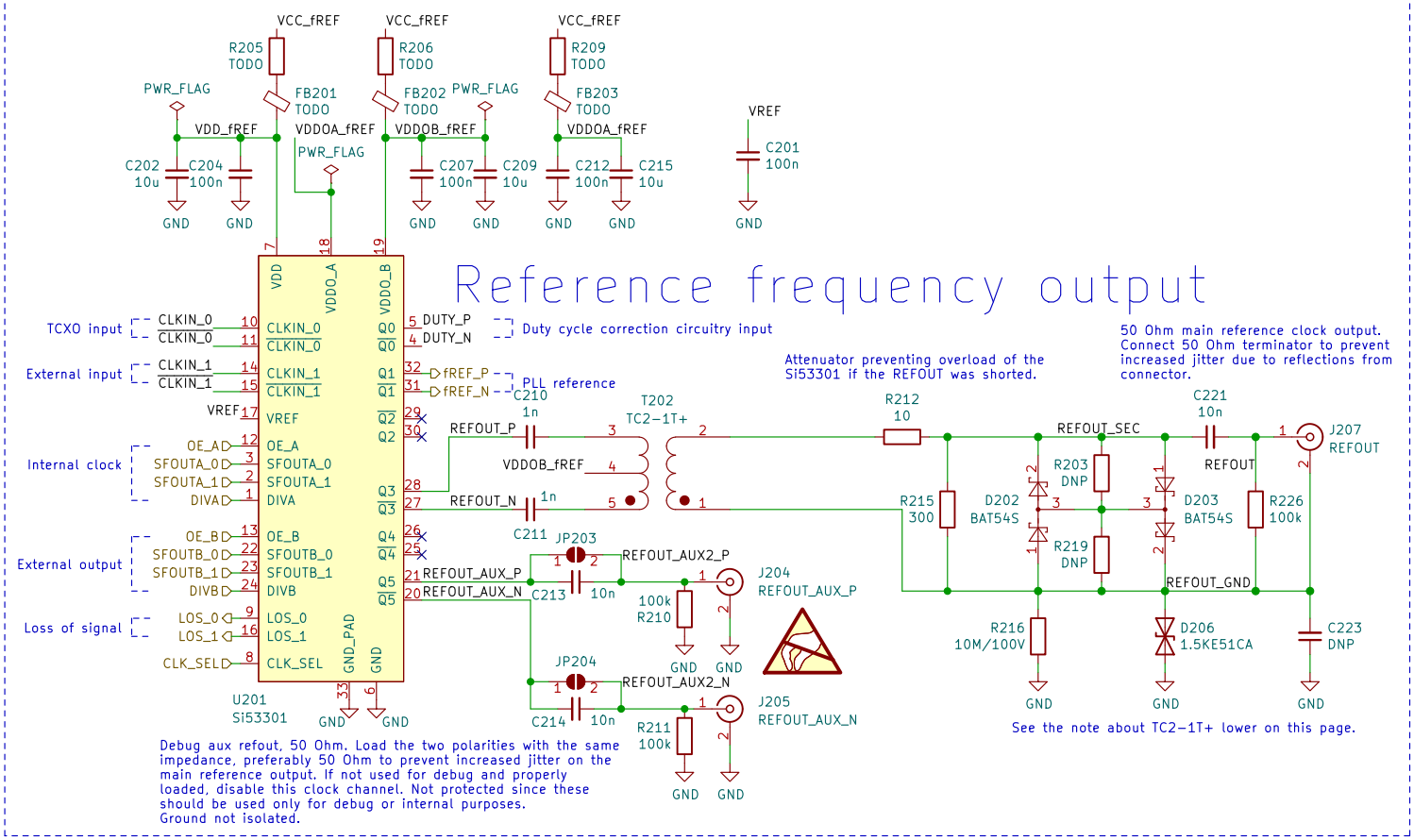
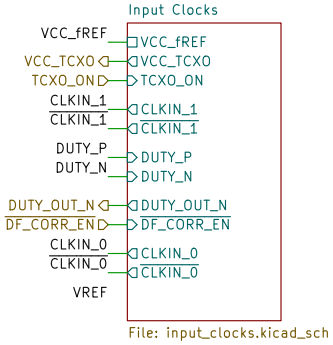
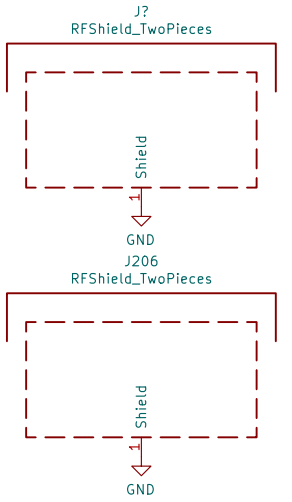

D101
SP0502BAHT
+5V
PWR_FLAG
PMEG60T30ELR
D102
GND
FB101
TODO
PWR_FLAG
J101
F101
TODO
POWER
PWR_FLAG
GND
MCU
PLL_ON
SCK
SDI
MUXout
CSB
CE
RampClk
RampDir
fREF_ON
TCXO_ON
CLK_SEL
DF_CORR_EN
DIVA
OE_B
SFOUTB_0
SFOUTB_1
DIVB
DUTY
LOS_1
LOS_0
VCC_fREF
VCC_TCXO
VCC_PLL
TP?
File: MCU.kicad_sch
PLL
PLL_ON
SCK
SDI
MUXout
CSB
CE
RampClk
RampDir
SYNC
SysRefReq
fREF_P
fREF_N
VCC_PLL
File: PLL.kicad_sch
Clock reference
fREF_ON
TCXO_ON
CLK_SEL
DF_CORR_EN
OE_A
SFOUTA_0
SFOUTA_1
DIVA
OE_B
SFOUTB_0
SFOUTB_1
DIVB
fREF_P
fREF_N
VCC_TCXO
VCC_fREF
LOS_0
LOS_1
DUTY_OUT_N
File: clock_refence.kicad_sch
VCC_TCXO
VCC_fREF
LOS_INT
LOS_EXT
R131 300
R108 300
R132 300
R107 3k
R109 3k
R110 3k
DNP R127
DNP R129
100n C101
0R R128
1n C122
C123 1n
0R R130
Internal oscillator LOS
External reference LOS
R102 2k
D103 LOS_INT
R101 3k3
Q101 BSS138
R103 10k
R106 2k
D106 LOS_EXT
R104 3k3
Q102 BSS138
R105 10k
Isolatable mounting holes
H101
H102
H103
H104 M3/3.2mm
JP?
Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek
Sheet: /
File: MWGEN-G1.kicad_sch
Title: Generator 0.0125 - 6.4 GHz (0.02 - 9.8 GHz)
Size: A4
Date: 2021-11-13
Rev: 211113-001
KiCad E.D.A. kicad 6.0.0-rc2-unknown-160328abc7~144~ubuntu21.10.1 Id: 1/5

Multiplexer / buffer

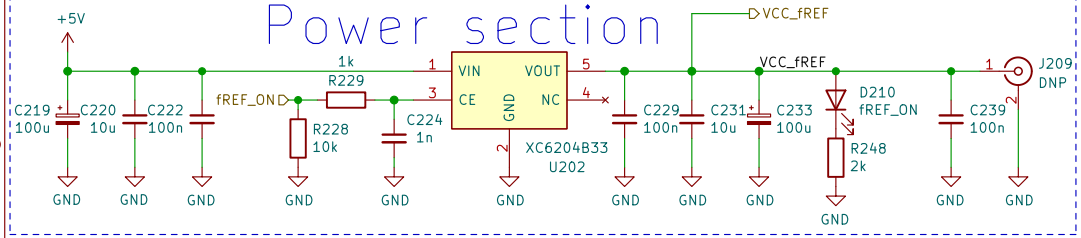


Reference frequency output





Power section



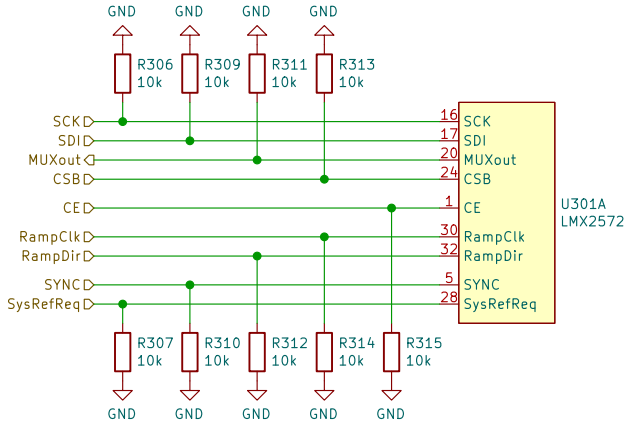
Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek

Sheet: /Clock reference/
File: clock_refence.kicad_sch

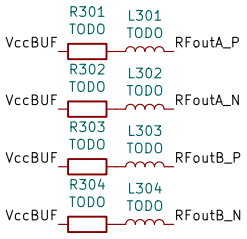
Title: Generator 0.0125 – 6.4 GHz (0.02 – 9.8 GHz)

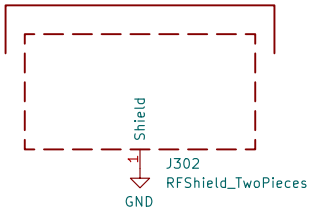
Size: A4	Date: 2021-11-13	**Rev: 211113-001**
KiCad E.D.A. kicad 6.0.0-rc2-unknown-160328abc7~144~ubuntu21.10.1	Id: 2/5	

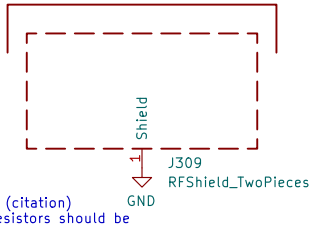
Communication section



Place these pullups only in case LMX2592 is used.
Do not place them when LMX2572 is used!

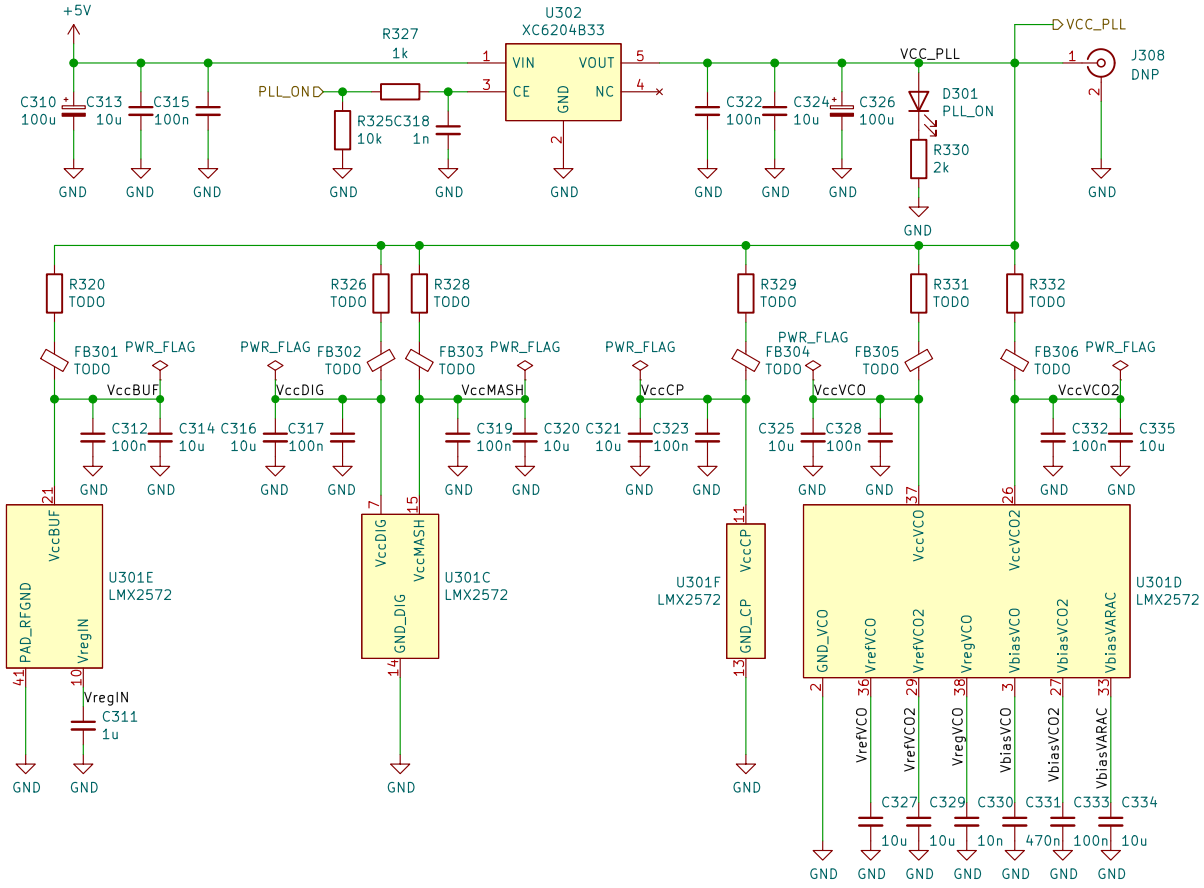




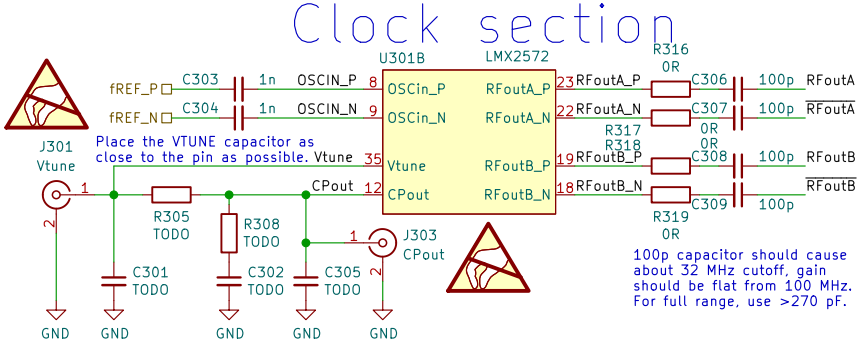


The output impedance of LMX2572 is "... just a few ohms." (citation)
The impedance should be measured and according series resistors should be placed to get 50R output. Place the resistors as close as possible to the PLL.
https://e2e.ti.com/support/clock-and-timing/f/48/t/833789?LMX2572-LMX2572-RF-output-impedance-
For LMX2592, place 0R resistors.

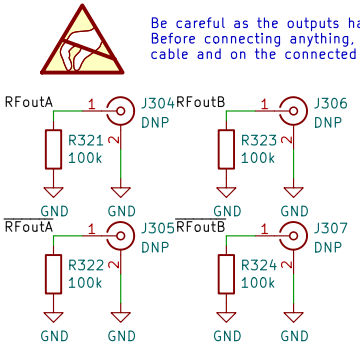
Power section



Clock section



100p capacitor should cause about 32 MHz cutoff, gain should be flat from 100 MHz. For full range, use >270 pF.

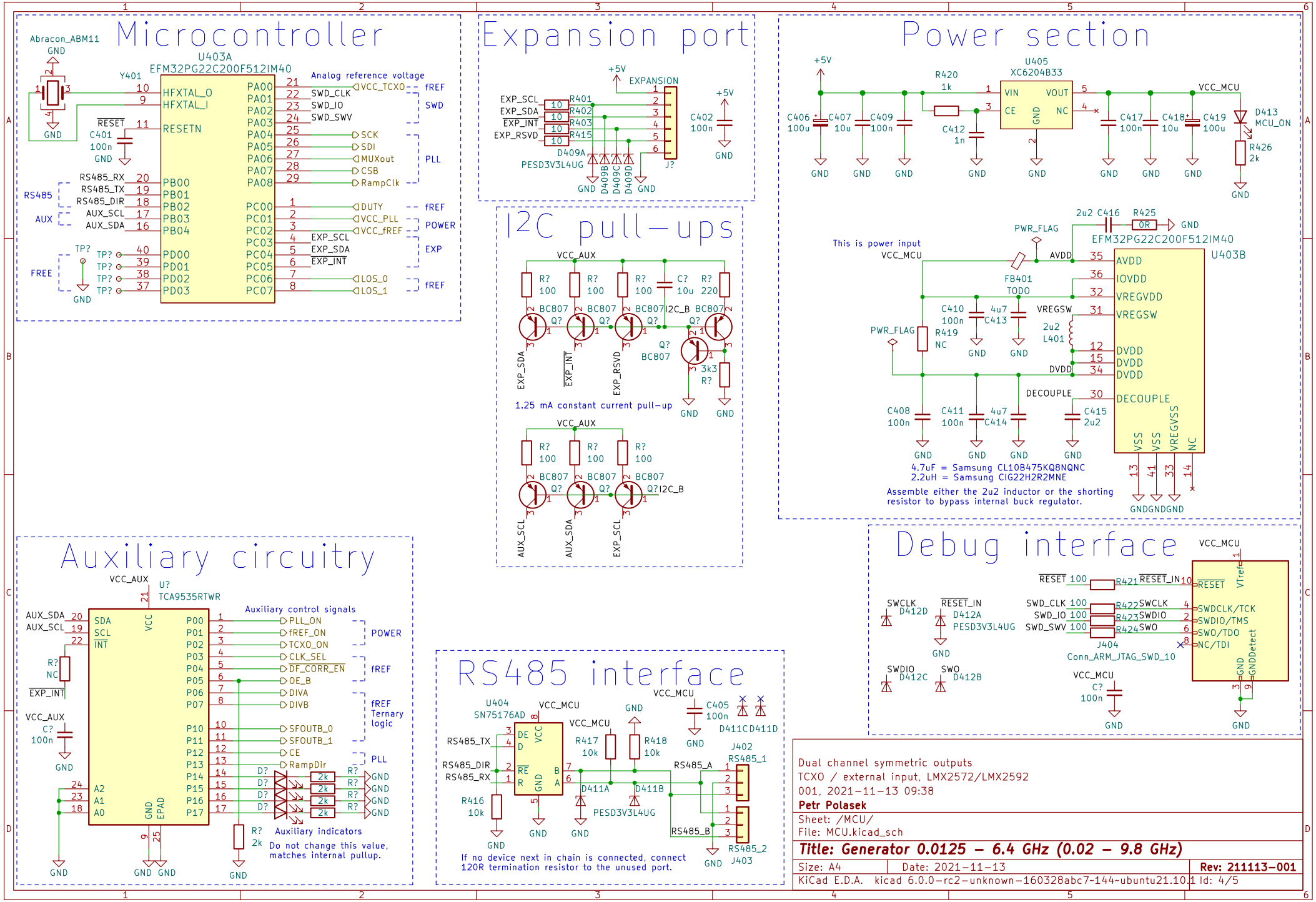


Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek

Sheet: /PLL/
File: PLL.kicad_sch

Title: Generator 0.0125 – 6.4 GHz (0.02 – 9.8 GHz)

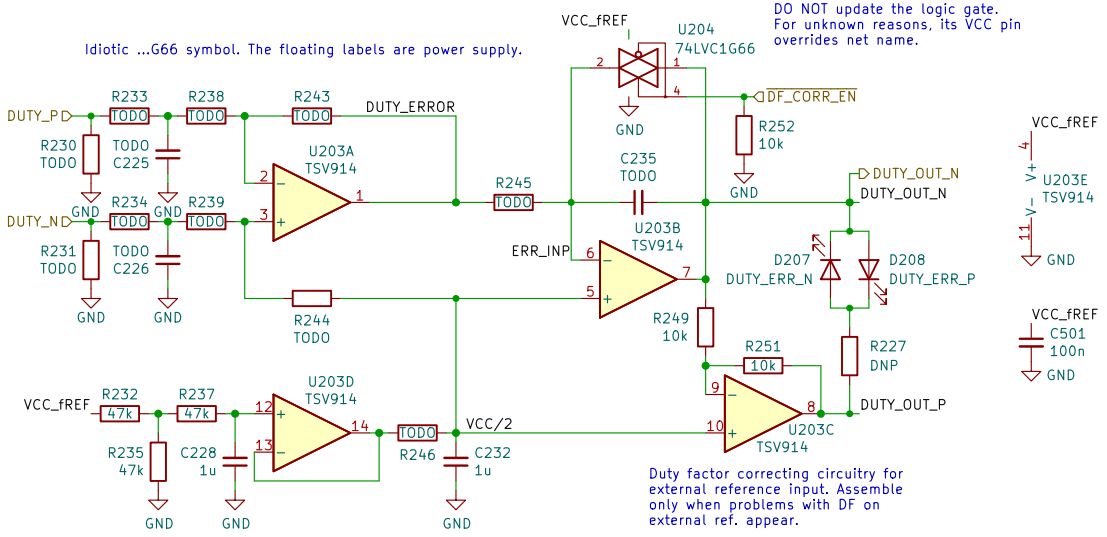
Size: A4	Date: 2021-11-13	**Rev: 211113-001**
KiCad E.D.A. kicad 6.0.0-rc2-unknown-160328abc7~144~ubuntu21.10.1	Id: 3/5	


Microcontroller
Abracon_ABM11
U403A
EFM32PG22C200F512IM40
Y401
HFXTAL_O
HFXTAL_I
RESETN
PA00
PA01
PA02
PA03
PA04
PA05
PA06
PA07
PA08
PB00
PB01
PB02
PB03
PB04
PC00
PC01
PC02
PC03
PC04
PC05
PC06
PC07
PD00
PD01
PD02
PD03
Analog reference voltage
VCC_TCXO
SWD_CLK
SWD_IO
SWD_SWV
SCK
SDI
MUXout
CSB
RampClk
DUTY
VCC_PLL
VCC_fREF
EXP_SCL
EXP_SDA
EXP_INT
LOS_0
LOS_1
fREF
SWD
PLL
POWER
EXP
RS485
AUX
FREE
RS485_RX
RS485_TX
RS485_DIR
AUX_SCL
AUX_SDA
Expansion port
EXPANSION
J?
EXP_RSVD
PESD3V3L4UG
D409A
D409B
D409C
D409D
+5V
Power section
U405
XC6204B33
VIN
VOUT
CE
NC
VCC_MCU
D413
MCU_ON
This is power input
PWR_FLAG
FB401
TODO
EFM32PG22C200F512IM40
U403B
AVDD
IOVDD
VREGVDD
VREGSW
DVDD
DECOUPLE
VSS
VREGVSS
4.7uF = Samsung CL10B475KQ8NQNC
2.2uH = Samsung CIG22H2R2MNE
Assemble either the 2u2 inductor or the shorting resistor to bypass internal buck regulator.
I2C pull-ups
VCC_AUX
BC807
I2C_B
1.25 mA constant current pull-up
Auxiliary circuitry
U?
TCA9535RTWR
Auxiliary control signals
PLL_ON
fREF_ON
TCXO_ON
CLK_SEL
DF_CORR_EN
OE_B
DIVA
DIVB
SFOUTB_0
SFOUTB_1
CE
RampDir
Auxiliary indicators
Do not change this value, matches internal pullup.
fREF Ternary logic
RS485 interface
U404
SN75176AD
RS485_TX
RS485_RX
RS485_DIR
RS485_A
RS485_B
RS485_1
RS485_2
J402
J403
If no device next in chain is connected, connect 120R termination resistor to the unused port.
Debug interface
SWCLK
SWDIO
SWO
RESET_IN
SWD_CLK
SWD_IO
SWD_SWV
J404
Conn_ARM_JTAG_SWD_10
SWDCLK/TCK
SWDIO/TMS
SWO/TDO
NC/TDI
GNDDetect
VTref
Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek
Sheet: /MCU/
File: MCU.kicad_sch
Title: Generator 0.0125 – 6.4 GHz (0.02 – 9.8 GHz)
Size: A4
Date: 2021-11-13
Rev: 211113-001
KiCad E.D.A. kicad 6.0.0-rc2-unknown-160328abc7~144~ubuntu21.10.1 Id: 4/5

Duty factor / DC corrector

Idiotic ...G66 symbol. The floating labels are power supply.

DO NOT update the logic gate.
For unknown reasons, its VCC pin
overrides net name.



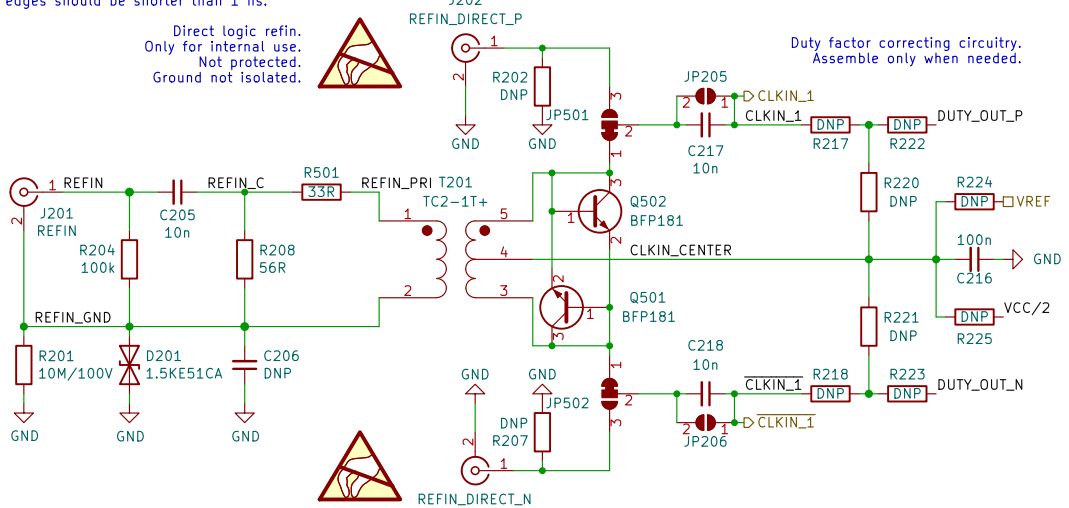
Duty factor correcting circuitry for
external reference input. Assemble
only when problems with DF on
external ref. appear.

Reference frequency input

The Si53301 requires slew rate at least 750 V/us to meet 50 fs additive jitter.
This would require 5.5 Vpk-pk @ 10 MHz or 1.45 Vpk-pk at 40 MHz for sine wave.
Therefore, clipped sine wave or rectangle is required for best jitter performance.
The clipped sine should have slew rate at least 400 V/us and voltage at least 150 mVpp,
edges should be shorter than 1 ns.

Direct logic refin.
Only for internal use.
Not protected.
Ground not isolated.

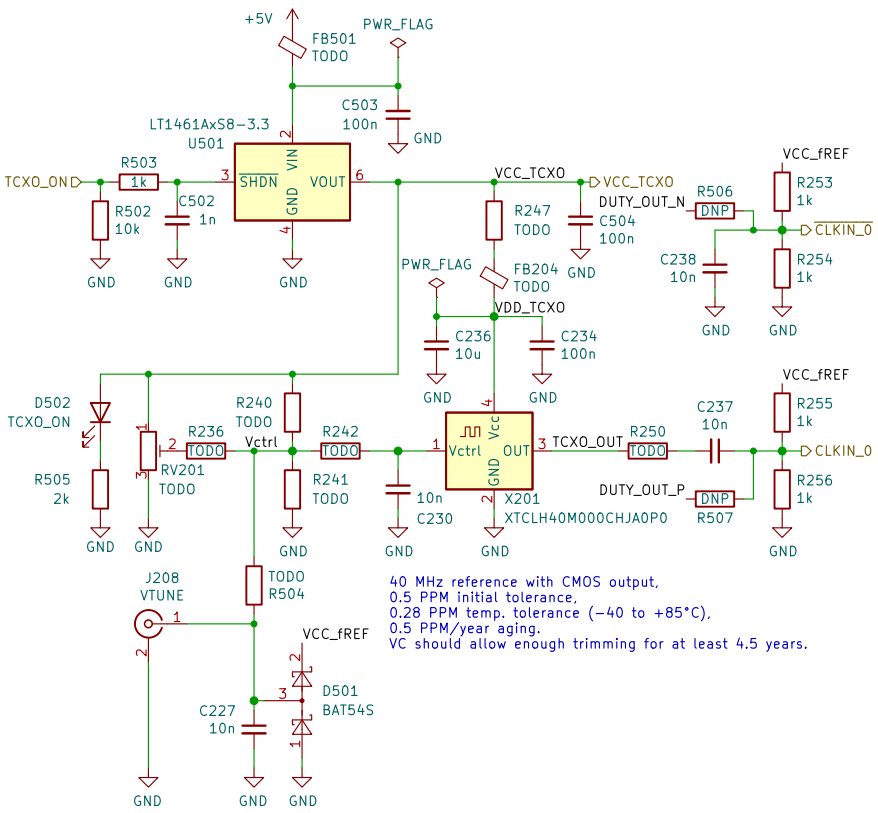
Duty factor correcting circuitry.
Assemble only when needed.



48V overvoltage protection.
The TC2-1T+ doesn't have pri-sec voltage rating!
Before assembling the TVS, check that the
TC2-1T+ can withstand at least 75 V DC.
Check by test, check every unit for one minute (before assembly).

Differential overvoltage protection. Clips large signals
without lowering slew rate. Can be replaced by most
microwave NPN transistors. Do not use diodes as these
tend to be too slow or have high capacitance except for
special types.

VCTCXO



40 MHz reference with CMOS output,
0.5 PPM initial tolerance,
0.28 PPM temp. tolerance (-40 to +85°C),
0.5 PPM/year aging.
VC should allow enough trimming for at least 4.5 years.

Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek

Sheet: /Clock reference/Input Clocks/
File: input_clocks.kicad_sch

Title: Generator 0.0125 - 6.4 GHz (0.02 - 9.8 GHz)

Size: A4	Date: 2021-11-13	**Rev: 211113-001**
KiCad E.D.A.	kicad 6.0.0-rc2-unknown-160328abc7~144~ubuntu21.10.1	Id: 5/5