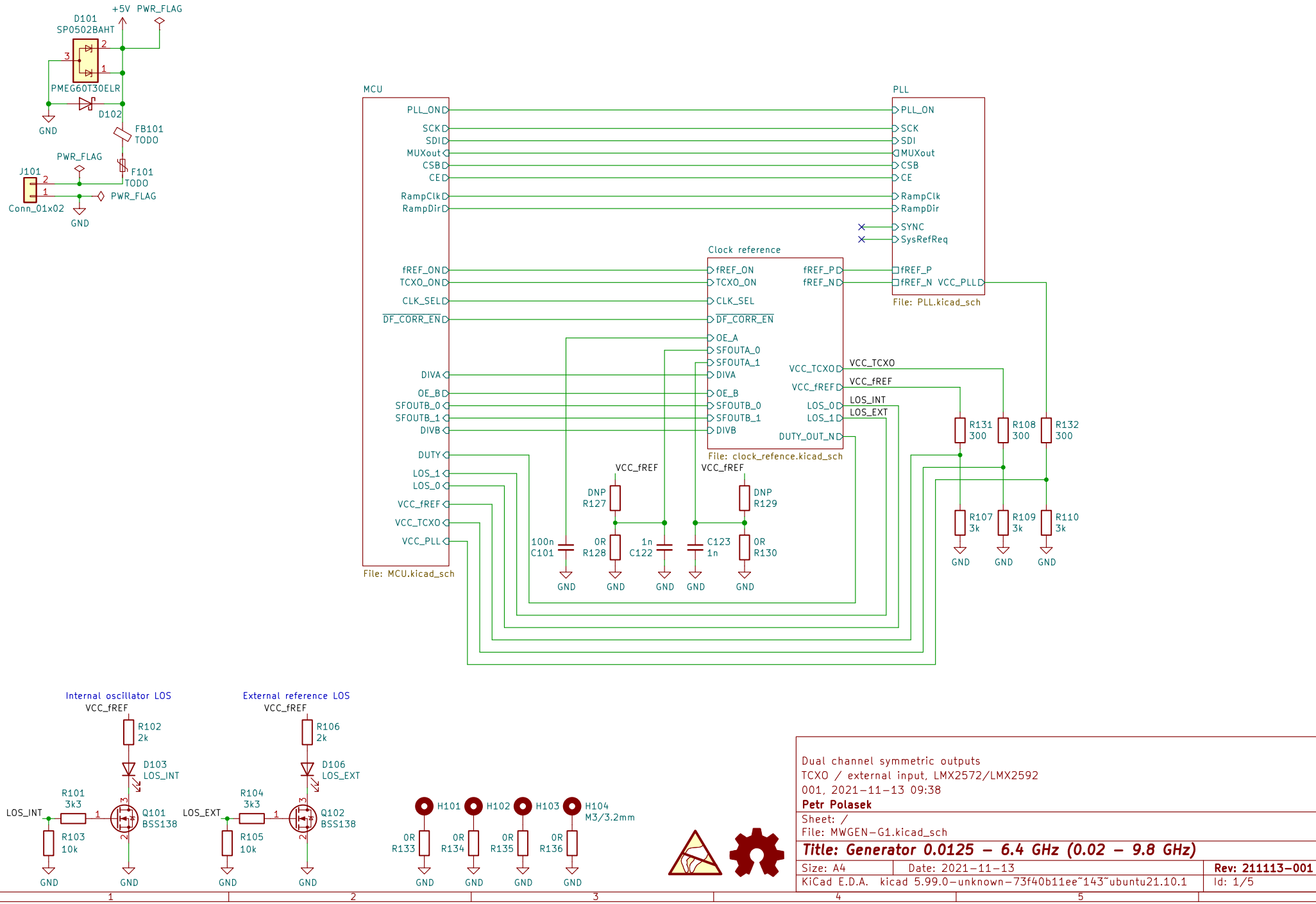
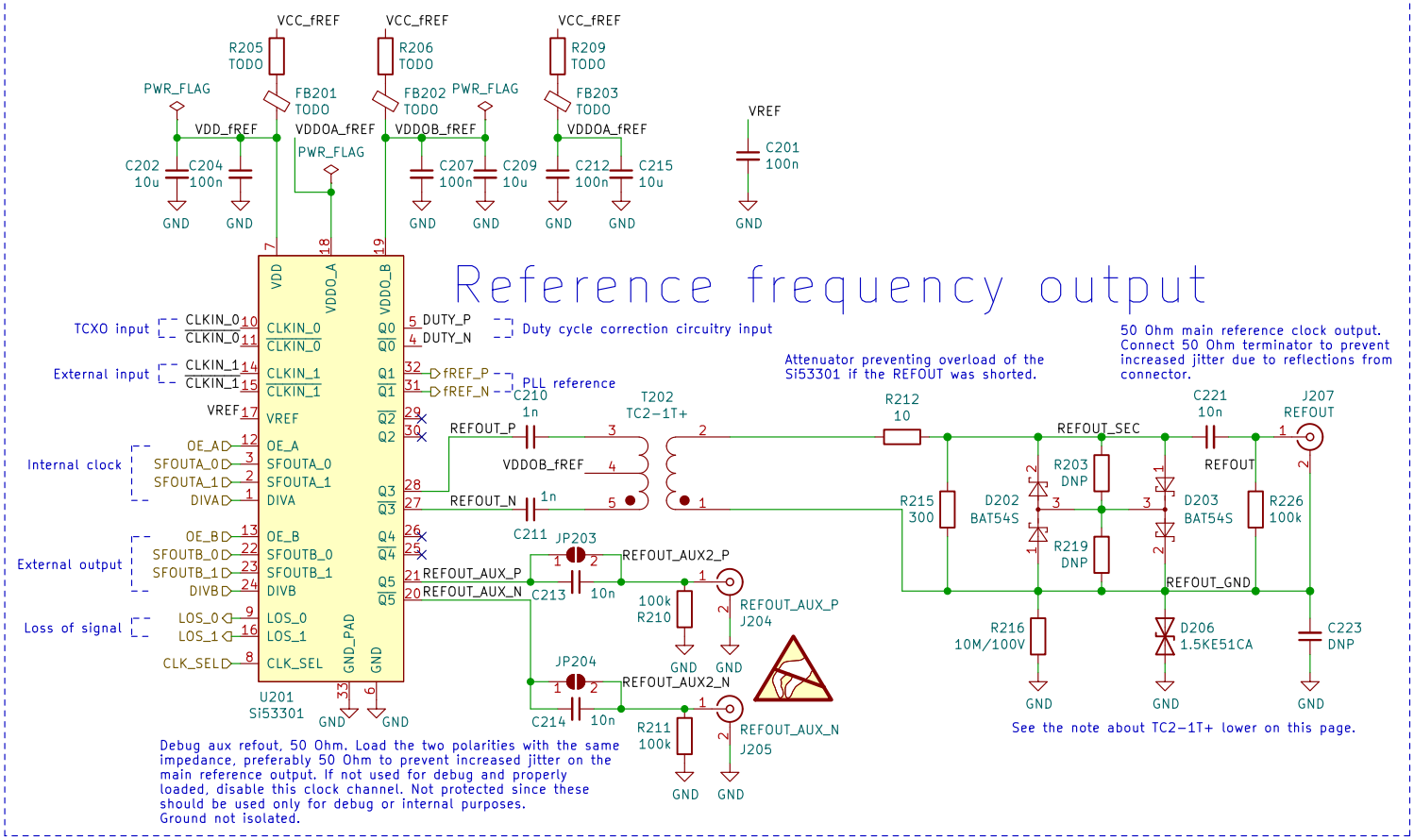
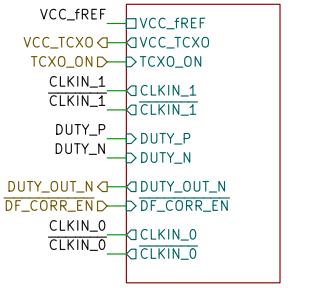

D101
SP0502BAHT
+5V
PWR_FLAG
PMEG60T30ELR
D102
GND
FB101
TODO
PWR_FLAG
J101
F101
TODO
Conn_01x02
PWR_FLAG
GND
MCU
PLL_ON
SCK
SDI
MUXout
CSB
CE
RampClk
RampDir
fREF_ON
TCXO_ON
CLK_SEL
DF_CORR_EN
DIVA
OE_B
SFOUTB_0
SFOUTB_1
DIVB
DUTY
LOS_1
LOS_0
VCC_fREF
VCC_TCXO
VCC_PLL
File: MCU.kicad_sch
PLL
PLL_ON
SCK
SDI
MUXout
CSB
CE
RampClk
RampDir
SYNC
SysRefReq
fREF_P
fREF_N
VCC_PLL
File: PLL.kicad_sch
Clock reference
fREF_ON
TCXO_ON
CLK_SEL
DF_CORR_EN
OE_A
SFOUTA_0
SFOUTA_1
DIVA
OE_B
SFOUTB_0
SFOUTB_1
DIVB
fREF_P
fREF_N
VCC_TCXO
VCC_fREF
LOS_0
LOS_1
DUTY_OUT_N
File: clock_refence.kicad_sch
VCC_TCXO
VCC_fREF
LOS_INT
LOS_EXT
R131 300
R108 300
R132 300
R107 3k
R109 3k
R110 3k
GND
VCC_fREF
DNP R127
VCC_fREF
DNP R129
100n C101
0R R128
1n C122
C123 1n
0R R130
GND
Internal oscillator LOS
VCC_fREF
R102 2k
D103 LOS_INT
R101 3k3
LOS_INT
Q101 BSS138
R103 10k
GND
External reference LOS
VCC_fREF
R106 2k
D106 LOS_EXT
R104 3k3
LOS_EXT
Q102 BSS138
R105 10k
GND
H101
H102
H103
H104 M3/3.2mm
0R R133
0R R134
0R R135
0R R136
GND
Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek
Sheet: /
File: MWGEN-G1.kicad_sch
Title: Generator 0.0125 - 6.4 GHz (0.02 - 9.8 GHz)
Size: A4
Date: 2021-11-13
Rev: 211113-001
KiCad E.D.A. kicad 5.99.0-unknown-73f40b11ee~143~ubuntu21.10.1
Id: 1/5

Multiplexer / buffer



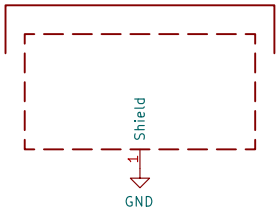
Reference frequency output

Input Clocks

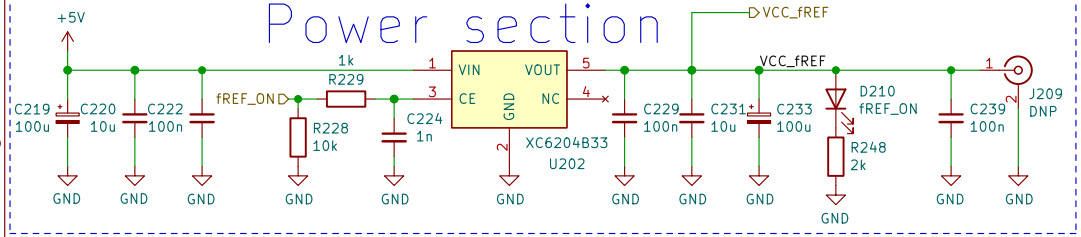


File: input_clocks.kicad_sch

J206 RFShield_TwoPieces



Power section



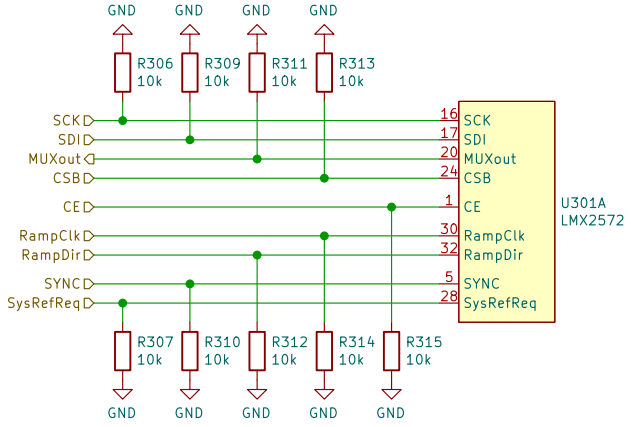
Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek

Sheet: /Clock reference/
File: clock_refence.kicad_sch

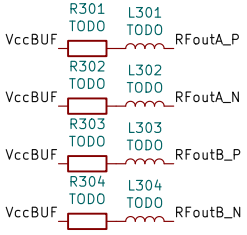
Title: Generator 0.0125 – 6.4 GHz (0.02 – 9.8 GHz)

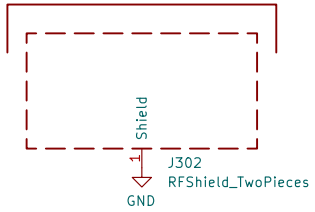
Size: A4	Date: 2021-11-13	**Rev: 211113-001**
KiCad E.D.A. kicad 5.99.0-unknown-73f40b11ee~143~ubuntu21.10.1		Id: 2/5

Communication section

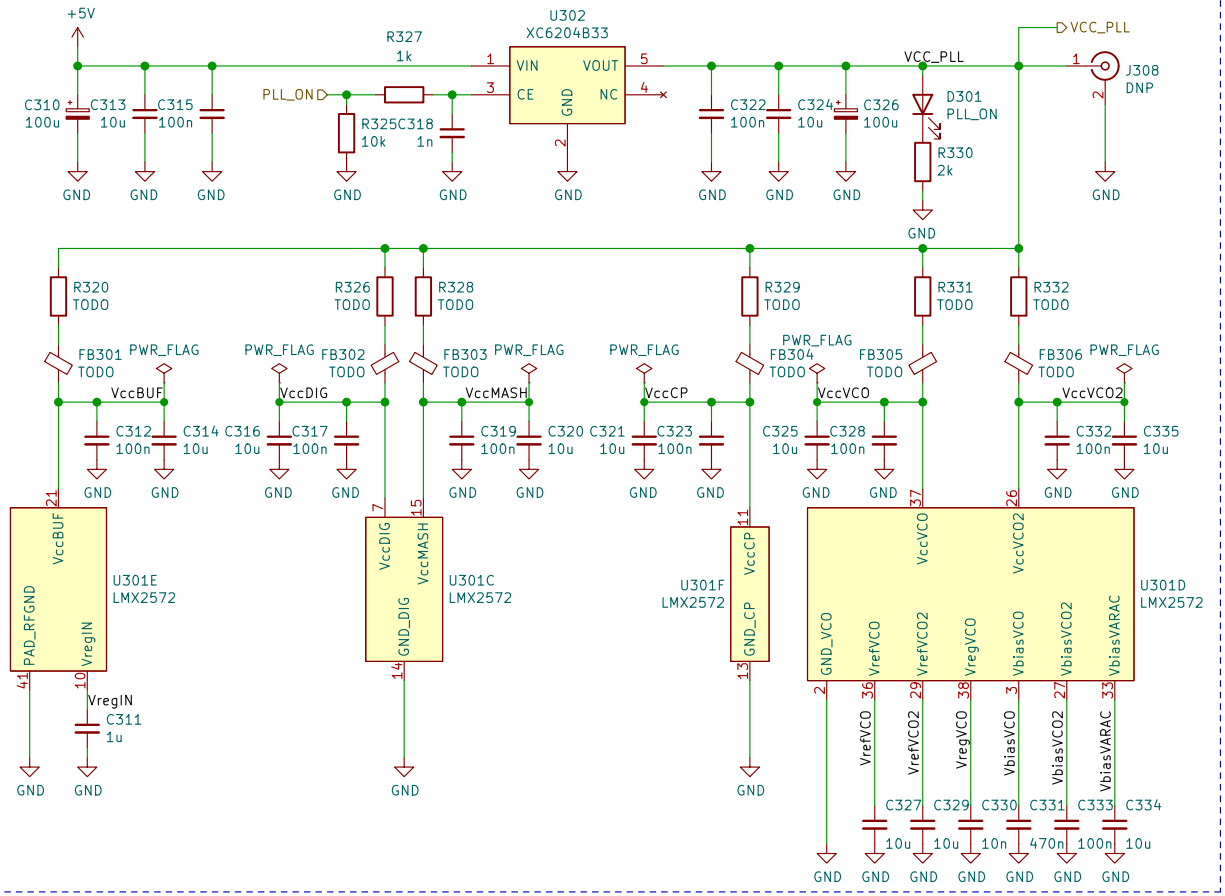


Place these pullups only in case LMX2592 is used.
Do not place them when LMX2572 is used!



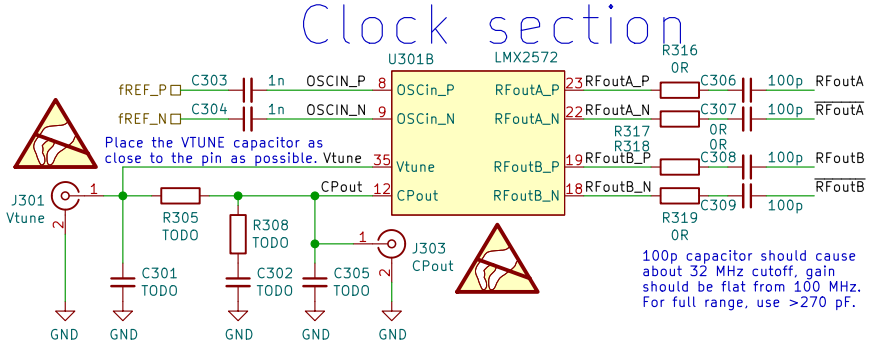


Power section



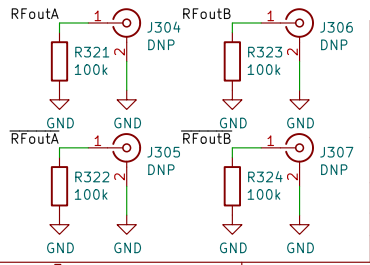
The output impedance of LMX2572 is "... just a few ohms." (citation)
The impedance should be measured and according series resistors should be placed to get 50R output. Place the resistors as close as possible to the PLL.
https://e2e.ti.com/support/clock-and-timing/f/48/t/833789?LMX2572-LMX2572-RF-output-impedance-
For LMX2592, place 0R resistors.

Clock section



100p capacitor should cause about 32 MHz cutoff, gain should be flat from 100 MHz. For full range, use >270 pF.

Be careful as the outputs have no protections and can be sensitive to ESD or devices with DC offset. Before connecting anything, first be sure to discharge any charge present on the core of the connecting cable and on the connected device!

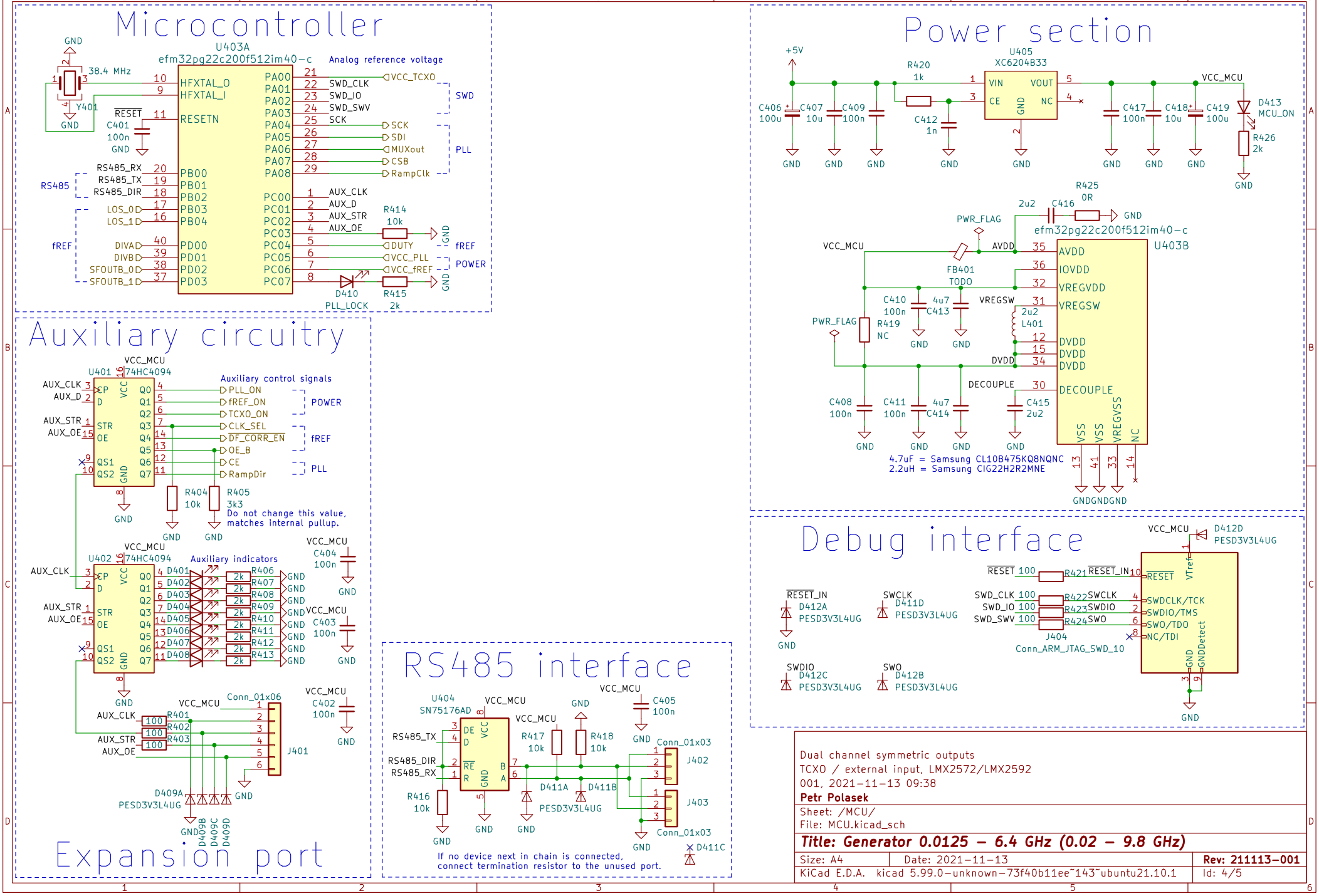


Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek

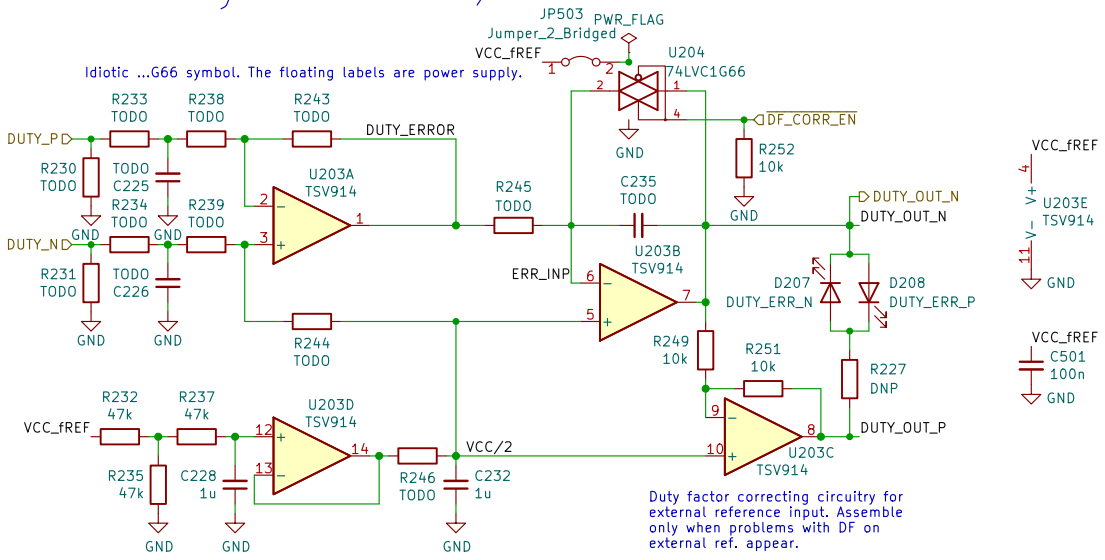
Sheet: /PLL/
File: PLL.kicad_sch

Title: Generator 0.0125 – 6.4 GHz (0.02 – 9.8 GHz)

Size: A4	Date: 2021-11-13	**Rev: 211113-001**
KiCad E.D.A. kicad 5.99.0-unknown-73f40b11ee~143~ubuntu21.10.1		Id: 3/5

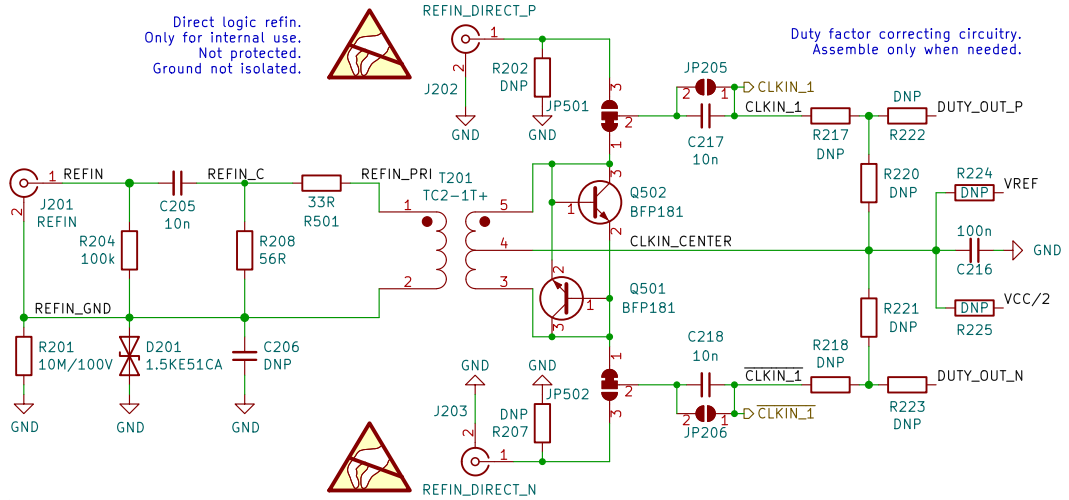

Microcontroller
U403A
efm32pg22c200f512im40-c
Analog reference voltage
38.4 MHz
Y401
RESET
C401
100n
HFXTAL_O
HFXTAL_I
RESETN
PA00
PA01
PA02
PA03
PA04
PA05
PA06
PA07
PA08
PB00
PB01
PB02
PB03
PB04
PC00
PC01
PC02
PC03
PC04
PC05
PC06
PC07
PD00
PD01
PD02
PD03
VCC_TCXO
SWD_CLK
SWD_IO
SWD_SWV
SCK
SDI
MUXout
CSB
RampClk
AUX_CLK
AUX_D
AUX_STR
AUX_OE
DUTY
VCC_PLL
VCC_fREF
SWD
PLL
POWER
fREF
RS485
RS485_RX
RS485_TX
RS485_DIR
LOS_0
LOS_1
DIVA
DIVB
SFOUTB_0
SFOUTB_1
R414
10k
R415
2k
D410
PLL_LOCK
Power section
+5V
U405
XC6204B33
VIN
VOUT
CE
GND
NC
R420
1k
R412
1n
C406
100u
C407
10u
C409
100n
C417
100n
C418
10u
C419
100u
D413
MCU_ON
R426
2k
VCC_MCU
R425
0R
C416
2u2
PWR_FLAG
efm32pg22c200f512im40-c
U403B
AVDD
IOVDD
VREGVDD
VREGSW
DVDD
DECOUPLE
VSS
VREGVSS
NC
FB401
TODO
C410
100n
C413
4u7
L401
2u2
R419
NC
C408
100n
C411
100n
C414
4u7
C415
2u2
4.7uF = Samsung CL10B475KQ8NQNC
2.2uH = Samsung CIG22H2R2MNE
Auxiliary circuitry
U401
74HC4094
U402
74HC4094
Auxiliary control signals
PLL_ON
fREF_ON
TCXO_ON
CLK_SEL
DF_CORR_EN
OE_B
CE
RampDir
Auxiliary indicators
R404
10k
R405
3k3
Do not change this value,
matches internal pullup.
C404
100n
C403
100n
C402
100n
D401
D402
D403
D404
D405
D406
D407
D408
R406
R407
R408
R409
R410
R411
R412
R413
2k
R401
R402
R403
100
Conn_01x06
J401
D409A
PESD3V3L4UG
D409B
D409C
D409D
Expansion port
RS485 interface
U404
SN75176AD
RS485_TX
RS485_DIR
RS485_RX
R416
10k
R417
10k
R418
10k
C405
100n
D411A
D411B
D411C
PESD3V3L4UG
Conn_01x03
J402
J403
If no device next in chain is connected,
connect termination resistor to the unused port.
Debug interface
RESET_IN
SWCLK
SWDIO
SWO
D412A
D411D
D412C
D412B
PESD3V3L4UG
R421
RESET_IN
R422
SWCLK
R423
SWDIO
R424
SWO
SWD_CLK
SWD_IO
SWD_SWV
100
J404
Conn_ARM_JTAG_SWD_10
D412D
PESD3V3L4UG
VTref
RESET
SWDCLK/TCK
SWDIO/TMS
SWO/TDO
NC/TDI
GNDDetect
Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek
Sheet: /MCU/
File: MCU.kicad_sch
Title: Generator 0.0125 – 6.4 GHz (0.02 – 9.8 GHz)
Size: A4
Date: 2021-11-13
Rev: 211113-001
KiCad E.D.A. kicad 5.99.0-unknown-73f40b11ee~143~ubuntu21.10.1
Id: 4/5

Duty factor / DC corrector

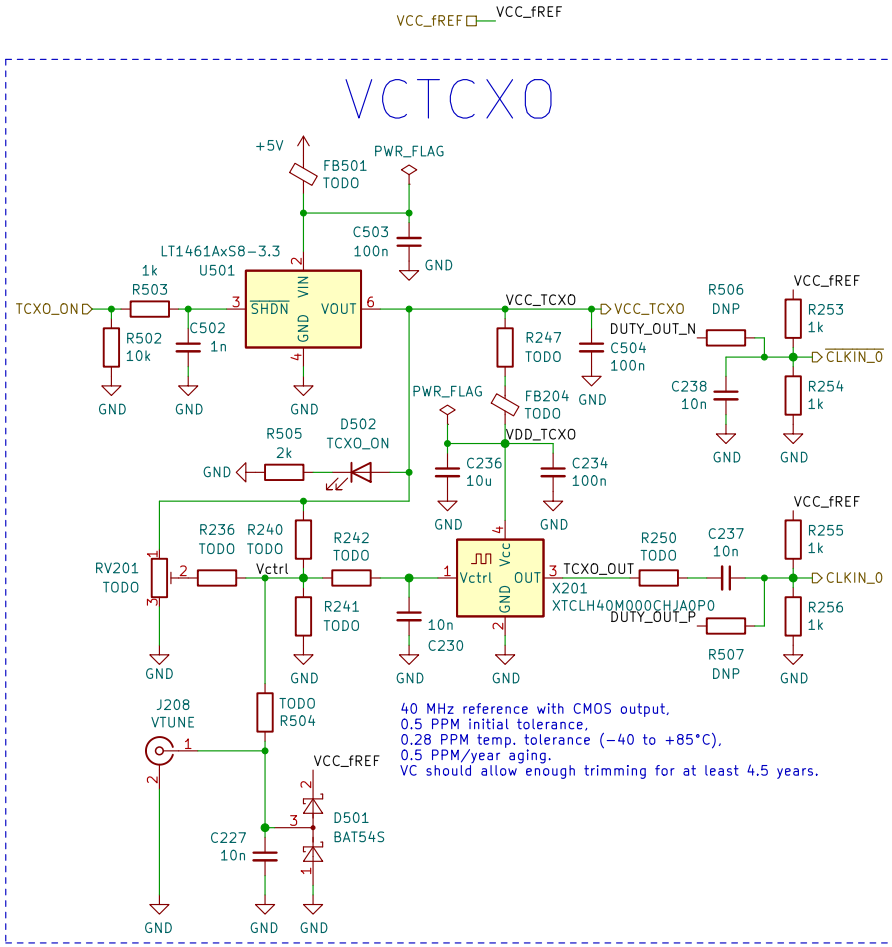


Reference frequency input

The Si53301 requires slew rate at least 750 V/us to meet 50 fs additive jitter.
This would require 5.5 Vpk-pk @ 10 MHz or 1.45 Vpk-pk at 40 MHz for sine wave.
Therefore, clipped sine wave or rectangle is required for best jitter performance.
The clipped sine should have slew rate at least 400 V/us and voltage at least 150 mVpp,
edges should be shorter than 1 ns.



VCTCXO



Dual channel symmetric outputs
TCXO / external input, LMX2572/LMX2592
001, 2021-11-13 09:38
Petr Polasek

Sheet: /Clock reference/Input Clocks/
File: input_clocks.kicad_sch

Title: Generator 0.0125 - 6.4 GHz (0.02 - 9.8 GHz)

Size: A4	Date: 2021-11-13	**Rev: 211113-001**
KiCad E.D.A. kicad 5.99.0-unknown-73f40b11ee~143~ubuntu21.10.1		Id: 5/5