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OPEN SOURCE SUMMIT
NORTH AMERICA

THE LINUX FOUNDATION

Embedded Linux Conference
North America

RISC-V: INSTRUCTION SETS WANT TO BE FREE

Krste Asanovic,
Professor, Computer Science Division,
University of California, Berkeley

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SLIDES

RISC-V®

Instruction Sets Want to be Free!



Krste Asanovic
 Prof. EECS, UC Berkeley;
 Chairman, RISC-V Foundation;
 Co-Founder and Chief Architect,
 SiFive Inc.

July 1, 2020

@risc_v

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promise of opening up the hardware world to the same kind of rapid innovation scene with open source software. Please welcome Krste.
 >> Hi, thank you for the introduction. Really excited to be here with the come of this open source event software events. So it's an instruction sets, and the model is that.

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Q&A WITH SPEAKER SPEAKER BIO



Daniel Qian
Software Engineer
eBay

Shijun (Daniel) Qian works on eBay's cloud team. He has a wide range of interests in many aspects of cloud native computing, mainly focused on cluster lifecycle management, monitoring, and networking. He is also an active open source contributor (github: @danielqsj): 1. Kubernetes Member & Reviewer 2. Top 100 contributors of Kubernetes. 3. Sponsor and maintainer of Prometheus components: kafka-exporter. 4. Speaking in KubeCon CloudNativeCon China 2018



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Why Instruction Set Architecture matters

- Why can't Intel sell mobile chips?
 - 99%+ of mobile phones/tablets based on ARM v7/v8 ISA
- Why can't ARM partners sell servers?
 - 99%+ of laptops/desktops/servers based on AMD64 ISA (over 95%+ built by Intel)
- How can IBM still sell mainframes?
 - IBM 360, oldest surviving ISA (50+ years)

***ISA is most important interface in computer system
where software meets hardware***

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existence. Actually the 360, it also introduced the notion of an architecture, the idea that you should separate the interface to a hardware platform from the actual implementation. The instruction is really the most important interface and a computer system because that's where software meets hardware. The rest of the computing we have open

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Open Interfaces Work for Software!

Field	<i>Open Standard</i>	<i>Free, Open Implement.</i>	<i>Proprietary Implement.</i>
Networking	Ethernet, TCP/IP	Many	Many
OS	Posix	Linux, FreeBSD	M/S Windows
Compilers	C	gcc, LLVM	Intel icc, ARMcc
Databases	SQL	MySQL, PostgreSQL	Oracle 12C, M/S DB2
Graphics	OpenGL	Mesa3D	M/S DirectX
ISA	??????	-----	x86, ARM, IBM360

- Why not successful free & open standards and free & open implementations, like other fields?

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software meets hardware. The rest of the computing we have open interfaces. You look at networking, ethernet, operating systems, languages, databases, open standard interfaces. We haven't had that at the instruction set level. Why is that? Why are we stuck? There is no good reason and that's part of this process, we

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Companies and their ISAs Come and Go

Proprietary ISA fortunes tied to business fortunes and whims

- Digital Equipment Corporation
 - PDP-11, VAX, Alpha
- Intel
 - i960, i860, Itanium
- MIPS
 - Sold to Imagination, bought by Wave, opened then closed R6 ISA
 - Opened up MIPS R6 ISA, then closed it down
- SPARC
 - Was opened up by Sun, then acquired by Oracle, now closed down
- ARM
 - Sold to Softbank at >40% premium
 - Now 25% sold off to Abu Dhabi investment fund

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bit version. There were a lot of companies building implementations around that. Later they were acquired by Oracle, and it was closed. Finally they just close down all of its five developments completely. ARM is a big powerful company, but there were some shock waves when they were sold. Other probably run company. People are worried about what will happen to the future.

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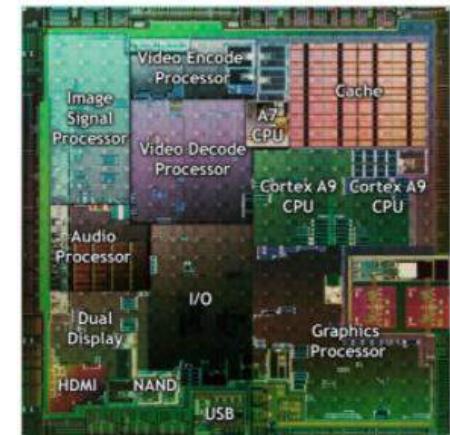


Today, many ISAs on one SoC

- Applications processor (usually ARM)
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- > dozen ISAs on some SoCs – each with unique software stack

Why?

- Apps processor ISA too big, inflexible for accelerators
- IP bought from different places, each proprietary ISA
- Engineers build home-grown ISA cores



NVIDIA Tegra SoC

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able to because of the licensing terms. Once somebody assembles it, each of those vendors is not able to use one of the preparatory, they design their own because they need to. One of the worst things that can happen is when you build it, the engineer of your company may decide they should just

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Do we need all these different ISAs?
Must they be proprietary?
Must they keep disappearing?

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decide they should just go build their own ISA. Which then means they have to support the software for that all the time afterwards. So do we really need all these different instruction sets? Do they have to be proprietary? Do they have to keep disappearing? What if there was one free and stable and open ISA. Why don't we

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RISC-V Background

- In 2010, after many years and many research projects using MIPS, SPARC, and x86, time for architecture group at UC Berkeley to choose ISA for next set of projects
- Obvious choices: x86 and ARM
 - x86 impossible – too complex, IP issues
 - ARM mostly impossible – complex, no 64-bit in 2010, IP issues
- So we started “3-month project” during summer 2010 to develop clean-slate ISA
 - Principal designers: Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanovic
- Four years later, May 2014, released frozen base user spec
 - many tapeouts and several research publications along the way
- Name RISC-V (pronounced “risk-five”) represents fifth major Berkeley RISC ISA



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time and my colleague Dave Patterson. Many people helped us out along the way. After four years we, the project took four years, but we had a frozen spec at that point. So it's called RISC-V, because it's the fifth major highest ISA. Went back to the highest projects from the early 80s, they always regret not keeping the

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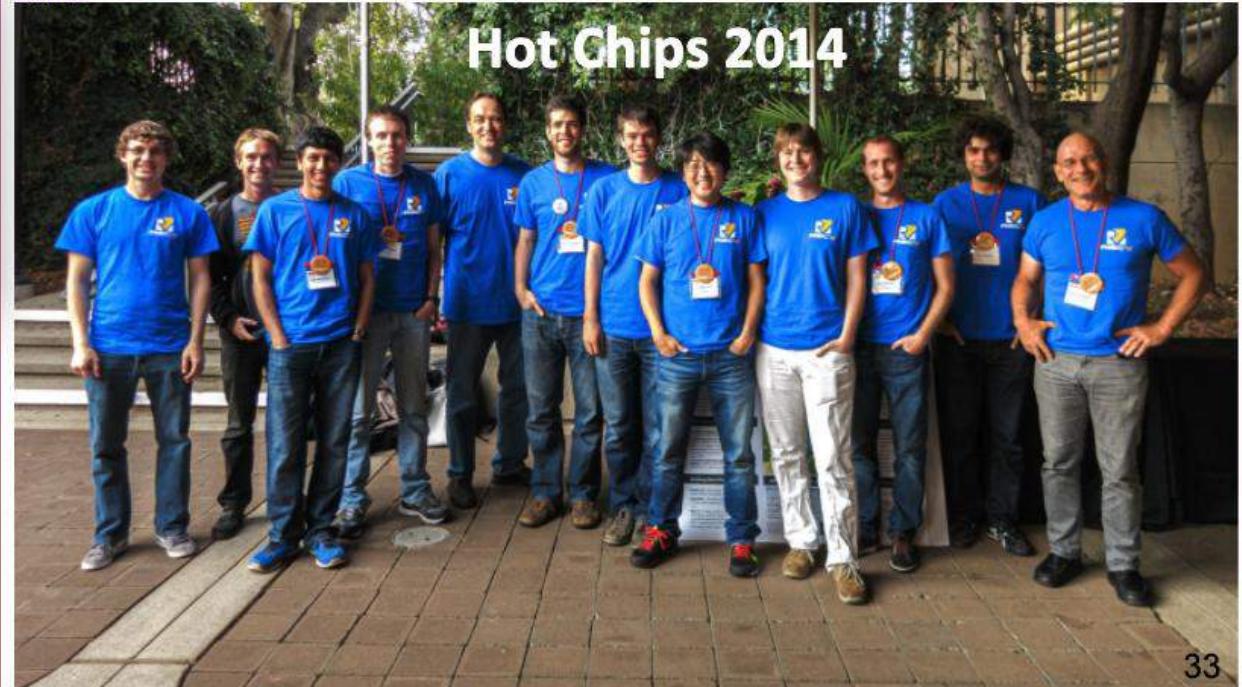
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had a frozen spec at that point. So it's called RISC-V, because it's the fifth major highest ISA. Went back to the highest projects from the early 80s, they always regret not keeping the plan. They renamed the projects RISC-V. Known as RISC-V and not RISC 4. And so we were working on this ISA and we started getting external emails from people asking about an instruction set and



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Welcome to the RISC-V revolution!



RISC-V International is a non-profit entity serving members and the industry

Our mission is to accelerate RISC-V adoption with shared benefit to the entire community of stakeholders.

- ✓ Drive progression of ratified specs, compliance suite, and other technical deliverables
- ✓ Grow the overall ecosystem / membership, promoting diversity while preventing fragmentation
- ✓ Deepen community engagement and visibility

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many people from the industry told us this was something they really needed. There really was a big hole in the market for an open instruction sets. One thing they said was with the University project, we need a more stable home for something if we will build industry around it. In 2015 we created the foundation to be a nonprofit entity to basically manage

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SLIDES**CHINA**

MORE THAN 200 MEMBERS HAVE JOINED THE CRVA AND CRVIC ASSOCIATIONS AS WELL AS 33 MEMBERS IN THE GLOBAL RISC-V FOUNDATION. ACROSS 2019 WE'VE LED DISCUSSIONS IN 6 CITIES AS WELL AS HOSTED A DAY OF TALKS AT THE WORLD INTERNET CONFERENCE. IN NOVEMBER, WE HOSTED 500 ATTENDEES AT THE CHINA RISC-V FORUM.



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around it. In 2015 we created the foundation to be a nonprofit entity to basically manage the standard. Recently we reincorporated to the foundation as a RISC-V international Houston and Switzerland to reinforce the message that it's intended as a global standard. I will give you some examples. In China

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EUROPE

THE EUROPEAN PROCESSOR INITIATIVE HAS DECLARED RISC-V AS A KEY ARCHITECTURE FOR THE NEXT GENERATION OF HPC PROCESSORS AND SYSTEMS, FOCUSED ON ACCELERATION.



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some examples. In China many members, a lot of interest with the open industry academia and using RISC-V. In Europe -- sorry, let me go back. In China and Europe, the process initiative recently announced that they have it as a key architecture that will build high-performance computing

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SLIDES**INDIA**

2014 WITH THE FUNDING OF 6 RISC-V PROCESSORS THROUGH THE SHAKTI PROJECT, RISC-V HAS BEEN WIDELY DECLARED THE NATIONAL ARCHITECTURE OF INDIA.



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some examples. In China many members, a lot of interest with the open industry academia and using RISC-V. In Europe -- sorry, let me go back. In China and Europe, the process initiative recently announced that they have it as a key architecture that will build high-performance computing accelerators. In India, they were actually one of the first countries to seriously adopt RISC-V and they funded a number of

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SLIDES**JAPAN**

MOMENTUM IS CONTINUING TO GROW IN OUR ENGAGEMENT AND EVENTS WITH A 50% JUMP AT OUR 2019 TOKYO DAY TO 360 REGISTERED ATTENDEES.



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computing accelerators. In India, they were actually one of the first countries to seriously adopt RISC-V and they funded a number of projects including the project which is developing six open source processors that can be used by anybody. In Japan we have seen increasing momentum. Many people are showing up to the events and Japan. Here in North America



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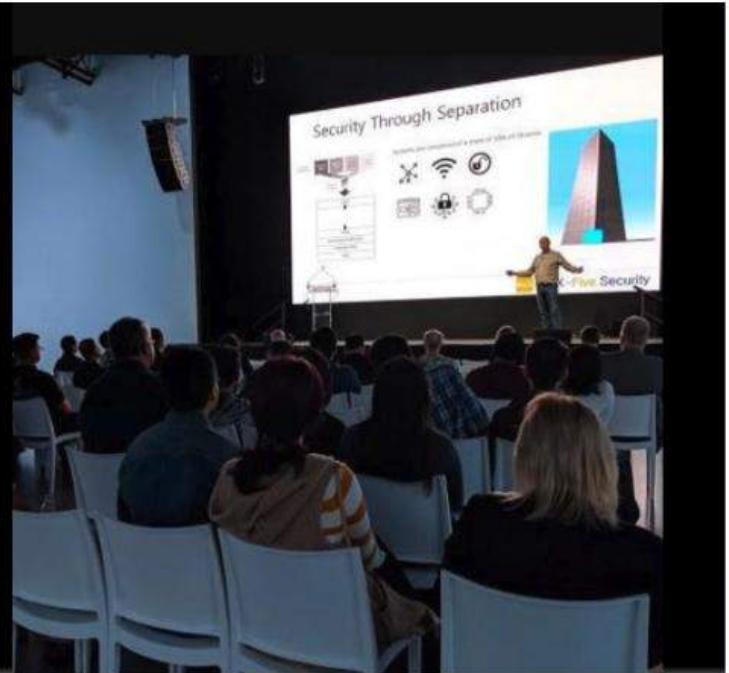
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NORTH AMERICA

NORTH AMERICA. INDUSTRY ADOPTION HAS TAKEN OFF WITH MILLIONS OF CORES SHIPPING FROM NVIDIA, WESTERN DIGITAL, SIFIVE, AND OTHERS.



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PAKISTAN

ON THE ROAD TO DECLARING RISC-V THEIR NATIONAL ARCHITECTURE, TWO OF THE BIGGEST GATHERINGS EVER OF 3000+ IN PAKISTAN FOR TWO SIFIVE TECH SYMPOSIA – OCT 2019



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momentum. Many people are showing up to the events and Japan. Here in North America, we are shipping using RISC-V, for example we are shipping with RISC-V calls in there. They announced they will move their entire product line to RISC-V. Many companies are providing this and assign them inside the U.S. Now one thing that may surprise you is the biggest RISC-V event we have had so far



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This is actually a photograph of the audience. I was giving a talk at the time, over 3,000 people attended to learn about RISC-V. It's really seen as enabling technology to have everybody build up their own computing technology. Now it's not just academia and researchers, and lobbyists, but almost the

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More than 435 RISC-V Members across 33 Countries Around the World



December 2019

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lobbyists, but almost the entire industry is very seriously approaching RISC-V. To scatter the different members we have. I will point out all the major companies and vendors are involved in RISC-V. We have Google, Samsung, you name it, almost every company is interested in RISC-V. And the growth and the membership has just been incredible over the last few years. So how does RISC-V



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RISC-V Ecosystem

Software

Open-source software:
GCC, binutils, glibc, Linux, BSD,
LLVM, QEMU, FreeRTOS,
ZephyrOS, LiteOS, SylixOS, ...

Commercial software:
Lauterbach, Segger, IAR,
Micrium, ExpressLogic, Ashling,
Imperas, AntMicro, ...



[ISA specification](#)

[Golden Model](#)

[Compliance](#)

Hardware

Open-source cores:
Rocket, BOOM, RI5CY,
Ariane, PicoRV32, Piccolo,
SCR1, Swerv, Hummingbird,
...

Commercial core providers:
Alibaba, Andes, Bluespec,
Cloudbear, Codasip, Cortus,
InCore, Nuclei, SiFive,
Syntacore, ...

Inhouse cores:
Nvidia, WDC, Alibaba,
+others

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own in-house, this is what they're doing on the GP. They both their own for their until use. Now on the software side, RISC-V has been adopted upstream as one of the main architectures and many of the open source projects. It's also being supported by a commercial license with vendors.

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**Simple**

- Far smaller than other commercial ISAs

Clean-slate design

- Clear separation between user and privileged ISA
- Avoids architecture or technology-dependent features

Modular ISA designed for extensibility/specialization

- Small standard base ISA, with multiple standard extensions
- Sparse & variable-length instruction encoding for vast opcode space

Stable

- Base and first standard extensions are frozen
- Additions via optional extensions, not new versions

Community designed

- Developed with leading industry/academic experts and software developers

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What's Different about RISC-V?

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today. We wanted to only include the pieces you need to reach those applications. We made it stable. We have no commercial interest to keep upgrading it. We have a lot of motivation to keep it stable and not change them. And part of it is community design. This is a big difference. We rely on

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Engaged engineers are domain experts Drive technical priorities in 20+ focus areas

Opcode Space Mgmt Standing Committee

Software Standing Committee

Base ISA Ratification Task Group

Privileged ISA Spec Task Group

UNIX-Class Platform Spec Task Group

Formal Specification Task Group

Trusted Execution Env Spec Task Group

B Extension (Bit Manipulation) Task Group

J Extension (Dynam. Translated Lang) Task Group

P Extension (Packed-SIMD Inst) Task Group

V Extension (Vector Ops) Task Group

Cryptographic Extension Task Group

Debug Specification Task Group

Fast Interrupts Spec Task Group

Memory Model Spec Task Group

Processor Trace Spec Task Group

Compliance Task Group

+ Security Committee, HPC Special interest group, soft-core SIG, and Safety Task Group

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reach those applications. We made it stable. We have no commercial interest to keep upgrading it. We have a lot of motivation to keep it stable and not change them. And part of it is community design. This is a big difference. We rely on a large range of experts to develop all of the parts including the

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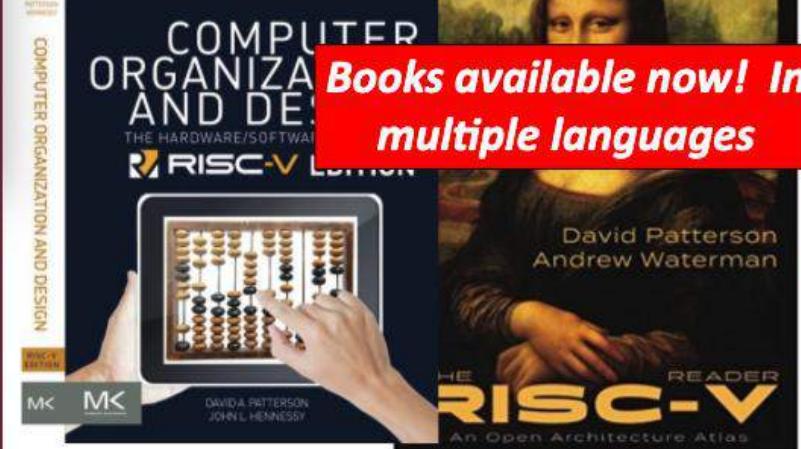
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RISC-V

COMPUTER ORGANIZATION AND DESIGN
RISC-V EDITION

Books available now! In multiple languages

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RISC-V in Education

John L. Hennessy | David A. Patterson

COMPUTER ARCHITECTURE

A Quantitative Approach



RISC-V spreading quickly throughout curricula of top schools

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stable and not change them. And part of it is community design. This is a big difference. We rely on a large range of experts to develop all of the parts including the software community. Here are a few of the different working groups that are working on enhancing the specification. It's also being fractured and education. We are seeing an uptick in schools.



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Why is RISC-V so popular?

- Engineers sometimes “*don't see forest for the trees*”
- The movement is ***not*** happening because some benchmark ran 10% faster, or some implementation was 30% lower power
- The movement ***is*** happening because ***new business model*** changes everything
 - Pick ISA first, then pick vendor or build own core
 - Add your own extension without getting permission
- Implementation features/PPA will follow
 - Whatever is broken/missing in RISC-V will get fixed

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And also because effectively everyone has an architectural license, we designed the ISA to work with extension without getting permission for anybody. It still lets you work on the software. Now you may pick it and say I can't find this level or this feature, but things are moving so fast that whatever is broken or missing and RISC-V will get fixed. We are working hard to fill in the whole ecosystem.

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Modest RISC-V Project Goal

Become the industry-standard ISA for all computing devices

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fast that whatever is broken or missing and RISC-V will get fixed. We are working hard to fill in the whole ecosystem. At this point it has become the industry standard ISA for everything. We are pretty far along and that old. This event, one of the questions I look at at any event is, where are the

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HiFive Unleashed: World's First Multi-Core RISC-V Linux Dev Board (Feb 2018)



- SiFive FU540-C000 (built in 28nm)
- 8 GB 64-bit DDR4 with ECC
- Gigabit Ethernet Port
- 32 MB Quad SPI Flash
- MicroSD card for removable storage
- MicroUSB for debug and serial communication
- Digital GPIO pins
- FMC connector for future expansion with add-in cards

Sold Out!

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Freedom Development Kit Comes with Linux BSP Based on Debian or Fedora

What percent is built for each architecture (past quarter)

percentage of packages

alpha
hppa
ia64
m68k
powerpcspe
ppc64
riscv64
sh4
sparc64
x32

2018.10 2018.12 2018.14 2018.15 2018.16 2018.17 2018.18 2018.19 2018.20 2018.21 2018.22 2018.23 2018.24 2018.25 2018.26 2018.27 2018.28 2018.29 2018.30 2018.31 2018.32 2018.33 2018.34

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HiFive Unleashed with Microsemi PolarFire Expansion Board



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is, where are the dEV boards? In 2018 we released the sci-fi, the first Dev Ron and unfortunately it sold out. We saw the impact it had on the community. For example, it shows you how fast it can work with RISC-V. And the other part about the board, because it was so limited, these are very expensive boards to

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Soon: Microchip PolarFire SoC Icicle Kit

- Low-cost RISC-V Linux dev board
- Hardened SiFive U54-MC plus PolarFire FPGA fabric on one chip
- Sign up for announcements on [crowdsupply.com](#)



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chip there building is including the sci-fi among a piece of silicon. This enables us to make a lower cost board that will have a lot of peripherals. The good thing is that a board is actually coming out, you will be able to sign up right now. At the end of July you'll be able to sign up and it should be shipped by the end



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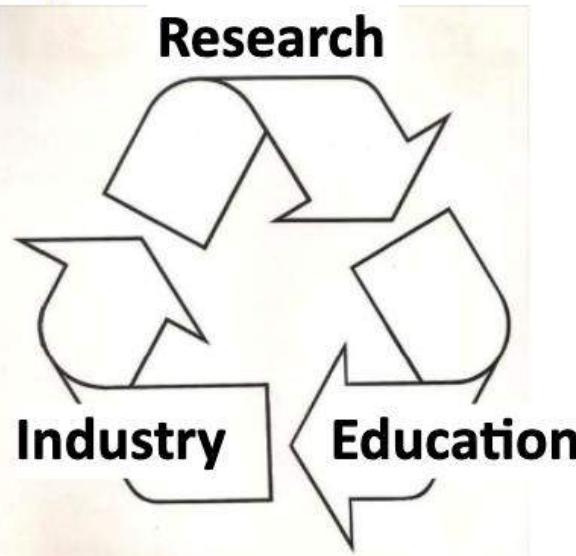
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RISC-V: Completing the Innovation Cycle



Open ecosystem is key to keeping the virtuous cycle going

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conclude here, RISC-V is all about maintaining an open ecosystem and really the important thing here is completing this innovation cycle. By having an open standard we can use an education, students can take that knowledge and apply to real industrial cause, and then if there's problems we can meet those problems directly to research. And this is the key, keeping this innovation cycle going.

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