DSD Final Project Scores(RISC V)

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1. Baseline

(1) Area: (um^2)

- Area: **277399.2874** um^2

```
Total cell area:                277399.287400
Total area:                    2932372.933366
```

(2) Total Simulation Time of given hasHazard testbench：(ns)

- Time = **5809.05 ns**

```
--------------------------- Simulation FINISH !!---------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 5809050 PS + 0
```

(3) Area*Total Simulation Time: (um^2 * ns)

- 5809.05 * 277399.2874 = **1611426330** um^2 * ns

(4)Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench) :(ns)

- 2.7ns

2. BrPred

(1) Total execution cycles of given I_mem_BrPred：(TB_CYCLE = 10ns)

- 2-bit saturating counter：239.5 cycles

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 2395 NS + 0
```

- 2-level adaptive predictor：239.5 cycles

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 2395 NS + 0
```

(2) Total execution cycles of given I_mem_hasHazard：(TB_CYCLE = 10ns)

- **2-bit saturating counter：<u>1861.5 cycles</u>**

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 18615 NS + 0
```

- **2-level adaptive predictor：<u>1735.5ns</u>**

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 17355 NS + 0
```

(3)Synthesis area of BPU(Total area of BrPred minus baseline design, two design clock cycle need to be same)：(syn_CYCLE = 5ns)

- **2-bit saturating counter：260730 - 243554 = <u>17176</u> (um^2)**
- **2-level adaptive predictor：261932 - 243554 = <u>18378</u> (um^2)**

3.Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same) same)：(um^2)

- Baseline + 2way Area

```
Total cell area:                254727.117565
Total area:                    2801293.453441
1
```

- Half word + 2way Area(Compressed design)

```
Total cell area:                270292.274376
Total area:                    3029192.968254
1
```

- Area difference

  15565.156810999993 (um^2)

(2) Total Simulation Time of given I_mem_compression : (ns)

- Simulation Time

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Total Cycle:        410
Hit Cycle:          x
Simulation complete via $finish(1) at time 2097500 PS + 0
```

- Total Simulation Time of 0x0000DEAD * 0x0000F625 = 0xD61A6D01
  2097.500 (ns)

(3) Area*Total Simulation Time: (um^2 * ns)

32647916.411072485 (um^2 * ns)

(4) Clock cycle for post syn simulation (cycle in sdc, not cycle in testbench): (ns)

5 (ns)