1. Description

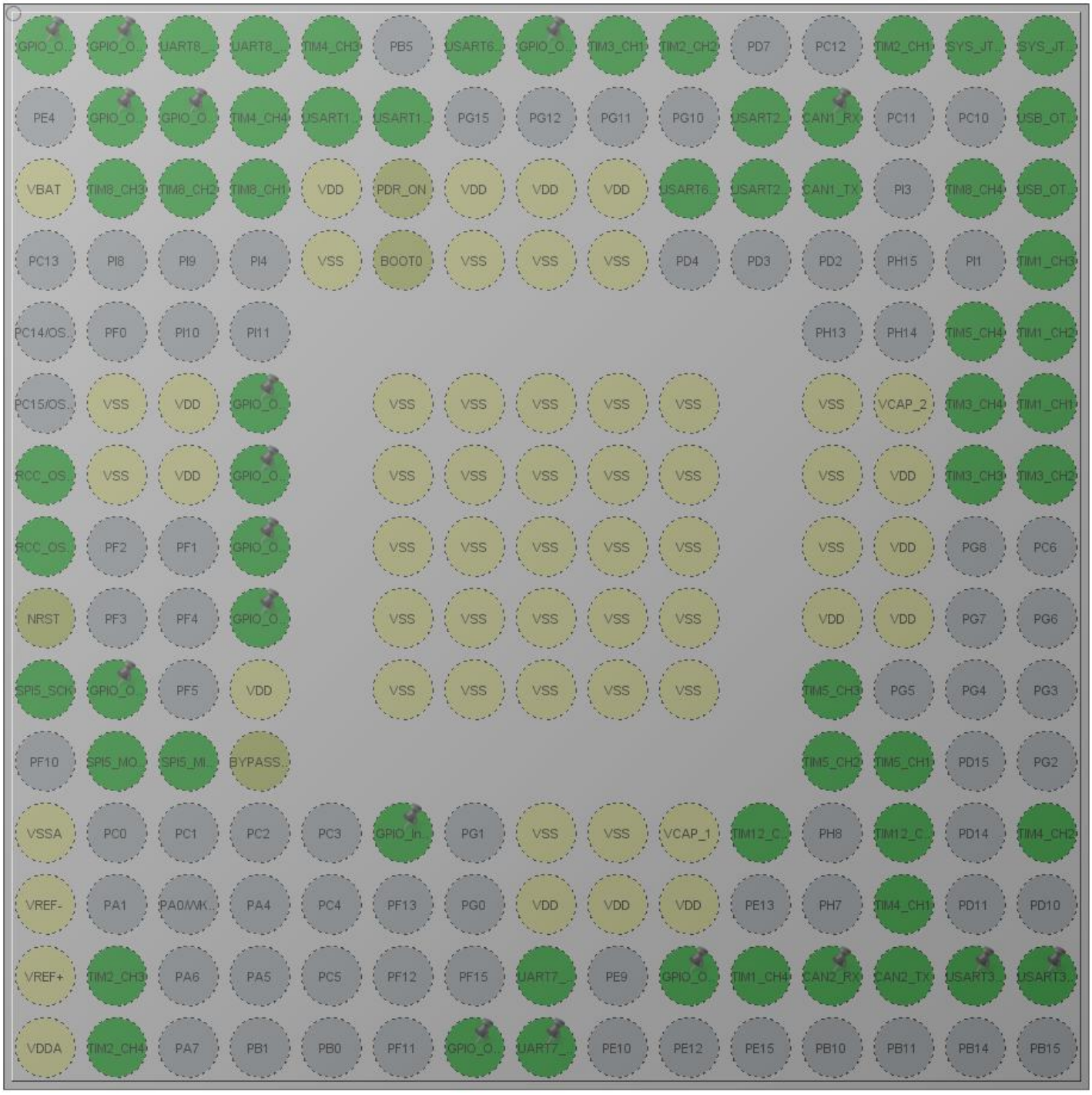
1.1. Project

Project Name	muc_template
Board Name	custom
Generated with:	STM32CubeMX 5.1.0
Date	06/12/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F427/437
MCU name	STM32F427IIHx
MCU Package	UFBGA176
MCU Pin number	201

2. Pinout Configuration



UFBGA176 +25 (Top view)

3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE3 *	I/O	GPIO_Output	
A2	PE2 *	I/O	GPIO_Output	
A3	PE1	I/O	UART8_TX	
A4	PE0	I/O	UART8_RX	
A5	PB8	I/O	TIM4_CH3	
A7	PG14	I/O	USART6_TX	
A8	PG13 *	I/O	GPIO_Output	
A9	PB4	I/O	TIM3_CH1	
A10	PB3	I/O	TIM2_CH2	
A13	PA15	I/O	TIM2_CH1	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B2	PE5 *	I/O	GPIO_Output	
B3	PE6 *	I/O	GPIO_Output	
B4	PB9	I/O	TIM4_CH4	
B5	PB7	I/O	USART1_RX	
B6	PB6	I/O	USART1_TX	
B11	PD6	I/O	USART2_RX	
B12	PD0	I/O	CAN1_RX	
B15	PA12	I/O	USB_OTG_FS_DP	
C1	VBAT	Power		
C2	PI7	I/O	TIM8_CH3	
C3	PI6	I/O	TIM8_CH2	
C4	PI5	I/O	TIM8_CH1	
C5	VDD	Power		
C6	PDR_ON	Reset		
C7	VDD	Power		
C8	VDD	Power		
C9	VDD	Power		
C10	PG9	I/O	USART6_RX	
C11	PD5	I/O	USART2_TX	
C12	PD1	I/O	CAN1_TX	
C14	PI2	I/O	TIM8_CH4	
C15	PA11	I/O	USB_OTG_FS_DM	
D5	VSS	Power		
D6	BOOT0	Boot		

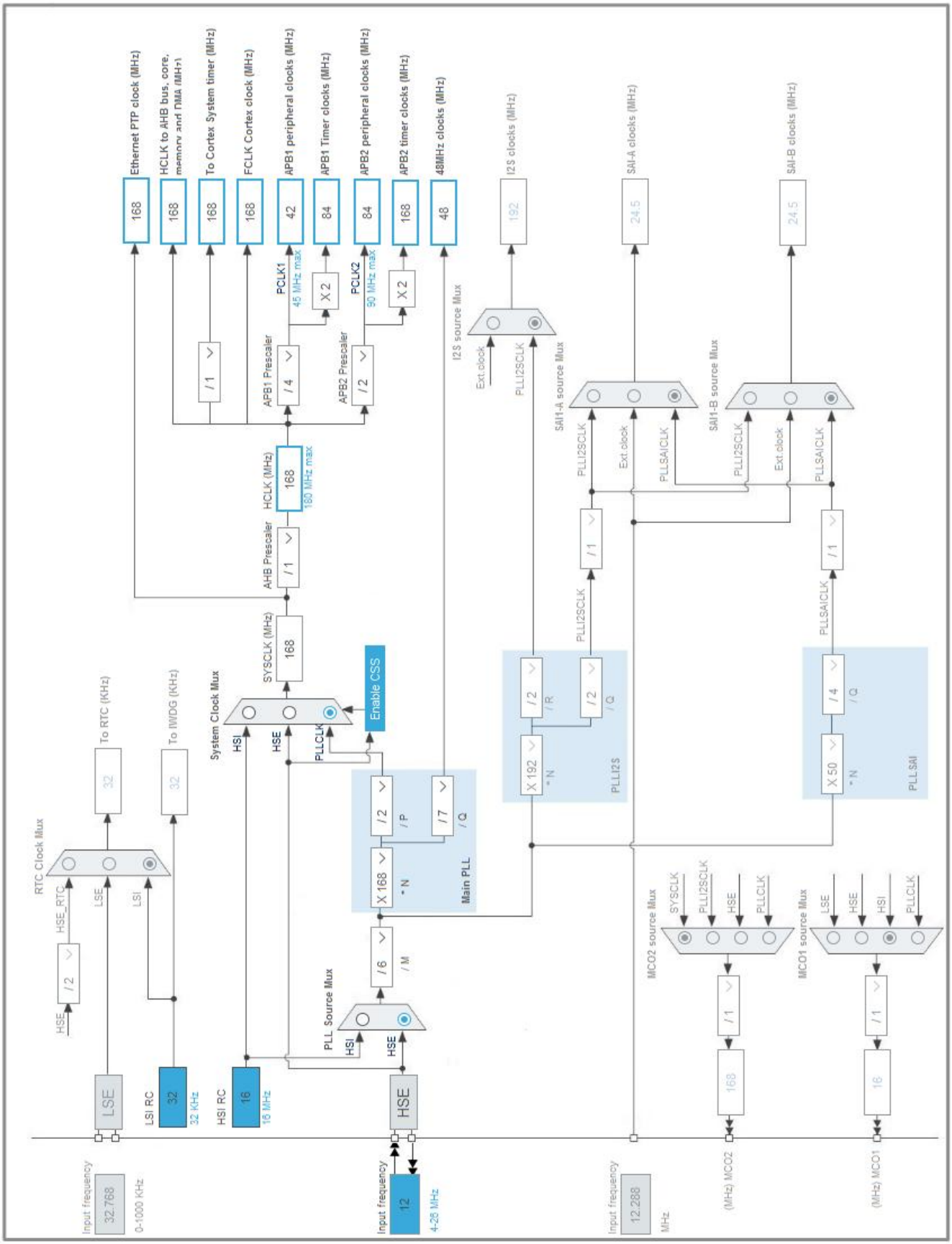
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D7	VSS	Power		
D8	VSS	Power		
D9	VSS	Power		
D15	PA10	I/O	TIM1_CH3	
E14	PI0	I/O	TIM5_CH4	
E15	PA9	I/O	TIM1_CH2	
F2	VSS	Power		
F3	VDD	Power		
F4	PH2 *	I/O	GPIO_Output	
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VCAP_2	Power		
F14	PC9	I/O	TIM3_CH4	
F15	PA8	I/O	TIM1_CH1	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	VSS	Power		
G3	VDD	Power		
G4	PH3 *	I/O	GPIO_Output	
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	VSS	Power		
G13	VDD	Power		
G14	PC8	I/O	TIM3_CH3	
G15	PC7	I/O	TIM3_CH2	
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H4	PH4 *	I/O	GPIO_Output	
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H13	VDD	Power		
J1	NRST	Reset		
J4	PH5 *	I/O	GPIO_Output	
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J12	VDD	Power		
J13	VDD	Power		
K1	PF7	I/O	SPI5_SCK	
K2	PF6 *	I/O	GPIO_Output	
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K12	PH12	I/O	TIM5_CH3	
L2	PF9	I/O	SPI5_MOSI	
L3	PF8	I/O	SPI5_MISO	
L4	BYPASS_REG	Reset		
L12	PH11	I/O	TIM5_CH2	
L13	PH10	I/O	TIM5_CH1	
M1	VSSA	Power		
M6	PB2/BOOT1 *	I/O	GPIO_Input	
M8	VSS	Power		
M9	VSS	Power		
M10	VCAP_1	Power		
M11	PH6	I/O	TIM12_CH1	
M13	PH9	I/O	TIM12_CH2	
M15	PD13	I/O	TIM4_CH2	
N1	VREF-	Power		
N8	VDD	Power		
N9	VDD	Power		
N10	VDD	Power		
N13	PD12	I/O	TIM4_CH1	
P1	VREF+	Power		
P2	PA2	I/O	TIM2_CH3	

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P8	PE8	I/O	UART7_TX	
P10	PE11 *	I/O	GPIO_Output	
P11	PE14	I/O	TIM1_CH4	
P12	PB12	I/O	CAN2_RX	
P13	PB13	I/O	CAN2_TX	
P14	PD9	I/O	USART3_RX	
P15	PD8	I/O	USART3_TX	
R1	VDDA	Power		
R2	PA3	I/O	TIM2_CH4	
R7	PF14 *	I/O	GPIO_Output	
R8	PE7	I/O	UART7_RX	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	muc_template
Project Folder	C:\Users\tyx\Desktop\\
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.23.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F427/437
MCU	STM32F427IIHx
Datasheet	024030_Rev9

6.2. Parameter Selection

Temperature	25
Vdd	null

7. IPs and Middleware Configuration

7.1. CAN1

mode: Mode

7.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.2. CAN2

mode: Mode

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable

Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

7.4. SPI5

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**128 ***
Baud Rate	**656.25 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**168-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2500-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.7. TIM2

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**168-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**2500-1 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0

Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.8. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.9. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.10. TIM5

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0

Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.11. TIM6

mode: Activated

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.12. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.13. TIM12

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2500-1 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.14. TIM14

mode: Activated

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**168-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**5000 ***
Internal Clock Division (CKD)	No Division

7.15. UART7

Mode: Multiprocessor Communication

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.16. UART8

Mode: Multiprocessor Communication

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.17. USART1

Mode: Multiprocessor Communication

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	8 Bits (including Parity)
Parity	**Even ***
Stop Bits	1

Advanced Parameters:

Data Direction	**Receive Only ***
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.18. USART2

Mode: Multiprocessor Communication

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.19. USART3

Mode: Multiprocessor Communication

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.20. USART6

Mode: Multiprocessor Communication

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.21. USB_OTG_FS

Mode: Device_Only

7.21.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
CAN2	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
TIM1	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PI0	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH12	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH11	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PI7	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI6	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI5	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI2	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM12	PH6	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH9	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART8	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART2	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART6	PG14	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG9	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USB_OTG_	PA12	USB_OTG_FS_	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FS		DP			*	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2/BOOT1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream4	Memory To Peripheral	Low
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal

Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream4 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
CAN1 RX0 interrupts	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
DMA2 stream1 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
CAN2 RX1 interrupt	true	0	0
USART6 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 TX interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
CAN2 TX interrupts	unused		
CAN2 RX0 interrupts	unused		
CAN2 SCE interrupt	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		
UART8 global interrupt	unused		
SPI5 global interrupt	unused		

*** User modified value**

9. Software Pack Report