

How many natural states will there be in a 5-bit ripple counter?

A) 4

B) 8

C) 16

D) 32

ANSWER: D

Adding 1001 and 0010 gives an output of _____

A) 0010

B) 1011

C) 1111

D) 1010

ANSWER: B

What is one disadvantage of an S-R flip-flop?

A) It has no enable input.

B) It has an invalid state.

C) It has no clock input.

D) It has only a single output.

ANSWER: B

If A=4'b1010 and B=4'b1100 then A&B

A) 4'b0000

B) 4'b1000

C) 4'b1010

D) 4'b0101

ANSWER: B

On a J-K flip-flop, when is the flip-flop in a hold condition

A) J = 0, K = 0

B) J = 1, K = 0

C) J = 0, K = 1

D) J = 1, K = 1

ANSWER: A

If A=1'b1,B=2'b01,C=2'b00 then y= {A,B[0],C[1]} equals

A) 3'b110

B) 3'b100

C) 3'b101

D) 1'b0

ANSWER: B

In Verilog `h2345 is a

A) 16 bit hexadecimal number

B) 4 bit hexadecimal number

C) 32 bit hexadecimal number

D) 8 bit hexadecimal number

ANSWER: C

Two J-K flip-flops with their J-K inputs tied HIGH are cascaded to be used as counters. After four input clock pulses, the binary count is _____.

A) 00

B) 11

C) 10

D) 01

ANSWER: A

Which logic level is not supported by verilog?

A) U

B) X

C) Z

D) None of these

ANSWER: A

Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?

- A) cross coupling
- B) gate impedance
- C) low input voltages
- D) asynchronous operation

ANSWER: A

If a net has no driver, it gets the value

- A) 0
- B) X
- C) Z
- D) U

ANSWER: C

If both inputs of an S-R flip-flop are low, what will happen when the clock goes HIGH?

- A) An invalid state will exist.
- B) No change will occur in the output
- C) The output will toggle.
- D) The output will reset.

ANSWER: B

How many states does a 3 bit up counter count?

- A) 5
- B) 3
- C) 8
- D) 7

ANSWER: C

Default value of reg is

- A) 0
- B) X

C) Z

D) U

ANSWER: B

The output of the sequential circuit depends upon _____

A) Present input

B) Past input

C) Present input and present state

D) None of the above

ANSWER: C

The task \$stop is provided to

A) End simulation

B) Suspend simulation

C) Exit simulator

D) None of these

ANSWER: B

Externally, an output port must always connect to a

A) net only

B) a reg only

C) either net or reg

D) None of these

ANSWER: A

When both set and reset are disabled in S-R flip flop then the output will be _____

A) Set

B) Reset

C) No Change

D) Indeterminate

ANSWER: C

If A= 4`b011 and B= 4b`0011, then the result of A**B will be

- A) 6
- B) 9
- C) 27
- D) Invalid expression

ANSWER: C

When both set and reset are enabled in S-R flip flop then the output will be _____

- A) Set
- B) Reset
- C) No Change
- D) Indeterminate

ANSWER: D

In which flip flop the present input will be the next output?

- A) SR
- B) JK
- C) D
- D) T

ANSWER: C

If A= 4b`001x and B= 4b`1011, then result of A+B will be

- A) 110x
- B) 1100
- C) xxxx
- D) None of these

ANSWER: C

The terminal count of a typical modulus-9 binary counter is

- A) 0000
- B) 1000

C) 1001

D) 1111

ANSWER: B

IC 7483 is a _____

A) 1 bit adder

B) 2 bit adder

C) 3 bit adder

D) 4 bit adder

ANSWER: D

The set-reset flip flops constructed by cross-coupling of _____ gates

A) AND, NAND

B) NAND, NOR

C) XNOR,NOR

D) None of the above

ANSWER: B

If A= 4`1xxz and B= 4`b1xxx, then A==B will return

A) 1

B) X

C) Z

D) 0

ANSWER: D

How many bits of information do flip-flop store?

A) 1

B) 2

C) 3

D) 4

ANSWER: A

Initial value of a=1 and b=2, then what will be final value if always @ (posedge clock)a=b;always @ (posedge clock)b=a;

- A) a= 2, b=1
- B) a= 1, b=2
- C) Both a and b will have same value either 0 or 1
- D) None of these

ANSWER: C

Whose operations are more faster among the following?

- A) Combinational circuits
- B) Sequential circuits
- C) Latches
- D) Flip flops

ANSWER: A

Initial value of a=1 and b=2, then what will be final value if always @ (posedge clock)a<=b;always @ (posedge clock)b<=a;

- A) a= 2, b=1
- B) a= 1, b=2
- C) Both a and b will have same value either 0 or 1
- D) None of these

ANSWER: A

A mod -10 counter must have _____ flip flops

- A) 10
- B) 4
- C) 2
- D) 3

ANSWER: B

Given the following Verilog code, what value of "a" is displayed?
always @ (clock) begin
a = 0;
a <= 1;
\$display(a);
end

- A) 0

B) 1

C) either 0 or 1 depending on simulator implementation

D) None of these

ANSWER: B

What is the maximum possible range of bit-count specifically in n-bit counter consisting of 'n' number of flip flops?

A) 0 to $2^{\text{exp}[No]}$

B) 0 to $2^{\text{exp}[No]} + 1$

C) 0 to $2^{\text{exp}[No]} - 1$

D) 0 to $2^{\text{exp}((n+1)/2)}$

ANSWER: C

In a pure combinational circuit is it necessary to mention all the inputs in sensitivity list?

A) No

B) Yes

C) It depends on the coding style

D) None of these

ANSWER: B

On the fifth clock pulse, a 4-bit Johnson sequence is $Q_0 = 0$, $Q_1 = 1$, $Q_2 = 1$, and $Q_3 = 1$. On the sixth clock pulse, the sequence is _____.

A) $Q_0 = 1$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$

B) $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 1$, $Q_3 = 0$

C) $Q_0 = 0$, $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 1$

D) $Q_0 = 0$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 1$

ANSWER: C

How many flops will be synthesized by the given code?
always @ (posedge clock)

```
begin Q1<=d; Q2<=q1; Q3<=q2; end
```

A) 1

B) 2

C) 3

D) 4

ANSWER: C

The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

A) 0000

B) 0010

C) 1000

D) 1111

ANSWER: C

Which operators has highest precedence in verilog

A) Unary

B) Multiplication

C) Addition

D) Conditional

ANSWER: A

To operate correctly, starting a ring shift counter requires _____

A) clearing all the flip-flops

B) presetting one flip-flop and clearing all others

C) clearing one flip-flop and presetting all others

D) presetting all the flip-flops

ANSWER: B

In the given code snippet, statement 2 will executed at initial begin#5 x= 1'b0; // statement 1# 15 y= 1b'1; //statement 2End

A) 15

B) 20

C) 5

D) Current simulation time

ANSWER: B

Variable and signal which will be updated first?

- A) Variable
- B) Signal
- C) Can't say
- D) Both Variable & Signal

ANSWER: B

How many flip-flops are required to make a MOD-32 binary counter?

- A) 3
- B) 45
- C) 5
- D) 6

ANSWER: C

Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

- A) Data Selector
- B) Data distributor
- C) Both data selector and data distributor
- D) DeMultiplexer

ANSWER: A

A D flip Flop can be made from a JK Flip Flop by making_____

- A) J=K=1
- B) J=K
- C) J=0; K=1
- D) J=K'

ANSWER: D

In an Down-counter, each flip-flop is triggered by

- A) The output of the next flip-flop
- B) The normal output of the preceding flip-flop

- C) The clock pulse of the previous flip-flop
- D) The inverted output of the preceding flip-flop

ANSWER: D

Which is the major functioning responsibility of the multiplexing combinational circuit?

- A) Decoding the binary information
- B) Generation of all minterms in an output function with OR-gate
- C) Generation of selected path between multiple sources and a single destination
- D) Encoding of binary information

ANSWER: C

If the number of selected input lines is equal to 2^m then it requires _____ select lines.

- A) 2
- B) m
- C) n
- D) $2n$

ANSWER: B

In 5-bit up-down counter, how many flip-flops are required?

- A) 2
- B) 3
- C) 4
- D) 5

ANSWER: D

How is a J-K flip-flop made to toggle?

- A) $J = 0, K = 0$
- B) $J = 1, K = 0$
- C) $J = 0, K = 1$
- D) $J = 1, K = 1$

ANSWER: D

A 4-bit binary up counter has an input clock frequency of 40 kHz. The frequency of the most significant bit is

- A) 1.25 kHz
- B) 2.50 kHz
- C) 160 kHz
- D) 320 kHz

ANSWER: B

With regard to a D latch, _____.

- A) the Q output follows the D input when EN is LOW
- B) the Q output is opposite the D input when EN is LOW
- C) the Q output follows the D input when EN is HIGH
- D) the Q output is HIGH regardless of EN's input state

ANSWER: C

A J-K flip-flop is in a "no change" condition when _____.

- A) J = 1, K = 1
- B) J = 1, K = 0
- C) J = 0, K = 1
- D) J = 0, K = 0

ANSWER: D

PLDs with programmable AND and fixed OR arrays are called

- A) PAL
- B) PLA
- C) APL
- D) PPL

ANSWER: A

What is the major difference between DRAM and SRAM?

- A) Dynamic RAMs are always active; static RAMs must reset between data read/write cycles
- B) SRAMs can hold data via a static charge, even with power off

- C) The only difference is the terminal from which the data is removed—from the FET Drain or Source
- D) DRAMs must be periodically refreshed

ANSWER: D

A J-K flip-flop with $J = 1$ and $K = 1$ has a 20 kHz clock input. The Q output is _____.

- A) constantly LOW
- B) constantly HIGH
- C) a 20 kHz square wave
- D) a 10 kHz square wave

ANSWER: D

On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____.

- A) the clock pulse is LOW
- B) the clock pulse is HIGH
- C) the clock pulse transitions from LOW to HIGH
- D) the clock pulse transitions from HIGH to LOW

ANSWER: C

What does the term “random access” mean in terms of memory?

- A) Any address can be accessed in systematic order
- B) Any address can be accessed in any order
- C) Addresses must be accessed in a specific order
- D) Any address can be accessed in reverse order

ANSWER: B

@posedge means

- A) Transition from x to 1
- B) Transition from 0 to 1
- C) Transition from z to 1
- D) Transition from 1 to 0

ANSWER: B

What is the hold condition of a flip-flop?

- A) both S and R inputs activated
- B) no active S or R input
- C) only S is active
- D) only R is active

ANSWER: B

The number FF in hexadecimal system has equivalence in digital system to

- A) 239
- B) 240
- C) 255
- D) 256

ANSWER: C

Canonical SOP form of logi expression consists of only _____.

- A) Cells
- B) Literals
- C) Minterms
- D) Maxterms

ANSWER: C

Which illustration from the below stated functions exhibits the conversion of product of maxterm form into sum of minterm form if the value of product of maxterm is $F(x,y,z) = \pi(1, 3, 6)$?

- A) $F(x,y,z) = \sum(0, 2, 4, 5, 7)$
- B) $F(x,y,z) = \pi(0, 2, 4, 5, 7)$
- C) $F(x,y,z) = \sigma(0, 2, 4, 5, 7)$
- D) $F(x,y,z) = S(0, 2, 4, 5, 7)$

ANSWER: A

The expression for Absorption law is given by _____

- A) $A + AB = B$
- B) $AB + AA' = A$

C) $A + AB = A$

D) $A + B = B + A$

ANSWER: C

For the SOP expression $A B' C + A' BC + ABC'$, how many 1s are in the truth table's output column?

A) 1

B) 2

C) 3

D) 4

ANSWER: C

How many gates would be required to implement the following Boolean expression after simplification? $XY + X(X + Z) + Y(X + Z)$

A) 1

B) 2

C) 4

D) 6

ANSWER: B

When grouping cells within a K-map, the cells must be combined in groups of _____

A) 2s

B) Powers of 2

C) 4s

D) Powers of 4

ANSWER: B

Use Boolean algebra to find the most simplified SOP expression for $F = ABD + CD + ACD + ABC + ABCD$

A) $F = ABD + ABC + CD$

B) $F = CD + AD$

C) $F = BC + AB$

D) $F = AC + AD$

ANSWER: A

The NAND or NOR gates are referred to as "universal" gates because either:

- A) can be found in almost all digital circuits
- B) can be used to build all the other types of gates
- C) are used in all countries of the world
- D) were the first gates to be integrated

ANSWER: B

Converting the Boolean expression $LM + M(NO + PQ)$ to SOP form, we get _____.

- A) $LM + MNOPQ$
- B) $L + MNO + MPQ$
- C) $LM + M + NO + MPQ$
- D) $LM + MNO + MPQ$

ANSWER: D

Which statement below best describes a Karnaugh map?

- A) A Karnaugh map can be used to replace Boolean rules.
- B) The Karnaugh map eliminates the need for using NAND and NOR gates.
- C) Variable complements can be eliminated by using Karnaugh maps.
- D) Karnaugh maps provide a cookbook approach to simplifying Boolean expressions.

ANSWER: D

Binary number 1101 is equal to octal number

- A) 14
- B) 15
- C) 16
- D) 17

ANSWER: B

Which of the following combinations cannot be combined into K-map groups?

- A) corners in the same row

- B) corners in the same column
- C) diagonal
- D) overlapping combinations

ANSWER: C

The one input NOR and NAND gate behaves like a

- A) converter
- B) inverter
- C) reflector
- D) differentiator

ANSWER: B

$F = AB + CD + E$ will be implemented with how many minimum number of NAND gates?

- A) 3
- B) 4
- C) 5
- D) 6

ANSWER: D

2's complement of binary number 101011 is

- A) 101010
- B) 010100
- C) 010101
- D) 001011

ANSWER: C

Which is the first logic family?

- A) DTL
- B) RTL
- C) TTL
- D) ECL

ANSWER: A

TTL uses

- A) Multi emitter transistor
- B) Multi collector transistor
- C) Multi base transistor
- D) Multi emitter or multi collector transistor

ANSWER: A

Which of the following statements apply to CMOS devices?

- A) The devices should not be inserted into circuits with the power on.
- B) All tools, test equipment, and metal workbenches should be tied to earth ground.
- C) The devices should be stored and shipped in antistatic tubes or conductive foam.
- D) All of the above.

ANSWER: D

One of De Morgan's theorems states that $(X+Y)' = X' \cdot Y'$. Simply stated, this means that logically there is no difference between:

- A) a NOR and an AND gate with inverted inputs
- B) a NAND and an OR gate with inverted inputs
- C) an AND and a NOR gate with inverted inputs
- D) a NOR and a NAND gate with inverted inputs

ANSWER: A

Which Boolean algebra property allows us to group operands in an expression in any order without affecting the results of the operation [for example, $A + B = B + A$] ?

- A) associative
- B) commutative
- C) distributive
- D) inversion

ANSWER: B

Applying the distributive law to the expression $A(B + C' + D)$, we get _____.

A) $AB + AC + AD$

B) $ABCD$

C) $A + B + C + D$

D) $AB + AC' + AD$

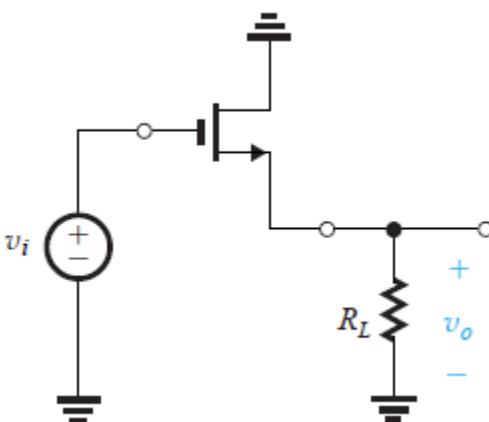
ANSWER: D

Comprehension Fall 2022-23

Analog Circuits

1. Improper Biasing of a transistor circuits leads to
 - a) distortion in output signal
 - b) faulty location of load line
 - c) excessive heating at collector terminal
 - d) heavy loading of emitter terminal
2. In order to achieve good stabilization in voltage divider method current I_L through R_1 and R_2
 - a) $I_L > 2I_B$
 - b) $I_L > 5I_B$
 - c) $I_L < 5I_B$
 - d) $I_L > 10I_B$
3. The universal bias stabilization circuit is most popular because
 - a) Its β sensitivity is high
 - b) I_C is equal to I_E
 - c) Voltage divider is heavily loaded by transistor base
 - d) I_C does not depend on transistor characteristics
4. Reducing the negative feedback in amplifiers which statement is wrong?
 - a) It widens the separation between 3 dB frequencies
 - b) It increases the gain bandwidth product
 - c) It improves gain stability
 - d) It reduces distortion
5. The threshold Voltage of an n-channel MOSFET can be increased by
 - a) Increasing channel doping concentration
 - b) Reducing channel length
 - c) Reducing gate oxide thickness
 - d) decreasing channel doping concentration
6. Consider the following two statements about the internal conditions in an n-channel MOSFET operation in the active region
S1: The inversion charge decreases from source to drain
S2: The channel potential increases from source to drain
Which of the following is correct?
 - a) Only S2 is true
 - b) Both S1 and S2 are false
 - c) Both S1 and S2 are true, but S2 is not a reason for S1
 - d) Both S1 and S2 are true, but S2 is a reason for S1
7. MOSFET can be used as a
 - a) Current controlled capacitor
 - b) Voltage controlled capacitor
 - c) Current controlled inductor
 - d) Voltage controlled inductor

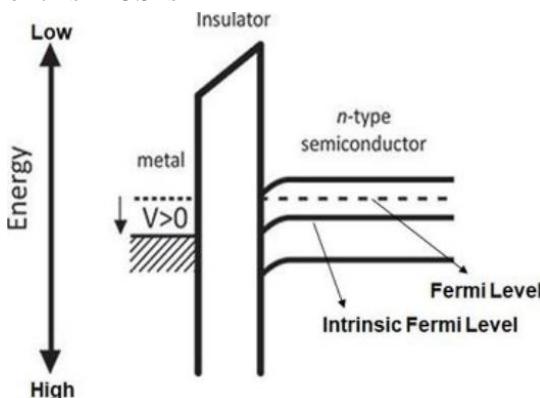
8. A good transconductance amplifier should have
- High input impedance and low output impedance
 - Low input impedance and High output impedance
 - High input and output impedances**
 - Low input and output impedances
9. In CMOS technology ,shallow P-well and N-well regions can be formed using
- Low pressure chemical vapour deposition
 - Low energy sputtering
 - Low temperature dry oxidation
 - Low energy Ion -Implantation**
10. The MOSFET in the following circuit is in which configuration



- a) Common Source (CS)
 b) Common Gate (CG)
c) Common Drain (CD)
 d) None of the mentioned
11. The gain bandwidth product of a two stage CE amplifier is
- Same as that of one stage
 - Greater than that of one stage**
 - Less than that of one stage
 - Product of the two gain bandwidth products of each stage
12. Which capacitance/s in hybrid π model represent/s the storage of excess minority carriers at the base emitter junction?
- Diffusion capacitance**
 - Transition capacitance
 - Both a and b
 - None of the above
13. Miller's theorem is applicable in a single stage CE hybrid π model in order to deal with
- Series combination of C_C and r'_{bc}
 - Series combination of C_e and r'_{be}
 - Parallel combination of C_C and r'_{bc}**
 - Parallel combination of C_e and r'_{be}

14. The bandwidth of an RF tuned amplifier is dependent on Q factor of the
- Tuned output circuit**
 - Tuned input circuit
 - Operating point
 - Output and input circuits as well as quiescent operating point.
15. In the high frequency response of a common emitter amplifier, the coupling and bypass capacitors are treated as
- Open circuit
 - Short Circuits**
 - Both (a) and (b)
 - None of these

16. The figure shows the band diagram of a Metal Oxide Semiconductor (MOS). The surface region of this MOS is in



- Inversion
 - Accumulation**
 - Depletion
 - Flat band
17. In the high frequency MOSFET model capacitances, C_{gs} and C_{gd} capacitances , represent the interaction between the gate and the channel inversion region near the
- Gate and source terminals
 - source and drain terminals**
 - Gate and drain terminals
 - None of the above terminals
18. Determine the unity gain bandwidth of an MOSFET with the parameters $g_m = 1.2 \text{ mA/V}$ $C_{gd} = 10 \text{ fF}$, and $C_{gs} = 50 \text{ fF}$
- 5.18GHz
 - 2.18GHz
 - 3.18GHz**
 - 4.67GHz
19. In common-source amplifier, voltage gain rolls off at _____ frequency because C_{gs} and C_{gd} short out _____ and C_{db} shorts out _____.
- Low, Input, output
 - High, Input, Output**

- c) Low,Output,Input
 - d) None of these
20. In common-source amplifier, effect of _____ on bandwidth is magnified by amplifier ____ gain.
- a) **C_{gd} ,Voltage**
 - b) C_{gs} , Voltage
 - c) C_{ds} ,Current
 - d) None of these
21. The main purpose of using transformer coupling in a class A amplifier is to make it more
- a) **Efficient**
 - b) Less costly
 - c) Less Bulky
 - d) Distortion free
22. The output power of a power amplifier is several times its input power,its is possible because
- a) Power amplifier introduces a negative resistance
 - b) There is positive feedback in the circuit
 - c) Step up transformer is used in the circuit
 - d) Power amplifier converts a part of the input d.c power into a.c power.**
23. Tuned voltage amplifiers are not used
- a) **Public address systems**
 - b) Radio receivers
 - c) in television receivers
 - d) where a band of frequencies is to be selected and amplified
24. A class B push-pull amplifier has the main advantage of being free from
- a) unwanted noise
 - b) circuit imbalance
 - c) even –order harmonic distortion**
 - d) amplitude distortion
25. Class AB operation is often used in power (large signal) amplifiers in order to
- a) get maximum efficiency
 - b) remove even harmonics
 - c) overcome a cross-over distortion**
 - d) reduce collector dissipation
26. A MOS differential amplifier (Fig.1) is operated at a total current of 0.8mA, using transistors with a W/L ratio of 100, $k_n' = \mu_n C_{ox} = 0.2 \text{ mA/V}^2$, $V_A = 20V$, and $R_D = 5k\Omega$. The values of I_d and $V_{ov} = (V_{GS} - V_t)$.

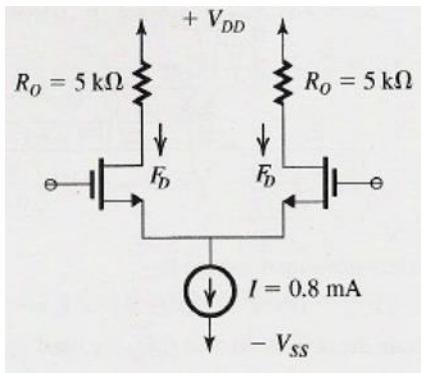


Fig.1. Differential Amplifier

- A) $I_d = 0.8\text{mA}$ and $V_{ov} = 0.2\text{V}$
- B) $I_d = 0.4\text{mA}$ and $V_{ov} = 0.2\text{mV}$
- C) $I_d = 0.8\text{mA}$ and $V_{ov} = 0.2\text{mV}$
- D) $I_d = 0.4\text{mA}$ and $V_{ov} = 0.2\text{V}$

27. The common mode rejection, supply rejection and DC gain of an op-amp and other analog circuits such as switched capacitors and converters are strongly dependent on

- A) Current Mirror
- B) Source Voltage
- C) Positive Feedback
- D) Negative Feedback

28. Which is an important criteria for all the current mirror characteristics.

- A) Input capacitance
- B) Bulk Current
- C) Bandwidth
- D) Impedance matching

29. A MOS differential pair is driven with an input CM level of 1.6V. If $I_{ss}=0.25\text{mA}$, $V_{TH}=0.5\text{ V}$, and $V_{DD}=1.8\text{ V}$, what is the maximum allowable load resistance?

- A) $2.6\text{k}\Omega$
- B) $3.6\text{k}\Omega$
- C) $4.6\text{k}\Omega$
- D) $5.6\text{k}\Omega$

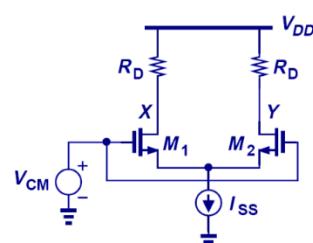


Fig.2. Differential Pair

30. In Cascode current mirror

- A) R_{out} is decreased by the close circuit voltage gain of M_4
- B) R_{out} is increased by the open circuit voltage gain of M_2
- C) R_{out} is increased by the open circuit voltage gain of M_4**
- D) R_{out} is decreased by the open circuit voltage gain of M_2

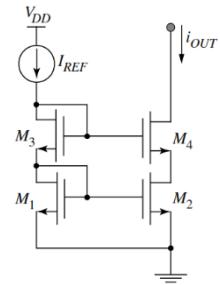


Fig .4

31. Common Source amplifier operated at a total current I_{ref} of 0.5mA, using transistors with a W/L ratio of 100, $k_n' = \mu_n C_{ox} = 0.2 \text{ mA/V}^2$, $V_{Tn} = 15 \text{ V}$, V_{DD} and $R = 10 \text{ k}\Omega$. The value of V_{out} is

- A) 15.1 V**
- B) 15.2 V
- C) 15.3 V
- D) 15.4 V

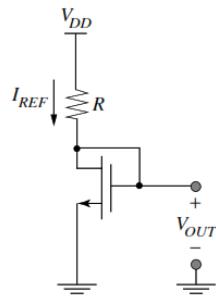


Fig.5

32. Consider the cascode current mirror shown in Fig. 6, where $I_{in} = 100 \mu\text{A}$, $\mu_n C_{ox} = 270 \mu\text{A/V}^2$ and each transistor has $W/L = 10 \mu\text{m} / 0.4 \mu\text{m}$. The g_m and V_{eff} for the current mirror is (neglecting the body effect)

- A. $g_m = 1.16 \text{ mA/V}$ and $V_{eff} = 0.17 \text{ V}$**
- B. $g_m = 1.26 \text{ mA/V}$ and $V_{eff} = 0.27 \text{ V}$
- C. $g_m = 1.36 \text{ mA/V}$ and $V_{eff} = 0.37 \text{ V}$
- D. $g_m = 1.46 \text{ mA/V}$ and $V_{eff} = 0.47 \text{ V}$

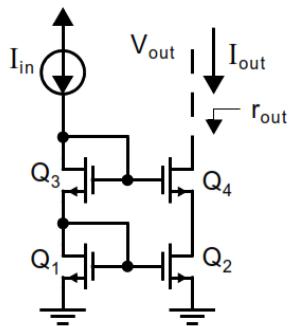


Fig 6. Cascode current mirror

33. Consider the MOSFET circuit shown in Fig. 7, where $I_D = 100 \mu\text{A}$, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ and $g_m = 1000 \mu\text{A/V}$, the W/L ratio is

- A. 10.5
- B. 11.5**
- C. 12.5
- D. 13.5

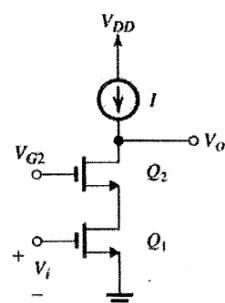


Fig.7.

34. Consider the MOSFET Differential amplifier circuit shown in Fig. 8, where $I_D = 200 \mu A$, $\mu_n C_{ox} = 400 \mu A/V^2$, $\mu_p C_{ox} = 100 \mu A/V^2$ and $g_m = 1000 \mu A/V$, the aspect ratio (W/L)₁₋₂ and (W/L)₃₋₄ are

- A. 25 and 100
- B. 12.5 and 100
- C. 25 and 50**
- D. 12.5 and 75

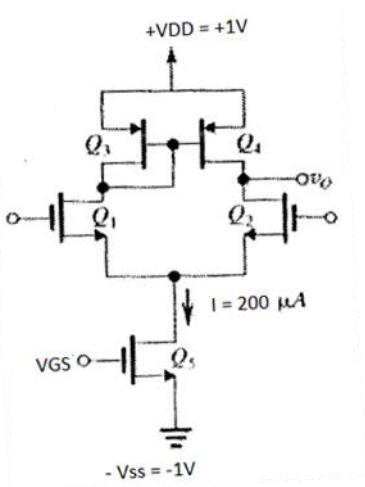


Fig. 7

35. The following theorem is applicable to the amplifier, provided that the amplifier should not have independent source and the open-circuit voltage gain A_{vo} of the amplifier must be negative.

- A. Superposition Theorem
- B. Wilson's Current Mirror Theorem
- C. Miller's Theorem**
- D. Thevenin's Theorem

36. Design an NMOS differential pair for a power budget of 3 mW and $\Delta V_{in,max}=500 \text{ mV}$. Assume $\mu_n C_{ox}=100 \mu A/V^2$ and $V_{DD}=1.8 \text{ V}$. W/L is

- A. 123.6
- B. 133.6**
- C. 143.6
- D. 153.6

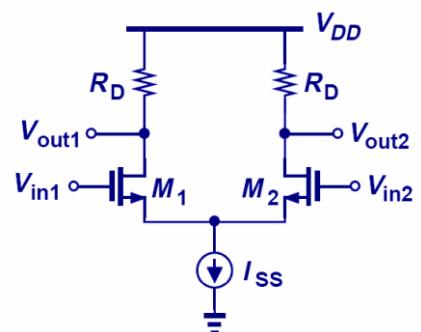


Fig 10. Differential amplifier

37. Which one of the following statement is false

- A. In large signal analysis the large signal values are used to find “small-signal” parameters
- B. In large signal analysis, DC Analysis is used to find the operating point and the bias conditions of circuit.
- C. In small signal analysis, AC Analysis: around the DC bias of the circuit, add a small AC source that slightly increases and decreases the bias point.
- D. In small signal analysis, replace the linear device with non-linear ones.

38. A differential amplifier has a differential mode gain of 1000 and a CMRR of 40 dB. If $V_1 = 0.55$ and $V_2 = 0.45$ V, the output V_0 is

- (A) 10 V
- (B) 10.5 V
- (C) 11 V
- (D) 15 V

39. In the MOSFET amplifier shown in the Fig.12 below, the transistor as $\mu=50$, $r_d=10\text{ k}\Omega$, $C_{gs}=5\text{ pF}$, $C_{gd}=1\text{ pF}$ and $C_{ds}=2\text{ pF}$, its mid-band voltage gain is

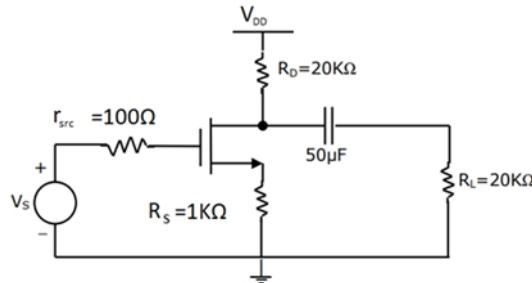


Fig 12. MOSFET amplifier

- A. -8.3
- B. -8.5
- C. 8.5
- D. 8.3

40. An amplifier without feedback has a voltage gain of 50, input Resistance of $1\text{ k}\Omega$ and output Resistance of $2.5\text{ k}\Omega$. The input Resistance of the current-shunt negative feedback factor of 0.2 is

- A. $1/3\text{ k}\Omega$
- B. $1/4\text{ k}\Omega$
- C. $1/5\text{ k}\Omega$
- D. $1/6\text{ k}\Omega$

41. Assuming that transistors M1 and M2 are identical and have a threshold voltage of 1V, the state of transistors M1 and M2 are respectively

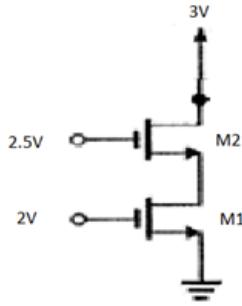


Fig 13. MOSFET amplifier

- A. Saturation, Saturation
- B. Linear, Saturation
- C. Saturation, Linear**
- D. Linear, Linear

42. The regions of operation of MOSFET to work as a linear amplifier and linear resistor are

- A. Cut off and saturation respectively
- B. Triode cut off respectively
- C. Triode and saturation respectively
- D. Saturation and triode respectively**

43. **Statement (I)** : MOSFETs are intrinsically faster than bipolar devices

Statement (II): MOSFETs have excess minority carrier

- A. Both statement(I) and statement (II) are individually true and statement (II) is the correct explanation of statement (I)
- B. Both statement(I) and statement (II) are individually true but statement (II) is not the correct explanation of statement (I)**
- C. Statement (I) is true but statement (II) is false
- D. Statement (I) is false but statement (II) is true

44. An n-channel enhancement mode MOSFET is biased at $V_{BS} > V_{TH}$ and $V_{DS} > (V_{BS} - V_{TH})$, where V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage and V_{TH} is the threshold voltage. Considering channel length modulation effect to be significant, the MOSFET behaves as a

- A. Voltage source with zero output impedance**
- B. Voltage source with non-zero output impedance
- C. Current source with finite output impedance
- D. Current source with infinite output impedance

45. The effect of negative feedback is to increase the _____ of a series voltage negative feedback amplifier by a factor of $(1+A_v\beta)$.

- a) Output impedance
- b) Voltage gain
- c) Input impedance
- d) Bandwidth**

46. Voltage gain of an amplifier without feedback is 70dB. It decreases to 30dB with feedback.

Calculate the feedback factor

- a) 0.00833
- b) 0.01033
- c) 0.01904
- d) 0.02356

47. An amplifier with initial open loop gain 400 is used as feedback amplifier. the feedback factor is 0.05. if the gain of the amplifier changes by 10% due to temperature, then the closed loop gain will change approximately by

- a) 0.1%
- b) 1%
- c) 0.5%
- d) 0.0005%

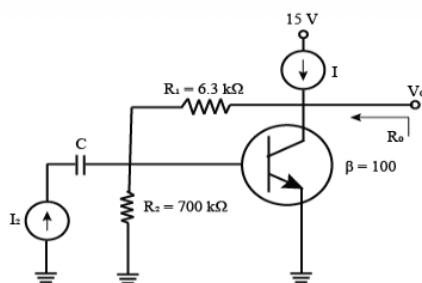
48. An amplifier ha open loop gain of 1000 ± 10 . Negative feedback is provided such that gain variation remains within 0.1%. what is the amount feedback β ?

- a) 9/1000
- b) 1/10
- c) 1/9
- d) 9/100

49. The overall gain of multistage amplifier is 160. When negative voltage feedback is applied the gain is reduced to 13.5.Find the fraction of the output that is feedback to input.

- a) 1/5
- b) 1/14
- c) 1/7
- d) 1/21

50. Consider the shunt-shunt feedback amplifier shown in the figure below.



The transistor is biased at $I_C=3.94$ mA, then the value of the output resistance R_0 is equal to

- a) 68.9 Ω
- b) 560 Ω
- c) 1 kΩ
- d) 10 kΩ

1. In a series RC circuit, the voltage across the resistor is 20 V and the capacitor is 30 V. The angle between the current and source voltage is (in degrees)

- A. 90
- B. 56.3
- C. 45
- D. 180

Ans:B. 56.3

2. A sine wave of 20 V, 5 KHz is applied to a parallel RC circuit with $R=100$ Ohms and $C=0.2 \mu F$. Find the total current.

- A. $0.5+j0.21$ A
- B. $0.2+j0.13$ A
- C. $0.6+j0.45$ A
- D. $0.9+j0.76$ A

Ans:B. $0.2+j0.13$ A

3. If a network contains B branches, and N nodes, then the number of mesh current equations would be

- A. $B-(N-1)$
- B. $N-(B-1)$
- C. $B-N-1$
- D. $(B+N)-1$

Ans:A. $B-(N-1)$

4. A network has 10 nodes and 17 branches. The number of different node pair voltages would be

- A. 7
- B. 9
- C. 45
- D. 10

Ans:B. 9

5. A circuit consists two resistances R_1 and R_2 in parallel. The total current passing through the circuit is I_T . The current passing through R_1 is

A. $I_T R_1 / (R_1 + R_2)$

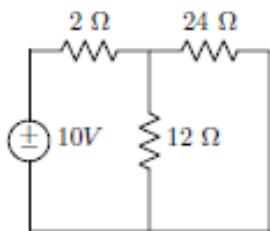
B. $I_T (R_1 + R_2) / R_1$

C. $I_T R_2 / (R_1 + R_2)$

D. $(I_T R_1 + R_2) / R_2$

Ans:C. $I_T R_2 / (R_1 + R_2)$

6. Find the current through the 24 Ohms resistor.



A. 0.33 A

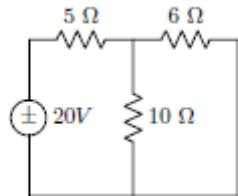
B. 0.12 A

C. 0.23 A

D. 0.43 A

Ans:A. 0.33 A

7. Find the current through the 6 Ohms resistor.



A. 1.43 A

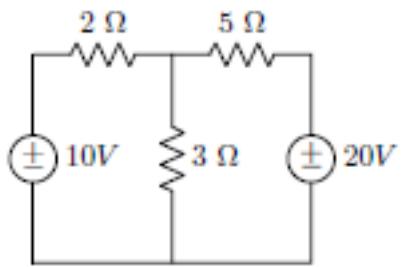
B. 1.22 A

C. 2.23 A

D. 4.43 A

Ans:A. 1.43 A

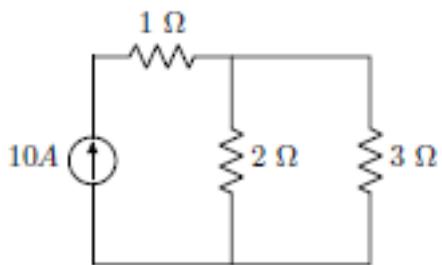
8. Find the current through the 3 Ohms resistor.



- A. 1.9 A
- B. 2.9 A
- C. 3.9 A
- D. 4.9 A

Ans:B. 2.9 A

9. Find the voltage across the 3 Ohms resistor.



- A. 4 V
- B. 8 V
- C. 12 V
- D. 16 V

Ans:C. 12 V

10. Three equal resistances of $3\ \Omega$ are connected in star. What is the resistance in one of the arms in an equivalent delta circuit?

- A. $10\ \Omega$
- B. $3\ \Omega$
- C. $9\ \Omega$

D. 27Ω

Ans:C. 9Ω

11. A sine wave has a frequency of 50 KHz. How many cycles does it complete in 20ms?

A. 1000

B. 10000

C. 500

D. 2000

Ans:A. 1000

12. A sine wave has a peak value of 25 V. Determine the rms value.

A. 17.68 V

B. 50 V

C. 15.93 V

D. None of the above

Ans:A. 17.68 V

13. A sine wave has a peak value of 12 V. Determine the form factor.

A. 1.11

B. 2.11

C. 1.4

D. 0.707

Ans:A. 1.11

14. In a pure capacitor, the voltage

A. is in phase with the current

B. is out of phase with the current

C. lags behind the current by 90 degree

D. leads the current by 90 degree

Ans:C. lags behind the current by 90 degree

15. In a parallel RLC circuit with $R=10 \text{ K } \Omega$, $X_C=18 \Omega$ and $X_L=12 \Omega$, the current

- A. leads the applied voltage
- B. lags behind the applied voltage
- C. is in phase with the voltage
- D. none of the above

Ans:A. leads the applied voltage

16. In a series RC circuit, $V_R=4 \text{ V}$ and $V_C=6 \text{ V}$. What is the magnitude of the total voltage?

- A. 7.2V
- B. 10V
- C. 6V
- D. 52V

Ans:A. 7.2V

17. In a series RLC circuit, $V_R=24 \text{ V}$, $V_L=15 \text{ V}$ and $V_C=45 \text{ V}$. What is the magnitude of the total voltage?

- A. 38.42V
- B. 84V
- C. -8V
- D. 54V

Ans:A. 38.24V

18. A voltage $v(t)=150\sin 250t$ is applied to a series RL circuit with $R=10 \Omega$ and $X_L=j15 \Omega$. Find the average power delivered to the circuit.

- A. 346.6W
- B. 246.6W
- C. 146.5W
- D. 234.6W

Ans:A. 346.6W

19. A sinusoidal voltage of 50 V is applied to a series RC circuit with $R=100 \Omega$ and $X_C=-j200 \Omega$. Find the apparent power.

- A. 11.21 VA

- B. 10.03 VA
- C. 5.01 VA
- D. 21.22 VA

Ans:A. 11.21 VA

20. In a series RC circuit, the true power is 300 W and the reactive power is 1000 W. Find the apparent power.

- A. 1043.9 VA
- B. 1000 VA
- C. 2043.9 VA
- D. 2000 VA

Ans:A. 1043.9 VA

21. In a complex impedance circuit, the maximum power transfer occurs when the load impedance is equal to

- A. complex conjugate of source impedance
- B. source impedance
- C. source resistance
- D. none of the above

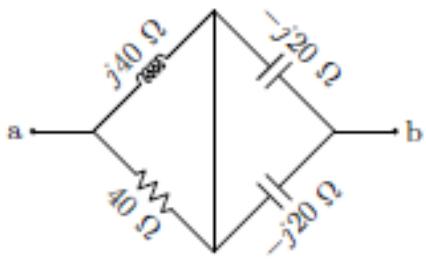
Ans:A. complex conjugate of source impedance

22. Maximum power transfer occurs at a

- A. 100% efficiency
- B. 50% efficiency
- C. 70% efficiency
- D. 25% efficiency

Ans:B. 50% efficiency

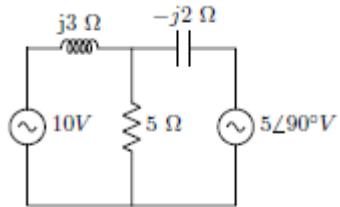
23. From the figure below find the equivalent resistance across a and b.



- A. $20-20j \Omega$
- B. $22.35, 26.56 \text{ deg } \Omega$
- C. $22.35, -26.56 \text{ deg } \Omega$
- D. $20-20j$

Ans: B. $22.35, 26.56 \text{ deg } \Omega$

24. Find the Norton equivalent resistance.



- A. $6,-90 \text{ degree } \Omega$
- B. $6,90 \text{ degree } \Omega$
- C. 5Ω
- D. 0Ω

Ans: A. $6,-90 \text{ degree } \Omega$

25. A 50Ω resistor is connected in parallel with inductive reactance of $j30 \Omega$. A 20 V signal is applied to the circuit. Find the total impedance.

- A. $25.97, 58.8 \text{ deg } \Omega$

- B. 25.97, -58.8 deg Ω
 C. 79, 58.8 deg Ω
 D. 45, 58.8 deg Ω

Ans:A. 25.97, 58.8 deg Ω

Q. 26. Under steady state conditions, the applied DC voltage drops entirely across the _____ when a DC voltage source is connected across a series R-L-C circuit.

- (a) R and L combination (b) C only (c) L only (d) R only

Answer: B

Q. 27. Consider a DC voltage source connected to a series R-C circuit. When the steady state reaches, the ratio of the energy stored in the capacitor to the total energy supplied by the voltage source, is equal to

Answer: A

Q. 28. A series RLC circuit has a resonance frequency of 1 KHz and a quality factor $Q = 150$. If each of R, L and C is doubled from its original value, the new Q of the circuit is

Answer: B

Q. 29. Consider the following statements S1 and S2

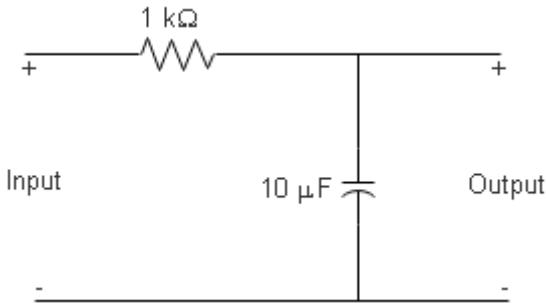
S1: At the resonant frequency the impedance of a series R-L-C circuit is zero

S2: In a parallel G-L-C circuit, increasing the conductance G results in decrease in its Q factor.

Which one of the following is correct?

Answer: C

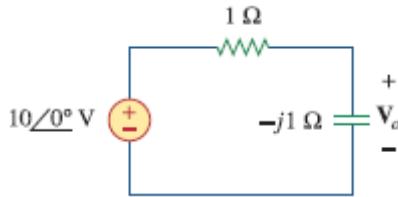
Q.30. In Figure the steady state output voltage corresponding to the input voltage $(3+4\sin 100t)$ V is



- a) $3 + \frac{4}{\sqrt{2}} \sin\left(100t - \frac{\pi}{4}\right) V$
- b) $3 + \frac{4}{\sqrt{2}} \sin\left(100t + \frac{\pi}{4}\right) V$
- c) $3 + 4\sqrt{2} \sin\left(100t - \frac{\pi}{4}\right) V$
- d) $3 + 4 \sin\left(100t - \frac{\pi}{4}\right) V$

Answer: A

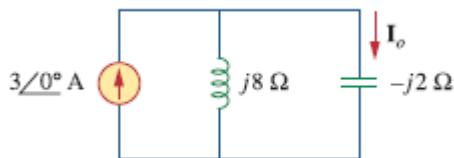
Q. 31. The voltage V_o across the capacitor in the Figure



- a) $5\angle 0^\circ v$
- b) $7.071\angle -45^\circ v$
- c) $7.071\angle 45^\circ v$
- d) $5\angle -45^\circ v$

Answer: B

Q. 32. The value of the current I_o in the circuit shown in Figure.



- a) $4\angle 0^\circ A$
- b) $2.4\angle -90^\circ A$
- c) $0.6\angle 0^\circ A$
- d) $-1A$

Answer: A

Q.33. Which of the following is *not* a right way to express the sinusoid $A \cos \omega t$?

- a) $A \cos 2\pi ft$ b) $A \cos(2\pi t/T)$
 c) $A \cos \omega(t-T)$ d) $A \sin(\omega t - 90^\circ)$

Answer: D

Q. 34. A function that repeats itself after fixed intervals is said to be:

- (a) a phasor (b) harmonic (c) periodic (d) reactive

Answer: C

Q. 35. Which of these frequencies has the shorter period?

- (a) 1 krad/s (b) 1 kHz

Answer: B

Q. 36. If $V_1 = 30 \sin(\omega t + 10^\circ)$ and $V_2 = 20 \sin(\omega t + 50^\circ)$, which of these statements are true?

- a) V_1 leads V_2 b) V_1 lags V_2 c) V_2 leads V_1 d) V_2 lags V_1

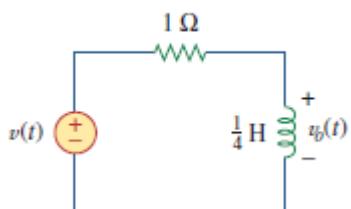
Answer: B,C

Q. 37. The imaginary part of impedance is called:

- (a) resistance (b) admittance
 (c) susceptance (d) conductance (e) reactance

Answer: E

Q. 38. At what frequency will the output voltage $V_o(t)$ in the Figure be equal to the input voltage $v(t)$?



- a) 0 rad/s (b) 1 rad/s (c) 4 rad/s
 (d) ∞ rad/s (e) none of the above

Answer: D

Q. 39. A series RC circuit has $|V_R| = 12V$ and $|V_C| = 5V$. The magnitude of the supply voltage is

- (a) -7 V (b) 7 V (c) 13 V (d) 17 V

Answer: C

Q. 40. A series RCL circuit has $R = 30\Omega$, $X_C = 50\Omega$, and $X_L = 90\Omega$. The impedance of the circuit is:

$$a) 30 + j140\Omega$$

$$b) 30 + j40\Omega$$

$$c) 30 - j40\Omega$$

$$d) -30 - j40\Omega$$

$$e) -30 + j40\Omega$$

Answer: B

Q. 41. The voltage $V = 12 \cos(60t + 45^\circ)$ is applied to a 0.1-H inductor. Then the steady-state current through the inductor is:

$$a) 2 \cos(60t - 45^\circ) A$$

$$b) 2 \cos(60t + 45^\circ) A$$

$$c) 2 \sin(60t - 45^\circ) A$$

$$d) 2 \cos(60t - 90^\circ) A$$

Answer: A

Q. 42. The voltage $V = 10 \cos(100t + 30^\circ)$ is applied to a $50 \mu F$ capacitor. Then the steady-state current through the capacitor is:

$$a) 2 \cos(60t - 45^\circ) mA$$

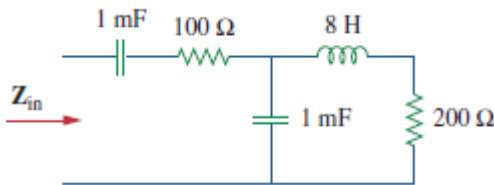
$$b) 50 \cos(100t + 120^\circ) mA$$

$$c) 50 \sin(100t - 120^\circ) mA$$

$$d) 50 \cos(100t - 90^\circ) mA$$

Answer: B

Q.43. The input impedance of the circuit shown in Figure at $\omega = 10 \text{ rad/s}$.



$$a) 100.52 - j150$$

$$b) 149.53 - j195$$

$$c) 149.53 + j195$$

$$d) 50.49 - j100$$

Answer: B

Q. 44. The time domain behavior of an RL circuit is $L \frac{di}{dt} + Ri = V_o \left(1 + Be^{\frac{-Rt}{L}} \sin t \right) u(t)$. for

an initial current of $i(0) = V_0 / R$, the steady state value of the current is given by:

$$a) i(t) \rightarrow \frac{V_0}{R}$$

$$b) i(t) \rightarrow \frac{V_0}{R}(1 + B)$$

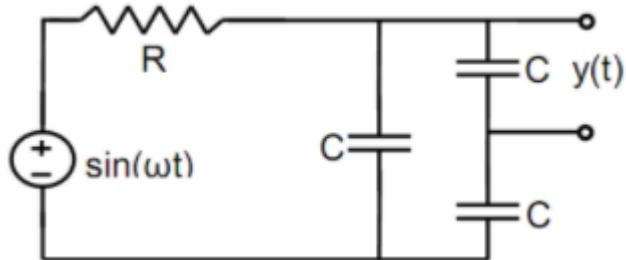
$$c) i(t) \rightarrow \frac{2V_0}{R}$$

$$d) i(t) \rightarrow \frac{2V_0}{R}(1 + B)$$

Answer: A

Q. 45. The steady state output of the circuit shown in Figure is given by

$$y(t) = A(\omega) \sin(\omega t + \varphi(\omega)).$$

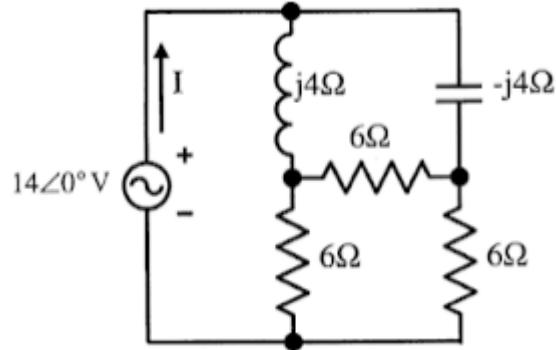


If the amplitude $|A(\omega)| = 0.25$, then the frequency ω is

- a) $\frac{1}{\sqrt{3}RC}$
- b) $\frac{2}{\sqrt{3}RC}$
- c) $\frac{1}{RC}$
- d) $\frac{2}{RC}$

Answer: B

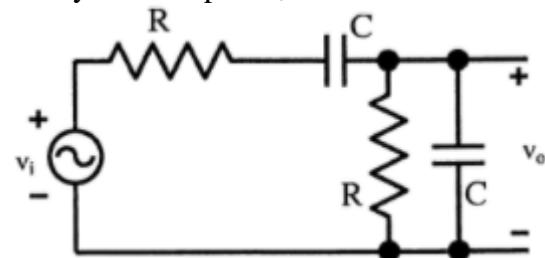
Q. 46. In the circuit shown in Figure, the current I is equal to



- a) $1.4\angle 0^\circ A$
- b) $2.0\angle 0^\circ A$
- c) $2.8\angle 0^\circ A$
- d) $3.2\angle 0^\circ A$

Answer: B

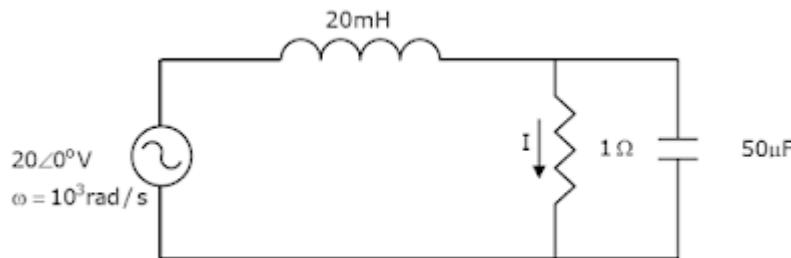
Q. 47. The circuit shown in Figure is driven by a sinusoidal input $V_i = V_p \cos(t / RC)$. The steady state output V_o is



- a) $(V_p / 3)\sin(t / RC)$
- b) $(V_p / 2)\cos(t / RC)$
- c) $(V_p / 2)\sin(t / RC)$
- d) $(V_p / 3)\cos(t / RC)$

Answer: D

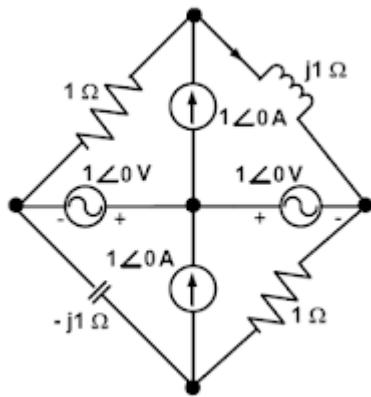
Q. 48. The current I in the circuit is



- a) $-j1A$ b) $j1A$
 c) $0A$ d) $20A$

Answer: A

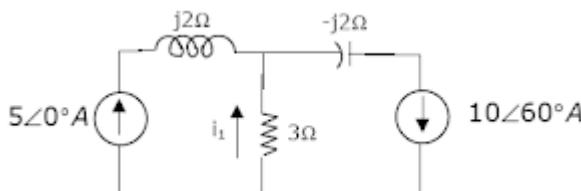
Q. 49. In the circuit shown in Figure, the current through the inductor is



- a) $\frac{2}{1+j}A$ b) $\frac{-1}{1+j}A$
 c) $\frac{1}{1+j}A$ d) $\frac{2}{1-j}A$
 e) $0A$

Answer: C

Q. 50. For the circuit shown in Figure, the instantaneous current $i_1(t)$ is



- a) $\frac{10\sqrt{3}}{2}\angle90^\circ A$ b) $\frac{10\sqrt{3}}{2}\angle-90^\circ A$
 c) $5\angle60^\circ A$ d) $5\angle-60^\circ A$

Answer: A

51. Laplace transform of the output response of a linear system is the system transfer function when the input is

- (i) a step signal
- (ii) a ramp signal
- (iii) an impulse signal

(iv) a sinusoidal signal

Ans: (iii) an impulse signal

52. The value of the impulse function at $t=0$ is

- (i) 0
- (ii) 1
- (iii) Infinity
- (iv) Indeterminate

Ans: (ii) 1

53. The value of the ramp function at time $t = \infty$ is

- (i) infinity
- (ii) unity
- (iii) zero
- (iv) indeterminate

Ans: (i) infinity

54. Time constant of a series RC circuit is

- (i) C/R
- (ii) R/C
- (iii) RC
- (iv) $1/RC$

Ans: (iii) RC

55. Time constant of a series RL circuit is

- (i) L/R
- (ii) R/L
- (iii) LR
- (iv) $1/LR$

Ans: (i) L/R

56. At $t=0$ with zero initial condition which of the following will act as a short circuit?

- (i) Inductor
- (ii) Capacitor
- (iii) Resistor
- (iv) None of the Options

Ans: (ii) Capacitor

57. At $t=0$ with zero initial condition which of the following will act as a open circuit?

- (i) Inductor
- (ii) Capacitor
- (iii) Resistor
- (iv) None of the Options

Ans: (i) Inductor

58. A 10- resistor, a 1-H inductor and a 1-F capacitor are connected in parallel. The combination is driven by a unit step current. Under steady-state conditions, the source current flows through the

- (i) resistor
- (ii) inductor
- (iii) capacitor only
- (iv) all the three elements

Ans: (ii) inductor

59. The impulse response of an RL circuit is a

- (i) rising exponential function
- (ii) decaying exponential function
- (iii) step function
- (iv) parabolic function

Ans: (ii) decaying exponential function

60. If the step response of an initially relaxed circuit is known then the ramp response can be obtained by

- (i) integrating the step response
- (ii) differentiating the step response
- (iii) integrating the step response twice
- (iv) differentiating the step response twice

Ans: (i) integrating the step response

61. The Laplace transform method enables one to find the response in

- (i) the transient state only
- (ii) the steady state only
- (iii) both transient and steady states
- (iv) the transient state provided sinusoidal forcing functions do not exist.

Ans: (iii) both transient and steady states

62. A non-linear system cannot be analyzed by Laplace transform because

- (i) it has no zero initial conditions
- (ii) superposition law cannot be applied
- (iii) non-linearity is generally not well defined
- (iv) All the options

Ans: (i) it has no zero initial conditions

63. A high Q coil has

- (i) large bandwidth
- (ii) high losses
- (iii) low losses
- (iv) flat response

Ans: (iii) low losses

64. The Q of a circuit can be increased by

- (i) increasing the bandwidth
- (ii) decreasing the bandwidth

- (iii) increasing R
 - (iv) None of the Options
- Ans: (ii) decreasing the bandwidth

65. In a series RLC circuit, the maximum voltage across the inductor occurs at a frequency
- (i) equal to resonant frequency
 - (ii) less than resonant frequency
 - (iii) greater than resonant frequency
 - (iv) None of the Options
- Ans: (iii) greater than resonant frequency
66. An RLC series circuit consists of a resistance of $1\text{k}\Omega$, an inductance of 0.1 H and a capacitance of 10 micro-farad. The Q-factor of the circuit will be
- (i) 100
 - (ii) 50
 - (iii) 10
 - (iv) 0.01
- Ans: (i) 100
67. A capacitor of 0.01 farad has a leakage resistance of 100 ohms across its terminals. The quality factor of it at 10rad/s should be
- (i) 0.1
 - (ii) 1
 - (iii) 10
 - (iv) 100
- Ans: (i) 0.1
68. An RLC resonant circuit has a resonant frequency of 1.5 MHz and a bandwidth of 10 kHz. If $C=150\text{ F}$, then the effective resistance of the circuit will be
- (i) $29.5\ \Omega$
 - (ii) $14.75\ \Omega$
 - (iii) $9.4\ \Omega$
 - (iv) $4.7\ \Omega$
- Ans: (iv) $4.7\ \Omega$
69. In a parallel RLC circuit, if $L=4\text{ H}$, $C=0.25\text{ F}$ and $R=40\Omega$ then the value of Q at resonance will be
- (i) 1
 - (ii) 10
 - (iii) 20
 - (iv) 40
- Ans: (ii) 10
70. In an RLC parallel circuit, at resonance the circuit is
- (i) Purely resistive
 - (ii) Purely inductive
 - (iii) Purely capacitive
 - (iv) None of the options
- Ans: (i) Purely resistive

71. In an RLC series resonant circuit, at half-power points

- (i) the current is half of the current at resonance
- (ii) the impedance is half the impedance at resonance
- (iii) the resistance is equal to the resultant reactances
- (iv) none of the option

Ans: (iv) none of the option

72. If two two-port networks are connected in series, and if the port current requirement is satisfied, which of the following is true?

- (i) The z-parameter matrices add
- (ii) The y-parameter matrices add.
- (iii) The ABCD-parameter matrices add.
- (iv) None of the option

Ans: (i) The z-parameter matrices add

73. If two two-port networks are connected in parallel, and if the port current requirement is satisfied, which of the following is true?

- (i) The z-parameter matrices add
- (ii) The y-parameter matrices add.
- (iii) The ABCD-parameter matrices add.
- (iv) None of the option

Ans: (ii) The y-parameter matrices add.

74. The quality factor of series RLC increases if

- (i) R decreases
- (ii) R increases
- (iii) impedance increases
- (iv) voltage increases

Ans: (i) R decreases

75. In a series resonant circuit, with the increase in L

- (i) resonant frequency will decrease
- (ii) bandwidth will decrease
- (iii) Q will increase
- (iv) all of the options

Ans: (iv) all of the options

ECM4098 - COMPREHENSIVE EXAMINATION

Module 5: Microcontroller and Embedded Systems

Microcontroller: 8-bit/16-bit Microprocessor Architectures [8085, 8086], - ARM7, Intel I (i3, i5, i7) series processors - 8051 architecture – Instruction set -8051- Peripherals: timer and ports- serial and interrupt- Peripheral Interfacing: LCD, LED, keypad- ADC, DAC, sensor with signal conditioning

1. Number of bit addressable memory present in 8051 microcontroller

- A) 32 bytes
- B) 16 bytes
- C) 8 bytes
- D) 128 bytes

ANSWER: B

2. Bit-addressable memory locations in 8051 are:

- A) 10H through 1FH
- B) 20H through 2FH
- C) 30H through 3FH
- D) 40H through 4FH

ANSWER: B

3. For the instruction given below in 8051 microcontrollers, which of the following holds good?

MOV A,#9CH

ADD A,#64H

- A) CY=0,AC=0,P=0
- B) CY=1,AC=1,P=0
- C) CY=0,AC=1,P=0
- D) CY=1,AC=1,P=1

ANSWER: B

4. When Bank2 of 8051 is selected, which of the following is true?

- A) PSW.5=0 and PSW.4=1
- B) PSW.2=0 and PSW.3=1
- C) PSW.3=1 and PSW.4=1
- D) PSW.3=0 and PSW.4=1

ANSWER: D

5. In 8051 microcontroller, “DJNZ R0, label” instruction is _____ byte.

- A) 2
- B) 3
- C) 1
- D) Can't be determined

ANSWER: A

6. In 8051 microcontrollers _____ register is checked by JZ, JNZ, instructions.

- A) DPTR
- B) A
- C) PSW
- D) B

ANSWER: B

7. If 8051 microcontroller the crystal frequency is 20MHz, what is the time taken by one machine cycle.

- A) 0.60 micro seconds
- B) 1.085 micro seconds
- C) 1 micro second
- D) 0.75 micro seconds

ANSWER: A

8. The internal RAM memory of the 8051 is

- A) 64 bytes
- B) 256 bytes
- C) 128 bytes

D) 32 bytes

ANSWER: C

9. 8051 can handle ----- interrupt sources

A) 5

B) 3

C) 4

D) 8

ANSWER: A

10. The 8051 microcontroller is of ___ pin package as a _____ processor

A) 30, 1 byte

B) 40, 8 byte

C) 20, 1 byte

D) 40, 8 bit

ANSWER: D

11. The Stack Pointer (SP) is of 8051 is ___ wide register and this may be defined anywhere in the

A) 8 bit, on chip 128 byte RAM

B) 8 byte, on-chip 128 byte RAM

C) 8 bit, on chip 256 byte RAM

D) 16 bit, on-chip 128 byte ROM

ANSWER: A

12. After reset, Stack Pointer (SP) register is initialized to address _____ in 8051 microcontrollers

A) 8H

B) 9H

C) 7H

D) 6H

ANSWER: C

13. What is the address range of SFR Register bank in 8051 microcontroller?

- A) 00H-77H
- B) 40H-80H
- C) 80H-FFH
- D) 80H-7FH

ANSWER: C

14. When the call instruction is executed in 8051 the topmost element of stack comes out to be?

- A) the address where stack pointer starts
- B) the address next to the call instruction
- C) address of the call instruction
- D) next address of the stack pointer

ANSWER: B

15. In 8051 microcontrollers, number of times the following loop will be executed is

MOV R6,#100

BACK:MOV R5,#50

HERE:DJNZ R5, HERE

DJNZ R6,BACK

END

- A) 5000
- B) 500
- C) 50
- D) 100

ANSWER: A

16. The meaning of the instruction MOV A, 05H in 8051 microcontrollers?

- A) data 05H is stored in the accumulator
- B) fifth bit of accumulator is set to one
- C) data in address 05H is stored in the accumulator
- D) none of the mentioned

ANSWER: C

17. Which of the following command in 8051 will move the number 27H into the accumulator?

- A) MOV A, P27
- B) MOV A, #27H
- C) MOV A, 27H
- D) MOV A, @27

ANSWER: B

18. Which of the following architecture family is a base for present day intel i3, i5 and i7 processors?

- A) x86
- B) 8051
- C) x85
- D) DSP

ANSWER: A

19. The instructions which affect the program counter in 8051 microcontrollers is

- A) Call & Return
- B) Call & Jump
- C) Push & Pop
- D) Return & Jump

ANSWER: B

20. The commands used for addressing the off-chip data and associated codes respectively by data pointer in 8051 microcontroller is

- A) MOVC & MOVY
- B) MOVX & MOVY
- C) MOVZ & MOVA
- D) MOVX & MOVC

ANSWER: D

21. The operations performed by bit-manipulating instructions in 8051 microcontroller is

- A) complement bit
- B) Set bit
- C) Clear bit
- D) All of these

ANSWER: D

22. The reason for the speed accessibility of external data memory slower than internal on-chip RAM

- A) Due to multiplexing of lower order byte of address-data bus
- B) Due to demultiplexing of higher order byte of address-data bus
- C) Due to multiplexing of higher order byte of address-data bus
- D) Due to demultiplexing of lower order byte of address-data bus

ANSWER: A

23. In 8051 microcontrollers, the register which holds the eighth bit divisor and store the remainder, after executing division operation

- A) A Register
- B) B Register
- C) Registers R0 through R7
- D) None of these

ANSWER: B

24. Which of the following command in 8051 will copy the contents of RAM whose address is in register 0 to port 1?

- A) MOV @ P1, R0
- B) MOV @ R0, P1
- C) MOV P1, @ R0
- D) MOV P1, R0

ANSWER: C

25. The total amount of external code memory that can be interfaced to the 8051 is

- A) 32K

B) 64K

C) 128K

D) 256K

ANSWER: B

26. What is the counting rate of a machine cycle in correlation to the oscillator frequency for 8051 timers?

A) 1 / 10

B) 1 / 12

C) 1 / 15

D) 1 / 20

ANSWER: B

27. Which special function register play a vital role in the 8051 timer/counter mode selection process by allocating the bits in it?

A) TMOD

B) TCON

C) SCON

D) PCON

ANSWER: A

28. Find out the roll over value for the 8051 timer in Mode 0, Mode 1 and Mode 2?

A) 00FFH,0FFFH,FFFFH

B) 1FFFH,0FFFH,FFFFH

C) 1FFFH,FFFFH,00FFH

D) 1FFFH,00FFH,FFFFH

ANSWER: C

29. The banked registers in ARM processors are used for _____?

A) Switching between supervisor and interrupt mode

B) Extended storing

C) Same as other general purpose registers

D) None of the mentioned

ANSWER: A

30. Which bit must be set in TCON register of 8051 in order to start the 'Timer 0' while operating in 'Mode 0'?

A) TR0

B) TF0

C) IT0

D) IE0

ANSWER: A

31. What is the maximum delay generated by the 12 MHz clock frequency in accordance to an auto-reload mode (Mode 2) operation of the 8051 timer?

A) 125 μ s

B) 250 μ s

C) 256 μ s

D) 1200 μ s

ANSWER: C

32. Which among the below mentioned sequence of program instructions represent the correct chronological order for the generation of 2kHz square wave frequency using 8051 timer?

1. MOV TMOD, 0000 0010 B

2. MOV TL0, # 06H

3. MOV TH0, # 06H

4. SETB TR0

5. CPL p1.0

6. ORG 0000H

A) 6, 5, 2, 4, 1, 3

B) 6, 1, 3, 2, 4, 5

C) 6, 5, 4, 3, 2, 1

D) 6, 2, 4, 5, 1, 3

ANSWER: B

33. Which factor is supposed to have the equal values at both phases of transmission and reception levels with an intimation of error-free serial communication in 8051?

- A) Baud Rate
- B) Number of data bits & stop bits
- C) Status of Parity bits
- D) All of these

ANSWER: D

34. Which bits exhibit and signify the termination phase of the character transmission and reception in 8051 SCON special function register?

- A) Control bits
- B) Status bits
- C) Monitor bits
- D) None of these

ANSWER: B

35. In 8051 microcontrollers, which one of the following is valid for MOV SCON, #88H?

- A) 8-bit, 1-start bit, 1-stop bit, Receive enabled
- B) 9-bit, 1-start bit, 1-stop bit, Receive disabled
- C) 9-bit, 1-start bit, 1-stop bit, Receive enabled
- D) 8-bit, 1-start bit, 1-stop bit, Receive disabled

ANSWER: B

36. To use 8051 Timer1 as counter, the clock pulse is applied to pin_____

- A) P3.4
- B) P3.5
- C) P3.6
- D) P3.7

ANSWER: A

37. In 8051, mode _____ the timer counts up to 13 bits

- A) Mode 0
- B) Mode 1
- C) Mode 2
- D) Mode 3

ANSWER: A

38. Select the interrupt with lowest priority _____ in 8051

- A) External Interrupt 0 (IE0)
- B) External Interrupt 1 (IE1)
- C) Serial Interrupt
- D) Timer Interrupt 0

ANSWER: C

39. What should be done if we want to double the baud rate in 8051?

- A) change a bit of the TMOD register
- B) change a bit of the PCON register
- C) change a bit of the SCON register
- D) change a bit of the SBUF

ANSWER: B

40. What is the function of the SCON register in 8051?

- A) to control SBUF and SMOD registers
- B) to program the start bit, stop bit, and data bits of framing
- C) to control SMOD registers
- D) none of the mentioned

ANSWER: B

41. What is the bit transmitting or receiving capability of mode 1 in 8051 serial communication

- A) 8 bits
- B) 10 bits

C) 11 bits

D) 12 bits

ANSWER: B

42. In 8051 an external interrupt 1 vector address is of _____ and causes of interrupt if _____.

A) 000BH, a high to low transition on pin INT1

B) 001BH, a low to high transition on pin INT1

C) 0013H, a high to low transition on pin INT1

D) 0023H, a low to high transition on pin INT1

ANSWER: C

43. In 8051, Serial port vector address is of _____. And causes an interrupt when _____.

A) 0013H, either TI or RI flag is set

B) 0023H, either TI or RI flag is reset

C) 0013H, either TI or RI flag is reset

D) 0023H, either TI or RI flag is set

ANSWER: D

44. Which bit of TMOD will exactly configure 8051 timer / counter as a timer or counter.

i) TMOD.6 of C/T for timer 1

ii) TMOD.6 of C/T for timer 0

iii) TMOD.2 of C/T for timer 0

iv) TMOD.2 of C/T for timer 1

A) i, ii

B) ii, iv

C) i, iii

D) iii, iv

ANSWER: C

45. Select the 8051 port which can't serve multiple functionality

A) Port 0

B) Port 1

C) Port 2

D) Port 4

ANSWER: B

46. Port ____ and Port ____ combine to give the 16-bits wide lines to interface with external memory in 8051.

A) 0, 1

B) 0, 2

C) 1, 2

D) 0, 3

ANSWER: B

47. There are _____ general purpose registers in 8085 processors.

A) 5

B) 6

C) 7

D) 8

ANSWER: B

48. When the port lines of a port are to be used as input lines then the value that must be written to the 8051 port address is

A) F0H

B) 0FH

C) FFH

D) 00H

ANSWER: C

49. The 8051 has _____ parallel I/O ports

A) 2

B) 3

C) 4

D) 5

ANSWER: C

50. In 8051, EA bit of IE (Interrupt Enable) Register is used to

- A) enable or disable external interrupts
- B) enable or disable internal interrupts
- C) enable or disable all the interrupts
- D) none of the mentioned

ANSWER: C

51. While interfacing 8051 with 16x2 LCD, What does 16 x 2 typical value indicate?

- A) 16 lines per character with 2 such lines
- B) 16 characters per line with 2 such lines
- C) 16 pixels per line with 2 such sets
- D) 16 lines per pixel with two such sets

ANSWER: B

52. While interfacing 8051 with LCD, which control line/s act/s as an initiator by apprising LCD about the inception of data transmission by the microcontroller?

- A) Enable (EN)
- B) Register Select (RS)
- C) Read/Write (RW)
- D) VEE

ANSWER: A

53. Match the following with respect to 8086 Microprocessor?

Column-1	Column-2
a) Address bus size (in bits)	i) 16
b) No. of Instruction Queue size (in Bytes)	ii) 20
c) Stack Pointer size (in bits)	iii) 6
d) AL register Size (in bits)	iv) 8

- A) a)-ii), b)-iii), c)-i), d)-iv)

B) a)-iii), b)-ii), c)-i), d)-iv)

C) a)-i), b)-iii), c)-ii), d)-iv)

D) a)-ii), b)-iv), c)-i), d)-iii)

ANSWER: A

54. While interfacing 8051 with LCD, when can a LCD display the text form of data?

A) only when RS line is high

B) only when RW line is high

C) only when RS line is low

D) only when RW line is low

ANSWER: A

55. How many data lines are essential in addition to RS , EN and RW control lines for interfacing LCD with 8051 microcontroller?

A) 3

B) 5

C) 8

D) 10

ANSWER: C

56. While interfacing 8051 with keypad, which of the following steps detects the key in a 4*4 keyboard matrix about the key that is being pressed?

A) masking of bits

B) ensuring that initially, all keys are open

C) checking that whether the key is actually pressed or not

D) all of the mentioned

ANSWER: D

57. While interfacing 8051 with keypad, what is described by this command:

`CJNE A,#00001111b, ROW1`

A) it masks the bit and then jumps to the label where ROW1 is written

B) it makes the value of the accumulator 0FH and then jumps at the address where ROW1 label is written

C) it compares the value of the accumulator with 0FH and jumps to the location where ROW1 label is there if the value becomes equal

D) it compares the value of the accumulator with 0FH and jumps to the location where ROW1 label is there if the value is not equal

ANSWER: D

58. While interfacing 8051 with keypad, to identify that which key is being pressed, we need to

A) ground all the pins of the port at a time

B) ground pins of the port one at a time

C) connect all the pins of the port to the main supply at a time

D) none of the mentioned

ANSWER: B

59. While interfacing 8051 with keypad, analyze the following figure and identify the key pressed if the value read from Port P1=BA (hex).

A) 8

B) 5

C) 9

D) 7

ANSWER: A

60. While interfacing 4 x 4 matrix keypad with 8051, rows and columns of keypad must be configured as.....respectively

A) output, input

B) input, input

C) input, output

D) output, output

ANSWER: A

61. Which interfacing 8051 with ADC0804 which one of the following pin used indicate start of conversion

A) CS

B) INTR

C) WR

D) RD

ANSWER: C

62. Which interfacing 8051 with ADC0804, why two pins for ground are available in ADC0804?

A) for controlling the ADCON0 and ADCON1 register of the controller

B) for controlling the analog and the digital pins of the controller

C) for both parts of the chip respectively

D) for isolate analog and digital signal

ANSWER: D

63. State which of the following statements are false with respect to 8051 interface with ADC0804

A) CLK IN pin used for External Clock Input or Internal Clock with external RC element

B) INTR pin tells about the end of the conversion

C) ADC0804 IC is an 8 bit parallel ADC in the family of the ADC0800 series

D) None of the mentioned

ANSWER: D

64. Which interfacing 8051 with ADC0804 what steps are followed?

A) select the analog channel, start the conversion, monitor the conversion, display the digital results

B) select the analog channel, activate the ALE signal (L to H pulse), start the conversion, monitor the conversion, read the digital results

C) select the analog channel, activate the ALE signal (H to L pulse), start the conversion, monitor the conversion, read the digital results

D) select the channel, start the conversion, end the conversion

ANSWER: B

65. Choose the correct option based on True/False conditions of following statement with respect to 8085 Microprocessor?

i) It has two 16-bit timers Timer 0 & 1

ii) RST5.5 is one of the Hardware interrupt source

iii) It has eight 8-bit general purpose registers

iv) Program Counter is 16-bit in size

- A) i-False, ii-True, iii-False, iv-True
- B) i-False, ii-True, iii-True, iv-False
- C) i-True, ii-False, iii-False, iv-True
- D) i-True, ii-False, iii-True, iv-False

ANSWER: A

66. While interfacing 8051 with 8-input DAC will have _____

- A) 8 discrete voltage levels
- B) 64 discrete voltage levels
- C) 128 discrete voltage levels
- D) 256 discrete voltage levels

ANSWER: D

67. The ADC0804 has _____ resolution

- A) 4-bit
- B) 8-bit
- C) 10-bit
- D) 12-bit

ANSWER: B

68. Why Vref is set of ADC to 2.56 V if analog input is connected to the LM35?

- A) to set the step size of the sampled input
- B) to set the ground for the chip
- C) to provide supply to the chip
- D) all of the mentioned

ANSWER: A

69. What steps have to be followed for interfacing a sensor to a micro controller 8051?

- A) make the appropriate connections with the controller, ADC conversion, analyse the results
- B) make connections of 8051 with an ADC to convert analog voltage to digital one , send this digital value to the controller, analyse the results

C) interface sensor with the MAX232, send now to micro controller, analyse the results

D) none of the mentioned

ANSWER: B

70. The Intel 8085 microprocessor is a _____ processor.

A) 4-bit

B) 8-bit

C) 16-bit

D) 32-bit

ANSWER: B

71. Given a 10-bit DAC with $V_{ref} = 3.3v$ and an input voltage of $V_s = 1.15v$ applied to pin A5, what digital number will be returned?

A) 1024

B) 356

C) 371

D) 724

ANSWER: B

72. What is the purpose of signal condition while interfacing an 8051 microcontroller with sensor.

A) to analyse any signal

B) conversion or modification is referred to as conditioning

C) conversion from analog to digital is signal conditioning

D) conversion from digital to analog is signal conditioning

ANSWER: B

73. While interfacing 8051 with DAC0808, converted analog output from digital inputs are acquired via

A) Comp

B) A1

C) IO

D) NC

ANSWER: C

74. Which one of the following operation is not commonly carried out by op-amp as a signal conditioning unit in 8051?

- A) Signal amplification
- B) Filtering
- C) I-V conversion
- D) circuit protection

ANSWER: D

75. The Intel 8086 microprocessor is a _____ processor.

- A) 4-bit
- B) 8-bit
- C) 16-bit
- D) 32-bit

ANSWER: C

ECM 2001 - Data Communication Networks

Comprehensive Examination

1. When a host on network A sends a message to a host on network B, which address does the router look at?
 - A. port
 - B. logical**
 - C. physical
 - D. none of the above

Answer: B

2. To deliver a message to the correct application program running on a host, the _____ address must be consulted.
 - A. port**
 - B. IP
 - C. physical
 - D. none of the above

Answer: A

3. The _____ layer is responsible for delivering data units from one station to the next without errors.
 - A. transport
 - B. network
 - C. data link**
 - D. physical

Answer: C

4. The _____ layer ensures interoperability between communicating devices through transformation of data into a mutually agreed upon format.
 - A. transport
 - B. network
 - C. data link
 - D. presentation**

Answer: D

5. The _____ address uniquely defines a host on the Internet.
 - A. physical
 - B. IP**
 - C. port
 - D. specific

Answer: B

6. _____ is actually a multiport repeater. It is normally used to create connections between stations in a physical star topology.

- A. An active hub**
- B. A passive hub
- C. either of the options
- D. None of the options

Answer: A

7. IEEE 802.1d specification, defines _____ criteria for a transparent bridges.
- A. two
 - B. three**
 - C. four
 - D. none of the above

Answer: B

8. _____ is the protocol suite for the current Internet.
- A. TCP/IP**
 - B. NCP
 - C. UNIX
 - D. ACM

Answer: A

9. In a bridged LAN, the _____ algorithm creates a topology in which each LAN can be reached from any other LAN through one path only.
- A. spanning tree**
 - B. binary tree
 - C. unary tree
 - D. none of the above

Answer: A

10. In the OSI model, as a data packet moves from the lower to the upper layers, headers are _____.
- A. added
 - B. removed**
 - C. rearranged
 - D. modified

Answer: B

11. A _____ forwards every frame; it has no filtering capability
- A. Passive hub
 - B. Repeater**
 - C. Bridge
 - D. Router

Answer: B

12. Some new two-layer switches, called _____ switches, have been designed to forward the frame as soon as they check the MAC addresses in the header of the frame
- A. cut-through**

- B. go-through
- C. come-through
- D. none of the above

Answer: A

13. Mail services are available to network users through the _____ layer.

- A. Data link
- B. Physical
- C. Transport
- D. Application**

Answer: D

14. Which of the following is true?

- A. ARP (Address Resolution Protocol) is used to determine the IP address from MAC address
- B. DHCP (Dynamic Host Configuration Protocol) is used to determine the IP address from MAC address.
- C. A computer can never have the same IP Address and MAC address.**
- D. CRC (Cyclic Redundancy Check) is used to correct errors.

Answer: C

15. Which topology requires a multipoint connection?

- A. Mesh
- B. Star
- C. Bus**
- D. Ring

Answer: C

16. Which topology requires a central controller or hub?

- A. Mesh
- B. Star**
- C. Bus
- D. Ring

Answer: B

17. Compute the number of duplex-links required to connect 10 devices using Mesh

- A. 10
- B. 45**
- C. 9
- D. 90

Answer: B

18. State which of the statements are true. Suppose a computer is moved from one department to another.

- A. Both the physical address and IP address will change
- B. Its physical address will change but IP address will not change
- C. Both the physical address and IP address will not change
- D. Its physical address will not change but IP address may change.**

Answer: D

19. Using stop and wait protocol, sender wants to transmit 13 data packets to the receiver. Out of these 13 data packets, every 3rd data packet is lost. How many packets sender will have to send in total?

- A. 20
- B. 16
- C. 19**
- D. 17

Answer: C

20. Consider a Go-back N ARQ protocol, where 10 bit sequence number is used. What is the size of the transmitter window?

- A. 1024
- B. 512
- C. 1023**
- D. 2048

Answer: C

21. Out of the following which denotes MAC address?

- A. Az32:6362:2434
- B. BA:AB:2276
- C. 1010:1234:5674:5789
- D. ABCD:AABB:DCBA**

Answer: D

22. Find the wrong one in the following statements.

- A. Asynchronous Transfer Mode (ATM) is a cell relay protocol
- B. ATM can handle real-time transmission
- C. ATM data packet is a cell composed of 52 bytes**
- D. ATM technology can be adopted for use in a LAN

Answer: C

23. Consider a CSMA/CD network that transmits data at a rate of 100 Mbps over 1 Km cable with no repeaters. If the minimum frame size required for this network is 2000 bytes. What is the signal propagation speed (Km/sec) in the cable?

- A. 25,000
- B. 12,500**
- C. 50,000
- D. 6,250

Answer: B

24. If the HDLC flag field pattern is found in the message data field, it needs to be altered through _____

- A. Byte stuffing
- B. Bit synchronization
- C. Byte synchronization
- D. None of these**

Answer: D

25. A sender uses the stop and wait ARQ protocol for reliable transmission of frames. Frames are of size 1000 bytes and the transmission rate at the sender is 40 Kbps. Size of an acknowledgement is 100 bytes and the transmission rate at the receiver is 8 Kbps. The one way propagation delay is 100 msec. Find the efficiency (Assuming no frame is lost).

- A. 30%
- B. 40%**
- C. 50%
- D. 60%

Answer: 40%

26. A network using CSMA/CD has a bandwidth of 10 Mbps. If the maximum propagation time (including the delays in the devices and ignoring the time needed to send a jamming signal) is 51.2 μ s, what is the minimum size of the frame?

- A. 128 bytes**
- B. 256 bytes
- C. 512 bytes
- D. 1024 bytes

Answer: A

27. A sender using stop and wait ARQ sends data frames numbered _____

- A. 0 and 1 only**
- B. Sequentially, beginning with 0

- C. Sequentially, beginning with 1
- D. Frames are not numbered

Answer: A

28. Priority to nodes can be given in wireless networks by using

- A. **Interframe spacing**
- B. RTS CTS
- C. Contention Window
- D. All of these

Answer: A

29. Assume that, in a Stop-and-Wait ARQ system, the bandwidth of the line is 1 Mbps, and 1 bit takes 20 ms to make a round trip. What is the bandwidth-delay product?

- A. 10,000 bits
- B. 20,000 bits**
- C. 40,000 bits
- D. 80,000 bits

Answer: B

30. The entire bandwidth is available to a particular station for a particular duration of time.

- A. FDMA
- B. TDMA**
- C. CDMA
- D. CSMA

Answer: B

31. The following access technique is used in 802.3 protocol

- A. CSMA
- B. CSMA/CA
- C. TDMA
- D. CSMA/CD**

Answer: D

32. A block of 128 addresses is granted to a small organization. We know that one of the addresses is 205.16.37.65/25. What is the 6th address in the block?

- A. 205.16.37.5**
- B. 205.16.37.6
- C. 205.16.37.0
- D. 205.16.37.71

Answer: A

33. We know that one of the addresses is 205.16.37.65/23. Find how many addresses are granted to a small organization?

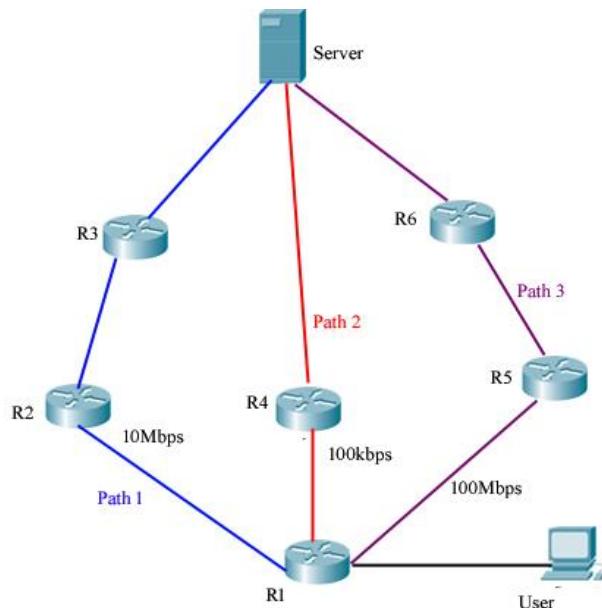
- A. 256
- B. 512**
- C. 1024
- D. 1023

Answer: B

34. As shown in below Figure, Find the best path between the user and server using Routing Information protocol (RIP).

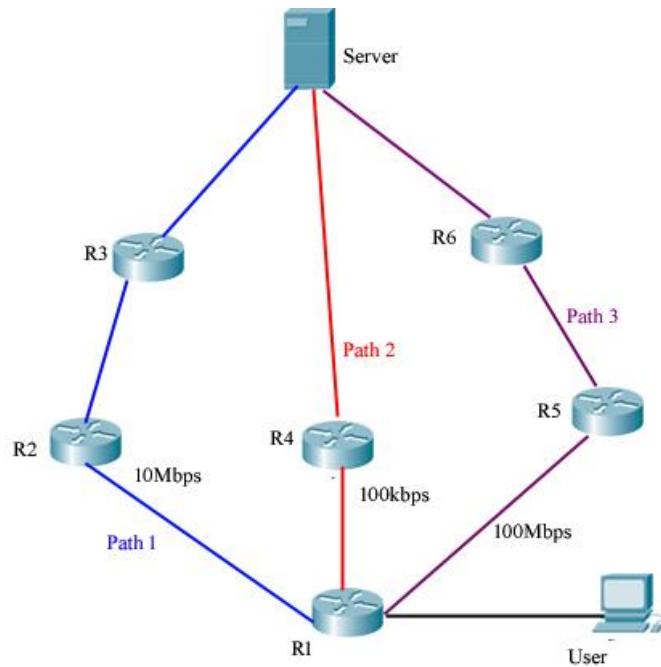
- A. Path 1
- B. Path 2**
- C. Path 3
- D. Path 2 and Path 3

Answer: B



35. In general routing strategy, which path is more appropriate for transmitting the heavy traffic from user to server as shown in Figure.

- A. Path 1
- B. Path 2
- C. Path 3**
- D. Path 1 and Path 2



Answer: C

36. Find the Network ID, if the IP address and subnet mask are 192.168.40.55 and 255.255.248.0 respectively.

- A. **192.168.40.0**
- B. 192.168.32.0
- C. 192.168.8.0
- D. 192.168.248.55

Answer: A

37. Find the class of address 11000001 10000011 00011011 11111111

- A. Class A
- B. Class B
- C. Class C**
- D. Class D

Answer: C

38. PPP is a byte-oriented protocol using byte stuffing with the escape byte _____.

- A. 01111101**

- B. 10111110
- C. 01111110
- D. 10000001

Answer: A

39. is a process-to-process protocol that adds only port addresses, checksum error control, and length information to the data from the upper layer.

- A. TCP
- B. UDP**
- C. IP
- D. ARP

Answer: B

40. In segment header, sequence number and acknowledgement number fields refer to ----

- A. Byte number**
- B. Buffer number
- C. Segment number
- D. None of these

Answer: A

41. A TCP connection is transferring a file of 10000 bytes. The first byte is numbered 20001. What is the sequence number of the segment if all data is sent in only one segment?

- A. 10000
- B. 10001
- C. 20001**
- D. None of these

Answer: C

42. Which is the correct expression for the length of UDP datagram?

- A. UDP length = IP length – IP header's length**
- B. UDP length = UDP length – UDP header's length
- C. UDP length = IP length + IP header's length
- D. UDP length = UDP length + UDP header's length

Answer: A

43. Connection establishment in TCP is called ----- handshaking

- A. Four-way
- B. Two-way
- C. One-way
- D. **None of these**

Answer: D

44. The SYN Flooding Attack in TCP belongs to a group of security attacks known as ---- attack.

- A. Denial of service**
- B. Replay
- C. Man in the Middle
- D. None of these

Answer: A

45. A DNS client is called _____

- A. DNS updater
- B. DNS resolver**
- C. DNS handler
- D. None of these

Answer: B

46. The domain which is used to map an address to a name is called

- A. Country Domain
- B. Main Domain
- C. Inverse Domain**
- D. Generic Domain

Answer: C

47. Both client and server release _____ connection after a page has been transferred.

- A. IP
- B. TCP**
- C. Hyperlink
- D. Network

Answer: B

48. In SMTP, the command to write receiver's mail address is written with the command _____

- A. SEND TO
- B. RCPT TO**

- C. MAIL TO
- D. RCVR TO

Answer: B

49. Which of the following is present in both an HTTP request line and a status line?

- A. **HTTP version number**
- B. URL
- C. Method
- D. None of these

Answer: A

50. A web cookie is a small piece of data that is _____

- A. **sent from a website and stored in user's web browser while a user is browsing a website**
- B. sent from user and stored in the server while a user is browsing a website
- C. sent from root server to all servers
- D. sent from the root server to other root servers

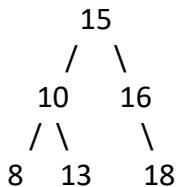
Answer: A

Data Structures and Algorithms

1. If you build a max heap for the sequence 17, 14, 15, 18, 20, 16, 25 and delete the root, what will be the new root?

- a. **20**
- b. 16
- c. 17
- d. 18

2. In the following binary search tree, what will be the inorder successor of 13 ?



- a. 10
- b. 15**
- c. 16
- d. 18

3. If the height of the binary tree is 7, maximum number of internal nodes the tree can have is,

- a. 128
- b. 127**
- c. 64
- d. 63

4. In a binary tree, which of the following is not a valid argument?

- a. It should have at least one node.
- b. 2
- c. 3
- d. 0**

5. If the keys 7 12 17 22 27 32 are to be stored in hash table using a hash function $h(x) = x \bmod 6$, how many collisions will happen?

- a. 0**
- b. 1
- c. 2
- d. 3

6. If the keys 4 8 12 16 18 23 28 32 are to be stored in hash table using hash function $h(x) = x \bmod 7$, the key 18 will go to which of the following slot?

- a. 4
- b. 5
- c. 36**

- d. 28
7. In a stack S 4 8 12 16 are pushed in the same order. Two times pop operation is executed, sum of the returned values is pushed again in stack S. Again two times pop operation is executed and sum of the returned values are pushed in stack S. The current top of the stack S is
- 4
 - 16
 - 28
 - 36**
8. To implement Stacks using Queues, what is the minimum number of queues required?
- 2
 - 3
 - 1**
 - At least 3
9. If you consider the following as number of operations that different algorithms take to complete a particular task on n elements, which one is linear ?
- $3n^3 + 3n + 7$
 - $3n^2 + 3n + 2$
 - $3n + 1$**
 - 8
10. In a circular queue with the capacity of n elements, insertion and deletion are performed using rear and front respectively. Initially rear and front are set to 1. Which of the following condition must be true for the queue to be full.
- front=rear
 - front =rear+1**
 - front=rear-1
 - rear=front +1
11. Consider the following pseudocode for the queue Q
- ```

Function(Q)
If (Q!=empty)
 x=delete(Q)
 Function(Q)
 Insert(Q,x)

```
- What will be the change in a queue ?
- Q element order is reversed**
  - Q is unchanged
  - Q's Front element is removed and inserted at the rear, other elements are unchanged.
  - Q is emptied.
12. Which of the following statement is more suitable while inserting in a circular queue .
- rear= rear +1
  - rear= rear-1
  - rear= (rear+1) mod SIZE**
  - rear=rear mod SIZE +1

13. Which of the following recurrence cannot be solved using a master method?
- a.  $T(n) = 2T(n/4) + n^{0.51}$
  - b.  $T(n) = 64T(n/8) - n^2 \log n$**
  - c.  $T(n) = \sqrt{2}T(n/2) + \log n$
  - d.  $T(n) = 16T(n/4) + n!$
14. The following is the result after first partition of quicksort algorithm, 10 8 6 9 11 14 16  
Which of the following is true?
- a. 11 could be the pivot , 14 could not be pivot.
  - b. 14 could be the pivot , 11 could not be pivot.
  - c. Either 11 or 14 could be pivot element**
  - d. 11 and 14 both are pivot elements.
15. Run time of the recurrence  $T(n)=7T(n/3)+n^2 \log n$ .
- a. Theta( $n^2 \log n$ )**
  - b. Theta ( $n^2$ )
  - c. Theta( $n^2 \log^2 n$ )
  - d. Theta( $n \log^2 n$ )
16. Minimum (Asymptotic) time required to check whether a given binary tree is a binary search tree or not.
- a.  $O(1)$
  - b.  $O(\log n)$
  - c.  $O(n)$**
  - d.  $O(n \log n)$
17. If you keep track of front, rear and count(no. of items in array), in a circular array when front =0 and rear=maxsize-1, what will be the count value.
- a.0
  - b.3
  - c.4
  - d.2**
18. Which of the following data structure can be applied directly on scheduling and resource allocation problems?
- a. stack
  - b. queue**
  - c. tree
  - d. linked list
19. If you are asked to implement stack using queue how many queues are required to represent stack efficiently.
- b. 1
  - c. 2**

d. 3

e. 4

20. Which is something you would NOT use a stack for?

- i. Printing a name in reverse order
  - ii. A function call within another function call
  - iii. Arranging the elements of an array in increasing or decreasing order.
  - iv. Printing the elements of an array in the order they appear within the array.
- a) Only (i)
  - b) (ii) and (iii) are correct
  - c) (iii) and (iv) are correct**
  - d) None of these are correct

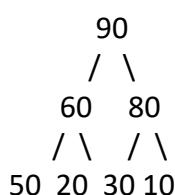
21. Which of the following type of queue is useful in building online multiplayer games.

- a. Simple queue
  - b. Circular queue**
  - c. Priority queue
  - d. Single ended queue
22. In a linked list, there is a pointer to the first node, each node has pointer to the next node and last node has pointer to the first node, the name of the linkedlist is,
- a. Singly linkedlist
  - b. Doubly linkedlist
  - c. Singly circularlinkedlist**
  - d. Doubly circular linkedlist

23. The important element(s) of dynamic programming is,

- a. Optimal substructure
  - b. Overlapping sub problems
  - c. Both a&b**
  - d. None of the given options
24. In a heap, initially where the new node will get inserted?
- a. Root
  - b. Child to root
  - c. Next bottom right**
  - d. anywhere

25. Consider following heap structure.



The array representation is

- a. 10 20 30 50 60 80 90
- b. 90 60 50 20 80 30 10

c. 90 60 80 50 20 30 10

d. 90 80 60 50 30 20 10

26. An array A of integers is given as A: array [1 ... 5] [1 ... 10]; The array is stored in column-major order and the first element of . The array is stored at location 50, Calculate the address of the element A[i][j] where each integer takes one memory location.

(a)  $5i + j + 44$

**(b)  $i + 5j + 44$**

(c)  $5i + j + 39$

(d)  $5j + i + 39$

27. We are given a stack on which two operations are possible, Push( ) and Pop( ). Further, we are given an input sequence 7 5 2 1 3 6, where 7 is the first element and 6 is the last element. Which sequence of elements cannot be printed using the given stack?

A] 6 3 1 2 5 7

**B] 2 1 3 6 7 5**

C] 5 2 7 1 3 6

D] None of above

28. Which of the given options provides the decreasing order of asymptotic complexity of functions f1, f2, f3 and f4?

$f_1=O(n)$ ,  $f_2=O(\log n)$ ,  $f_3=O(n^2)$   $f_4=O(2n)$

A] f1, f2, f3, f4

**B] f2 ,f1,f4,f3**

C] f4,f3,f2,f1

D] None of these

29. Which of the following methods have time complexity  $O(n)$  for a sorted array in descending order, where elements are distinct?

(i) Finding maximum element in the array.

(ii) Finding minimum element in the array.

(iii) Finding the mode of the array.

(iv) Find any element in an array.

A] i alone

**B] ii, iii and iv**

C] ii and iii

D] ii and iv

30. What is the infix version of the following postfix expression?

$x\ 12\ +\ z\ 17\ y\ +\ 42\ * /\ +$

a.  $x + 12 + z / ((17 + y) * 42)$

- b.  $x + 12 + z / 17 + y * 42$
- c.  $x + 12 + z / (17 + y) * 42$
- d.  $x + (12 + z) / (17 + y * 42)$

31. Suppose  $T_1(n) = O(F(n))$  and  $T_2(n) = O(F(n))$ . Which of the following are true?

- (a)  $T_1(n) + T_2(n) = O(F(n))$
- (b)  $T_1(n) * T_2(n) = O(F(n))$
- (c)  $T_1(n) = T_2(n) = O(1)$
- (d)  $T_1(n) = O(T_2(n))$

32. Suppose we are implementing quadratic probing with a hash function  $\text{Hash}(X) = X \bmod 100$ . If an element with key 4594 is inserted and the first three locations attempted are already occupied, then the next cell that will be tried is

- (a) 2
- (b) 3
- (c) 9
- (d) 97
- (e) none of the above

33. In a connected graph with no loops or multiple edges, which of the following inequalities is not correct? ( $v$  is the number of vertices,  $e$  is the number of edges)

- (a)  $e \leq v^2$
- (b)  $e \geq v - 1$
- (c)  $v \leq e^2 + 1$
- (d)  $v \geq e/2$
- (e) All of the above

34. A circular doubly linked list has exactly two nodes, each of whose addresses are stored in two pointer variables, say head and tail. Which among the following statements is NOT True?

- A. Head->next=tail
- B. Head->prev->next=tail
- C. Tail->prev->next=tail
- D. Tail->next->prev=tail

35. We have two stacks, named as A and B. Function Push( &A, data) pushes data on stack A, whereas function Push( &B, data) pushes data on stack B. Pop function on stack A pop out the element from stack A, and pushes it on stack B. On the other hand, Pop function on stack B pops out the element from stack B, and prints it on the screen. Which sequence of character will be printed on the screen after following set of operations: Push( &A, 8 ), Push( &B, 9 ), Push( &A, 4 ), Push( &B, 7 ), Push( &A, 3 ), Pop( &A ), Push( &B, 5 ), Pop( &A ), Pop( &A ), Pop( &B )?

- A] 9 7 3 5 4 8
- B] 8 4 5 3 7 9
- C] 3 4 8 5 7 9
- D] None of these

36. Which of the following will occur after the following set of operations on an empty stack of size 4. Push( 2 ), Push( 3 ), Pop( ), Push( 3 ), Pop( ), Pop( ), Push( 2 ), Pop( ), Pop( ) ?

- A] Stack underflow

- B] Stack overflow
- C] Operations will not lead to any error.
- D] None of above

37. For the two functions  $f(n) = n^2 + 3n + 4$  and  $g(n) = n^3$  we can conclude that,

- a.  $f(n) = O(g(n))$
- b.  $f(n) = \Theta(g(n))$
- c.  $g(n) = O(f(n))$
- d.  $g(n) = \Theta(f(n))$

38. What can you say about the asymptotic growth of the function  $(n) = 3n^2 + 7n - 5$ ?

- a.  $f(n) = \Omega(n^2)$
- b.  $f(n) = O(n^2)$
- c.  $f(n) = \Theta(n^2)$
- d. None of the above

39. How many vertices are there in a complete graph with  $n$  vertices?

- a.  $n*(n-1)/2$
- b.  $n*(n+1)/2$
- c.  $2n$
- d.  $n/2$

40. Consider a 13 element hash table for which  $f(key)=key \bmod 13$  is used with integer keys.

Assuming linear probing is used for collision resolution, at which location would the key 103 be inserted, if the keys 661, 182, 24 and 103 are inserted in that order?

- a. 0
- b. 1
- c. 11
- d. 12

41. What is the value of the sum of the minimum in-degree and maximum out-degree of an Directed Acyclic Graph?

- a. Will always be zero
- b. Depends on a graph
- c. **Will always be greater than zero**

42. Traversal of a graph is different than tree because.

- a. There can be a loop in the graph
- b. DFS on a graph uses stack, while inorder traversal is recursive
- c. **Both A and B**
- d. None of the above

43. A Hash Function ff defined as  $f(key)=key \bmod 7$ . With linear probing while inserting the keys 37,38,72,48,98,11,56 into a table indexed from 0, in which location key 11 will be stored (Count table index 0 as 0th location)?

- a. 3
- b. 4
- c. 5
- d. 6

44. What is the result if total time is bound of in prim's algorithm?

- a. **O(E+V log V)**
- b. O(V log V)
- c. O(E log E)
- d. None of the above

45. Why graph traversal is difficult than tree traversal ?

- a. because tree is binary
- b. because tree is undefined
- c. **Because tree have root**

46. The worst case time complexity of insertion sort is  $O(n^2)$ . What will be the worst case time complexity of insertion sort if the correct position for inserting element is calculated using binary search?

- a.  $O(N \log N)$
- b.  $O(N)$
- c.  **$O(N^2)$**
- d.  $O(1)$

47. Consider the code given below,:

```
void insertionsort(int arr[], int size)
{
 int i, j, value;
 for(i=1; i<size; i++)
 {
 value = arr[i];
 j = i;
 while(...)
 {
 arr[j] = arr[j-1];
 j = j-1;
 }
 arr[j] = value;
 }
}

what is line of code required for while statement to run the insertion sort
a. (j>0) || (arr[j-1]>value)
b. (j>0)&&(arr[j-1]>value)
```

- c.(j>0)&&(arr[j+1]>value)
- d.(j>0)&&(arr[j+1]<value)

48. Consider an array of length 5, arr[5] = {9, 7, 4, 2, 1}. What are the steps of insertions done while running insertion sort on the array?

- a. **7 9 4 2 1 ,4 7 9 2 1 ,2 4 7 9 1, 1 2 4 7 9**
- b. 9 7 4 1 2, 9 7 1 2 4, 9 1 2 4 7 ,1 2 4 7 9
- c. 7 4 2 1 9, 4 2 1 9 7 ,2 1 9 7 4, 1 9 7 4 2
- d. 7 9 4 2 1, 2 4 7 9 1, 4 7 9 2 1 ,1 2 4 7 9

49. A connected planar graph having 6 vertices, 7 edges contains \_\_\_\_\_ regions.

- a.11
- b.15
- c.1
- d.3**

50. When the entries 7, 4, 6, 1, 2, 3, 8, 5 are successively inserted into an initially empty binary search tree, what is the height of the resulting tree?

- a. 4**
- b. 3
- c. 7
- d. 2

## **ECM4098 - COMPREHENSIVE EXAMINATION**

### **Module 5: Microcontroller and Embedded Systems**

Embedded Systems: Characteristics - microcontroller architectures (RISC, CISC)- programming the peripherals of microcontrollers- emerging bus standards – embedded system modelling-operating system -real time concepts.

**Prepared by: Dr. Prakash V, Dr. Balamurugan M S**

1. Which microcontrollers are adopted for designing medium scale embedded systems?

- A) 8-bit
- B) 16-bit to 32-bit
- C) 64-bit
- D) 4-bit

Answer: B

2. Which types of an embedded systems involve the coding at a simple level in an embedded ‘C’, without any necessity of RTOS?

- A) Small Scale Embedded Systems
- B) Medium Scale Embedded Systems
- C) Large Scale Embedded Systems
- D) All of the these

Answer: A

3. The constraints related to the design metrics of an embedded system

- A) Ability to fit on a single chip
- B) Low power consumption
- C) Fast data processing for real-time operations
- D) All of the these

Answer: D

4. Which of the following is not true about embedded system?

- A) Built around specialized hardware
- B) May or may not contain an operating system
- C) Execution behaviour always deterministic
- D) Operate under extreme environmental conditions

Answer: C

5. A missile navigation system is an example of?

- A) Small scale embedded system
- B) Medium scale embedded system
- C) Large scale embedded system
- D) None of the these

Answer: C

6. Which one of the following is valid reason for microcontroller preferred in embedded system?

- A) Large size
- B) High power
- C) More design time
- D) Highly reliable

Answer: D

7. Choose the correct sequence of embedded system design process for top-down approach.

- 1. Requirements
- 2. Components
- 3. Architecture
- 4. Specification
- 5. System integration

- A) 1, 2, 3, 4, 5
- B) 2, 4, 3, 1, 5
- C) 1, 4, 3, 2, 5
- D) 4, 2, 1, 3, 5

Answer: C

8. Which embedded system design life cycle phase perform initial design before the detailed implementation?

- A) Product specification
- B) Hardware & software partitioning
- C) Iteration and implementation
- D) Hardware/software integration

Answer: C

9. Which embedded system design life cycle phase helps to perform debugging and identification errors?

- A) Product specification
- B) HW/SW integration
- C) HW/SW design
- D) Maintenance and upgrade

Answer: B

10. Which embedded system design phase helps to determine whether the system is performing close to its optimal capabilities or not?

- A) Product testing and release
- B) HW/SW integration
- C) HW/SW design
- D) Maintenance and upgrade

Answer: A

11. Choose the correct sequence of embedded system design life cycle.

- 1. Product specification
- 2. Detailed hardware and software design
- 3. Hardware & software partitioning
- 4. Hardware/software integration
- 5. Iteration and implementation
- 6. Product testing and release
- 7. Maintenance and upgrading

- A) 1, 3, 5, 2, 4, 6, 7
- B) 1, 2, 3, 4, 5, 6, 7
- C) 1, 5, 3, 2, 4, 6, 7
- D) 1, 3, 5, 4, 2, 6, 7

Answer: A

12. Embedded systems are used as control systems. What does this mean?

- A) They monitor and control machinery to achieve a result
- B) They control desktops and laptops
- C) They control what happens in any computer system
- D) They have a way of controlling everything

Answer: A

13. Which of the following is the key characteristics of embedded system?

- A) Cost insensitive
- B) No specialized tools required
- C) No power constraints
- D) Fewer system resources

Answer: D

14. The computer architecture which aims at reducing the time of execution of instructions is \_\_\_\_\_

- A) CISC
- B) RISC
- C) ISA
- D) ANNA

Answer: B

15. Which Processor architecture includes multi-clocks?

- A) CISC
- B) RISC
- C) ISA
- D) ANNA

Answer: A

16. Which of the following is true?

- A) The RISC processor has a more complicated design than CISC.
- B) RISC Focus on software
- C) CISC Focus on software
- D) RISC has Variable sized instructions

Answer: B

17. Pipe-lining is a unique feature of \_\_\_\_\_

- A) CISC
- B) RISC
- C) ISA
- D) ANNA

Answer: B

18. Which of the following is true about CISC processor?

- A) Micro programmed control unit is found in CISC.
- B) Data transfer is from memory to memory.
- C) In this instructions are not register based.
- D) All of the these

Answer: D

19. Choose the correct microcontroller classification based on instruction set architecture

- A) CISC & RISC
- B) Von-Neumann & Harvard
- C) Volatile & Non-volatile
- D) Internal & External

Answer: A

20. Based on how microcontroller gets its CPU arrangement with the ROM and RAM, it can be classified as \_\_\_\_\_ & \_\_\_\_\_ architecture.

- A) CISC & RISC
- B) Von-Neumann & Harvard
- C) Volatile & Non-volatile
- D) Internal & External

Answer: B

21. Choose the correct option based on True/False condition of following statements on RISC instruction set architecture

- 1) RISC is a micro programming unit
  - 2) In RISC, number of instruction is more
  - 3) Instruction decoding is simple in RISC
  - 4) RISC support highly pipelined instruction execution
- A) 1)- True, 2)-True, 3)-False, 4)-False
  - B) 1)-True, 2)-False, 3)-False, 4)-True
  - C) 1)-True, 2)-False, 3)-True, 4)-False
  - D) 1)-False, 2)-False, 3)-True, 4)-True

Answer: D

22. The CISC stands for

- A) Computer Instruction Set Compliment
- B) Complete Instruction Set Compliment
- C) Computer Indexed Set Components
- D) Complex Instruction set computer

Answer: D

23. What is the full form of RISC?

- A) Read Instruction Set Architecture
- B) Reduced Instruction Set Computer.
- C) Register Instruction Set Computer.
- D) Reduced Interrupt Service Computer

Answer: B

24. Which of the following is/are invalid digital pin configuration in Arduino Uno?

- A) INPUT
- B) OUTPUT
- C) INPUT\_PULLUP
- D) INOUT

Answer: D

25. What is the output of the following Arduino sketch

```
void setup() {
 Serial.begin(9600);
}
void loop() {
 Serial.write(40);
}
```

- A) Send a signal to pin 40 on the Arduino board
- B) Send an octal number of 40 through the Serial pins
- C) Send a byte with value 40 through the Serial pins
- D) Send a hexadecimal number of 40 through the Serial pins

Answer: C

26. In Arduino, sketch Which of the following statement is used to configure digital pin 7 as output pin and glow a LED connected to it.

- A) pinMode(7, OUTPUT); digitalWrite(7, HIGH);
- B) PinMode(7, OUTPUT); DigitalWrite(7, HIGH);
- C) Pinmode(7, OUTPUT); Digitalwrite(7, HIGH);
- D) pinmode(7, OUTPUT); digitalWrite(ledPin, LOW);

Answer: A

27. Which of the following statement is valid to generate a delay of 2 seconds in Arduino?

- A) delay(2000);
- B) delayMicroseconds(2000);
- C) millis(2000);
- D) elay(2);

Answer: A

28. What is the output of the program given below if a voltage of 5V is supplied to the pin corresponding to the A0 pin on an Arduino UNO?

```
void setup() {
 Serial.begin(9600);
 pinMode(A0, INPUT);
}
void loop() {
 int s = analogRead(A0);
 Serial.println(s);
}
```

- A) 0
- B) 1024

- C) 512
- D) 5

Answer: B

29. Which of the following digital pin(s) is a valid PWM pin in Arduino Uno?

- A) 3
- B) 4
- C) 7
- D) 12

Answer: A

30. What is the header file used for interfacing LCD in Arduino Uno?

- A) LCD.h
- B) TextLCD.h
- C) LiquidCrystal.h
- D) All of them

Answer: C

31. Which of the following statement is valid with respect to function analogRead(pin) of Arduino Uno analog pin?

- A) Only works on analog pins A0-A5
- B) Need to declare as INPUT
- C) Return a value between 0 to 255
- D) Reads ADC value for every 100 milliseconds

Answer: A

32. Which of the following statement is used to configure digital pin 13 as output pin and read the status of the switch connected on Arduino Uno.

- A) pinMode(13, INPUT); digitalWrite(13);
- B) pinMode(13, HIGH); digitalWrite(13);
- C) pinMode(13, LOW); digitalWrite(13);
- D) pinMode(13, OUTPUT); digitalWrite(13);

Answer: A

33. Number of digital I/O pins in Arduino Uno is?

- A) 14
- B) 10
- C) 6
- D) 4

Answer: A

34. Which of the following options of LED segments (by letter) are combined to display a digit 3 in a common cathode 7-segment display?

- A) A, B, C, D and G set to HIGH & F, E and DP set to LOW
- B) A, B, C, D and G set to LOW & F, E and DP set to HIGH
- C) A, B, F, E and G set to LOW & C, D and DP set to HIGH
- D) A, B, F, E and G set to HIGH & C, D and DP set to LOW

Answer: A

35. Assume an 8-bit ADC operated with 5V as a reference voltage then, what will be the range of digital output value of the ADC?

- A) 0 - 255
- B) 0 - 7
- C) 0 – 5
- D) 0 – 1024

Answer: A

36. Which signal is used to select the slave in the serial peripheral interfacing (SPI) protocol?

- A) slave select
- B) master select
- C) interrupt
- D) clock signal

Answer: A

37. Which are the two lines used in the I2C protocol?

- A) SDA and SPDR
- B) SPDR and SCL
- C) SDA and SCL
- D) SCL and CS

Answer: C

38. What does UART stand for?

- A) universal asynchronous receiver transmitter
- B) unique asynchronous receiver transmitter
- C) universal address receiver transmitter
- D) unique address receiver transmitter

Answer: A

39. In I2C protocol data packet transmission is initiated and terminated by? -----

- A) Master SCL
- B) Master SDA
- C) Slave SCL
- D) Slave SDA

Answer: B

40. USB device are connected using -----structure

- A) Star
- B) Tree
- C) List
- D) Ring

Answer: A

41. Which protocol does not have error detection or acknowledgement mechanism?

- A) UART
- B) SPI
- C) I2C
- D) CAN

Answer: B

42. In the CAN arbitration which of the following are true

- 1) Arbitration – needed when multiple nodes try to transmit at the same time
  - 2) More than one transmitter is allowed to transmit at a time based on the need
  - 3) A node waits for bus to become idle
  - 4) Nodes with more important messages continue transmitting
- A) 1,2,3,4  
B) 2,3,4  
C) 1,3  
D) 1,3,4

Answer: B

43. Serial Peripheral Interface protocol is

- A) Single Master Multi Slave
- B) Multi Master Single Slave
- C) Multi Master Multi Slave
- D) Single Master Single Slave

Answer: A

44. Which of the following IEEE standard follows Zigbee software stack?

- A) IEEE 802.11
- B) IEEE 802.15.4
- C) IEEE 802.11.1
- D) IEEE 802.11.2

Answer: B

45. Bluetooth transceiver devices operate in \_\_\_\_\_ band.

- A) 2.4 GHz ISM
- B) 2.5 GHz ISM
- C) 2.6 GHz ISM
- D) 2.7 GHz ISM

Answer: A

46. The transfer rate, when the USB is operating in low-speed of operation is \_\_\_\_\_

- A) 5 Mb/s
- B) 12 Mb/s
- C) 2.5 Mb/s
- D) 1.5 Mb/s

Answer: D

47. The devices connected to USB is assigned a \_\_\_\_\_ address.

- A) 9 bit
- B) 16 bit
- C) 4 bit
- D) 7 bit

Answer: D

48. What can UML interfaces be used for?

- A) To provide concrete classes with the stereotype "interface"
- B) To program in Java and C++, but not in C#
- C) To define executable logic that can be reused in several classes
- D) To specify required services for types of objects

Answer: D

49. Key elements of UML use-case diagrams are

- A) People, computer
- B) Actors, use cases
- C) People, classes and objects
- D) Uses, cases

Answer: B

50. In UML class diagram, inside each class what is to be printed?

- A) Its name, attributes, operations and derived class
- B) Its name, attributes and operations
- C) Its name and attributes
- D) Its name and operations

Answer: A

51. Choose the appropriate UML diagram to explain the time-oriented operations at finite time instance.

- A) Class diagram
- B) Sequence diagram
- C) Component diagram
- D) Use case diagram

Answer: B

52. Which of the following diagram is used for describing and analysing concurrent process.

- A) Petrinet model
- B) UML Use case
- C) UML Class
- D) UML Sequence

Answer: B

53. Which of the following UML diagram(s) describes static structure of a system?

- A) Sequence diagram
- B) Object diagram
- C) Use case diagram
- D) Activity diagram

Answer: B

54. In UML how are object interconnections modelled as relationships

- A) Dependencies
- B) Generalizations
- C) Associations
- D) All of the these

Answer: D

55. Collaboration diagram, activity diagram, interaction diagram and use case diagram are considered as type of

- A) Non-behavioural diagram
- B) Non structural diagram
- C) Structural diagram
- D) Behavioural diagram

Answer: D

56. Which feature distinguishes a Petri net from a standard network?

- A) The presence of tokens and transitions
- B) Relative independence on parameter values
- C) Initial conditions
- D) All of the these

Answer: A

57. The inheritance relationship is used in which UML diagram

- A) Use case
- B) Class
- C) Activity
- D) Sequence

Answer: A

58. Which is the valid visibilities that attribute can have in class diagram?

- A) Public
- B) Global
- C) Actors
- D) States

Answer: A

59. Which diagram is used to understand the reaction of objects on receiving external stimuli?

- A) Component diagram
- B) State diagram
- C) Use case diagram
- D) Class diagram

Answer: B

60. Average time for a particular task is constrained as well as is number of instances when some maximum time is exceeded, stated approach is known as

- A) Hard real-time systems
- B) Real-data constraints
- C) Real-time constraints
- D) Soft real-time systems

Answer: D

61. To access the services of operating system, the interface is provided by the

- A) System calls
- B) API
- C) Library
- D) Assembly instructions

Answer: A

62. Which one of the following is not true?

- A) kernel is the program that constitutes the central core of the operating system
- B) kernel is the first part of operating system to load into memory during booting
- C) kernel is made of various modules which cannot be loaded in running operating system
- D) kernel remains in the memory during the entire computer session

Answer: C

63. If a process fails, most operating system write the error information to a \_\_\_\_\_

- A) log file
- B) another running process
- C) new file
- D) none of the mentioned

Answer: A

64. Which one of the following is not an example for real time operating system?

- A) VxWorks
- B) Windows CE
- C) RTLinux
- D) Palm OS

Answer: D

65. Which of the following is not a state of a process in OS?

- A) New
- B) Old
- C) Waiting
- D) Running

Answer: B

66. In an OS, if a process is executing in its critical section, then no other processes can be executing in their critical section. This condition is called

- A) mutual exclusion
- B) critical exclusion
- C) synchronous exclusion
- D) asynchronous exclusion

Answer: A

67. When high priority task is indirectly pre-empted by medium priority task effectively inverting the relative priority of the two tasks, the scenario is called

- A) priority inversion
- B) priority ceiling
- C) priority exchange
- D) priority modification

Answer: A

68. What is the critical section?

- A) It is the part of the process which is being executed for so long
- B) It is the part of the thread which is going to be terminated
- C) It is the part of the program where shared resources are accessed by the process
- D) It is the part of the program where different processes are shared

Answer: C

69. In rate monotonic scheduling

- A) shorter duration job has higher priority
- B) longer duration job has higher priority
- C) priority does not depend on the duration of the job
- D) based on first arrival for execution

Answer: A

70. Which of the following statements are true?

- I. Shortest remaining time first scheduling may cause starvation
  - II. Preemptive scheduling may cause starvation
  - III. Round robin is better than FCFS in terms of response time
- 
- A) I only
  - B) I and III only
  - C) II and III only
  - D) I, II and III

Answer: D

71. In which type of kernel does the entire operating system run as a single program?

- A) Monolithic kernel
- B) Microkernel kernels
- C) Hybrid Kernels
- D) Nano Kernels

Answer: A

72. Context switching is the process of

- A) Process by which a process is temporarily swapped (moved) from the main memory (RAM) to the secondary memory (Disk)
- B) The process of saving the context of a task being suspended and restoring the context of a task being resumed
- C) Context Switching is the mechanism that allows multiple processes to use a multiple CPU
- D) Context Switching stores the status of the ongoing process so that the process can be reloaded from the starting of execution of task

Answer: B

73. In OS, Pre-emptive kernel is

- A) Allows the currently executing task to stop its execution and provides the processor for the new task
- B) Permits the currently executing task to complete its execution and provides the processor for new task
- C) Doesn't permit the new task to run its execution
- D) Permits the new task to totally remove the execution of current task from the processing

Answer: A

74. Choose the incorrect statement with respect to process and threads concept?

- A) Processes are dependent hence they share memory.
- B) Processes require more time for context switching than thread
- C) If a process gets blocked, remaining processes can continue execution.
- D) Processes require more resources than threads.

Answer: A

75. The problem of priority inversion can be solved by \_\_\_\_\_

- A) priority inheritance protocol only
- B) priority ceiling protocol only
- C) both priority inheritance and priority ceiling protocol
- D) none of the mentioned

Answer: C

1. The instruction, Add #91,R1 does \_\_\_\_\_
  - a) Adds the value of 91 to the address of R1 and stores 91 in that address
  - b) Adds 91 to the value of R1 and stores it in R1**
  - c) Finds the memory location 91 and adds that content to that of R1
  - d) None of the mentioned
  
2. In the case of zero-address instruction method, the operands are stored in \_\_\_\_\_
  - a) Registers
  - b) Accumulators
  - c) Push down stack**
  - d) Cache
  
3. Add #34, when this instruction is executed, the following happen/s \_\_\_\_\_
  - a) The processor raises an error and requests for one more operand
  - b) The value stored in memory location 34 is retrieved and one more operand is requested**
  - c) The value 34 gets added to the value on the stack and is pushed onto the stack
  - d) None of the mentioned
  
4. The addressing mode which makes use of in-direction pointers is \_\_\_\_\_
  - a) Indirect addressing mode**
  - b) Index addressing mode
  - c) Relative addressing mode
  - d) Offset addressing mode
  
5. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is \_\_\_\_\_
  - a) EA = 5+R1
  - b) EA = R1
  - c) EA = [R1]
  - d) EA = 5+[R1]**

6. The addressing mode/s, which uses the PC instead of a general purpose register is \_\_\_\_\_

- a) Indexed with offset
- b) Relative**
- c) Direct
- d) Both Indexed with offset and direct

7. When we use auto increment or auto decrement, which of the following is/are true?

- 1) In both, the address is used to retrieve the operand and then the address gets altered
- 2) In auto increment, the operand is retrieved first and then the address altered
- 3) Both of them can be used on general purpose registers as well as memory locations
- a) 1, 2, 3
- b) 2
- c) 1, 3
- d) 2, 3**

8. The addressing mode, where you directly specify the operand value is \_\_\_\_\_

- a) Immediate**
- b) Direct
- c) Definite
- d) Relative

9. The effective address of the following instruction is MUL 5(R1,R2).

- a)  $5+R1+R2$
- b)  $5+(R1*R2)$
- c)  $5+[R1]+[R2]$**
- d)  $5*([R1]+[R2])$

.

10. \_\_\_\_\_ addressing mode is most suitable to change the normal sequence of execution of instructions.

- a)** Relative
- b) Indirect
- c) Index with Offset
- d) Immediate

11. During the execution of the instructions, a copy of the instructions is placed in the \_\_\_\_\_

- a) Register
- b) RAM
- c) System heap
- d)** Cache

12. Two processors A and B have clock frequencies of 700 MHz and 900 MHz respectively.

Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

- a)** A
- b) B
- c) Both take the same time
- d) Insufficient information

13. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_

- a) Super-scaling
- b)** Pipe-lining
- c) Parallel Computation
- d) None of the mentioned

14. When performing a looping operation, the instruction gets stored in the \_\_\_\_\_

- a) Registers
- b) Cache**
- c) System Heap
- d) System stack

15. If a processor clock is rated as 1250 million cycles per second, then its clock period is \_\_\_\_\_

- a)  $1.9 * 10^{-10}$  sec
- b)  $1.6 * 10^{-9}$  sec
- c)  $1.25 * 10^{-10}$  sec
- d)  $8 * 10^{-10}$  sec**

16. If the instruction, Add R1, R2, R3 is executed in a system that is pipe-lined, then the value of S is (Where S is a term of the Basic performance equation)?

- a) 3
- b) ~2
- c) ~1**
- d) 6

17. The main virtue for using single Bus structure is \_\_\_\_\_

- a) Fast data transfers
- b) Cost effective connectivity and speed
- c) Cost effective connectivity and ease of attaching peripheral devices**
- d) None of the mentioned

18. \_\_\_\_\_ register Connected to the Processor bus is a single-way transfer capable.

- a) PC
- b) IR
- c) Temp
- d) Z**

19. The main advantage of multiple bus organization over a single bus is \_\_\_\_\_

- a) Reduction in the number of cycles for execution
- b) Increase in size of the registers
- c) Better Connectivity
- d) None of the mentioned

20. Which registers can interact with the secondary storage?

- a) MAR
- b) PC
- c) IR
- d) R0

21. During the execution of a program which gets initialized first?

- a) MDR
- b) IR
- c) PC
- d) MAR

22. The registers, ALU and the interconnection between them are collectively called as \_\_\_\_\_

- a) process route
- b) information trail
- c) information path
- d) data path

23. Which method/s of representation of numbers occupies a large amount of memory than others?

- a) Sign-magnitude
- b) 1's complement
- c) 2's complement
- d) 1's & 2's compliment

24. When we perform subtraction on -7 and 1 the answer in 2's complement form is \_\_\_\_\_

- a) 1010
- b) 1110
- c) 0110
- d) 1000**

25. When 1101 is used to divide 100010010 the remainder is \_\_\_\_\_

- a) 101
- b) 11
- c) 0
- d) 1**

26. In memory mapped I/O the number of devices that can be connected to share the same memory is

- a) 1 device b) 2 devices **c) N devices** d) N-1 devices

27. Which register contains the relevant information about the operation of the I/O devices

- a) Data register **b) Status register** c) Memory unit. D) Extra register

28. When I/O devices and memory share the same address space, it is called \_\_\_\_\_.

- a. memory shared I/O** b) DMA controlled c) Interrupt controlled I/O d)  
**memorymapped**

29. How many pins are usually present in a serial port?

- a) 9** b) 32 c) 64 d) 27

30. Which of the following flag must be set to enable the display to display the data?

- a. Status flag **b) Keyboard enable** c) Display enable d) I/O enable

31. Printers, hard drives and CD drives use \_\_\_\_\_ ports

- a. Serial Ports **b) PCI** c) Parallel ports d) SCSI ports

32. Bluetooth port has
- a. Incoming ports b) Outgoing ports **c) Both a) and b)** d) None
33. Parallel ports send data bit by bit at a time.
- a. True **b) False** c) Maybe d) Irrelevant choices
34. Wireless ports that transmit data between two devices placed close to each other are called\_\_\_\_\_.
- a. FireWire b) USB **c) Infrared** d) SCSI ports
35. In dynamic parallel processing, which module of the CPU decides which instructions are to be run in parallel?
- a) Processor** b) ALU c) Load/Store unit d) compiler
36. What are the types of dependences that arise while executing ILP?
- a) Data b) Name c) Control **d) All of the above**
37. When a CPU implements ILP within a single processor, it is called
- a) Multi-scalar processors b) single processor **c) Super scalar processor** d) multi-processor
38. In super scalar processors
- a) Two instructions are sent from the instruction queue to the dispatch unit
  - b) Multiple instructions are sent from the instruction queue to dispatch unit
  - c) Single instruction is sent from the instruction fetch unit to the instruction queue
  - d) Multiple instructions are sent from the instruction fetch unit to the instruction queue**

39. Consider the computation of the equation  $y = a1.x1+a2.x2+a3.x3$ . Consider that you are using a VLIW processor where there are 2 load/store units, 1 multiply unit and 1 add unit. Calculate how many cycles are required to arrive at the final result  $y$ .

- a) 12
- b) 14
- c) 6
- d) 5**

40. In VLIW processors, the instruction scheduling is done

- a) Statistically by compiler**
- b) Dynamically by processor at runtime**
- c) Both a) and b)**
- d) None of the above**

41. The order in which the instructions are carried out in a pipelined architecture is

- a) instruction fetch, operand fetch, instruction decode, instruction execution and operand store
- b) instruction fetch, instruction decode, operand fetch, instruction execution and operand store**
- c) instruction fetch, instruction execution, instruction decode, operand fetch, and operand store
- d) instruction fetch, instruction decode, instruction execution, operand fetch, and operand store

42. Which of the following is a type of pipelining

- a) arithmetic pipelining b) instruction pipelining c) processor pipelining d) **All of the above**

43. When many processors are connected together to execute instructions in parallel, it is called

- a) Processor level parallelism**
- b) Instruction level parallelism
- c) Both a) and b)
- d) None

44. When an array of processors is attached as an add-on to a general purpose computer, it is called

- a) Multi-processors
- b) VLIW processors
- c) Attached array computers**
- d) SIMD array computers

45. Which of the following statements about the SIMD processors is true?

- a) Each processor has ALU and Register
- b) The processors are arranged in an array fashion and execute instructions in parallel
- c) The master control unit takes care of all the control signals
- d) All of the above**

46. When only one instruction is executed in a single clock cycle, it is called

- a) MIMD processors b) MISD processors **c) SISD processors** d) SIMD processors

47. Which of the following does not come under parallel processing?

- a) SISD processors** b) SIMD processors c) MIMD processors d) MISD processors

48. A multiprocessor system can have which of the following memory organizations?

- a) Shared memory b) Distributed memory **c) Both a) and b)** d) Single unshared memory

49. When each processor can have access to the local memory of any other processor, it is called

- a) Distributed memory **b) Distributed shared memory** c) Shared memory d) Virtual memory.

50. The protocol that supports write-back caches is

- a) Memory protocol b) Distributed protocol c) MSI protocol **d) MESI protocol.**

## Comprehensive QB Bank

**Course : Linear Integrated Circuits, No.of Questions: 50**

**Faculty Name : Dr. Ashis Tripathy & Dr. Dr. Girija Shankar Sahoo**

1. The two input terminals of an operational amplifier are called
  - (a) differential and non-differential (b) **inverting and non-inverting**
  - (c) positive and negative (d) high and low
2. A differential amplifier has
  - (a) four inputs (b) three inputs (c) **two inputs** (d) one input
3. n OP-AMP circuit uses a feedback, which is called
  - (a) open loop (b) **inverting feedback**
  - (c) closed loop (d) non- inverting feedback
4. A differential amplifier has
  - (a) common-collector transistor (b) **an emitter follower**
  - (c) common-base transistor (d) an OP-AMP
5. A differential amplifier is used in OP-AMP circuits due to
  - (a) **high input impedance** (b) low input impedance
  - (c) high output impedance (d) low output impedance
6. Differential amplifiers are commonly used in
  - (a) **instrumentation amplifiers** (b) buffers
  - (c) summing amplifier (d) zero-crossing-detectors
7. The common-mode signal VC is applied to
  - (a) the inverting input terminal (b) the non-inverting input terminal
  - (c) **both the input terminals** (d) all of the above
8. When the two input terminals of a difference amplifier are grounded

- (a) the dc output voltage is zero (b) the ac output voltage is zero  
(c) the output offset voltage exist (d) none of these

9. The CMRR of a difference amplifier is

- (a)  $CMRR=20 \log (Ad/Ac)$  (b)  $CMRR=20 \log (AC/Ad)$  (c)  $CMRR=40 \log (AC/Ad)$  (d)  
 $CMRR=40 \log (Ad/Ac)$

10. The input offset current of a difference amplifier is

- (a) the difference of the two base currents (b) average of the two collector currents  
(c) the average of the two base currents (d) difference of the two collector currents

11. The input stage and second stage of an OP-AMP are

- (a) differential amplifiers (b) CE amplifier  
(c) common collector amplifier (d) power amplifier

12. An operational amplifier IC is an

- (a) analog IC (b) digital IC  
(c) hybrid IC (d) digital as well as analog IC

13. In an ideal operational amplifier IC, the transistors are

- (a) matched (b) different characters  
(c) unmatched (d) none of these

14. The last stage of an operational amplifier is the

- (a) output driver (b) differential amplifier  
(c) buffer (d) level shifter

15. The rise time and overshoot of an operational amplifier are

- (a) 0.3 ns and 6% (b) 0.3 ms and 6% (c) 0.3 ps and 2% (d) 0.3 ps and 6%

16. An ideal OP-AMP has

- (a) infinite input impedance (b) zero output impedance  
(c) infinite voltage gain (d) All of these

17. The number of pins of the IC741 OP-AMP is

- (a) 8 (b) 10 (c) 12 (d) 14

18. The short-circuit output current of IC741 is

- (a) 25 A (b) 25 mA (c) 25 pA (d) 25 nA

19. The maximum rate of change of output voltage per unit time is

- (a) slew rate (b) CMRR
- (c) offset voltage (d) supply-voltage rejection ratio

20. The input offset voltage in an OPAMP is due to

- (a) mismatch in transistor parameters (b) voltage irregularity
- (c) imperfect ground (d) None of these

21. Commercially available OPAMP is

- (a) IC 742 (b) IC 723 (c) IC 741 (d) IC 555

22. The CMRR of an OPAMP is

- (a) much larger than unity (b) zero
- (c) much smaller than unity (d) unity

23. The CMRR of an OPAMP is

- (a) Impedance dependent (b) Voltage dependent
- (c) Frequency dependent (d) Independent of these

24. A differential amplifier has the differential gain of 100. If its CMRR = 240, then the common mode gain is

- (a) 0.24 (b) 0.417 (c) 24000 (d) 1

25. The linear application of an operational amplifier is

- (a) adder circuit (b) log amplifier
- (c) antilog amplifier (d) schmitt trigger

26. The non-linear application of an operational amplifier is

- (a) adder circuit (b) **comparator**
- (c) subtractor circuit (d) voltage-to-current converter

27. An astable multivibrator has

- (a) One stable state (c) One quasi-stable state
- (b) Two stable state (d) **Two quasi-stable state**

28. An monostable multivibrator has

- (a) **One stable state** (c) One quasi-stable state
  - (b) Two stable state (d) Two quasi-stable state
29. An bistable multivibrator has
- (a) One stable state (c) One quasi-stable state
  - (b) **Two stable state** (d) Two quasi-stable state

30. If an multivibrator has one stable and one quasi-stable, the circuit is called as

- (a) Astable multivibrator (c) Bi-stable multivibrator
- (b) **Monostable multivibrator** (d) None of these

31. Pulse stretches is the alternative name of

- (a) **Monostable multivibrator** (c) 555 timer
- (b) Flip-flop (d) Schmitt-trigger

32. A 555 timer consists of

- (a) **Two comparator, one flip-flop and one transistor**
- (b) Only operational amplifiers
- (c) One comparator, one flip-flop
- (d) None of these

33. Which multivibrator can able to convert 10ms pulse into a 10ms pulse?

- (a) Astable multivibrator (c) Bi-stable multivibrator
- (b) **Monostable multivibrator** (d) None of these

34. A 556 timer IC consists of

- (a) Two 555 timer (b) Three 555 timer
- (c) Four 555 timer (d) None of these

35. A monostable multivibrator consists of

- (a) Operational amplifiers (c) 555 timer
- (b) Logic gates (d) All of these

36. A Schmitt trigger circuit is a

- (a) Monostable multivibrator (c) Free-running multivibrators
- (b) Bi-stable multivibrator (d) None of these

37. If RESET pin of 555IC is made low, then

- (a) output is high (b) output is low
- (c) IC will not work (d) IC may be damaged

38. Multivibrators

- (a) generate square wave (b) convert sine to square wave
- (c) convert triangular to sine wave (d) convert triangular to square wave

39. Non-linearity in the output of converter is expressed in

- a) None of the mentioned
- b) Percentage of reference voltage
- c) Percentage of resolution
- d) Percentage of full scale voltage

40. A binary input 000 is fed to a 3bit DAC/ADC. The resultant output is 101. Find the type of error?

- a) Settling error
- b) Gain error
- c) Offset error

d) Linearity error

41. A monotonic DAC is one whose analog output increases for

- a) Decreases in digital input
- b) An increases in analog input
- c) An increases in digital input

d) Decreases in analog input

42. All the commercially available DAC are

- a) Monotonic
- b) Non-monotonic
- c) Either monotonic or non-monotonic
- d) None of the mentioned

43. Pick out the incorrect statement “In a 3 bit weighted resistor DAC”

- a) Although the op-amp is connected in inverting mode, it can also be connected in non-inverting mode
- b) The op-amp simply work as a current to voltage converter
- c) The polarity of the reference voltage is chosen in accordance with the input voltage
- d) None of the mentioned

44. What is the disadvantage of binary weighted type DAC?

- a) Require wide range of resistors
- b) High operating frequency
- c) High power consumption
- d) Slow switching

45. How to overcome the limitation of binary weighted resistor type DAC?

- a) Using R-2R ladder type DAC
- b) Multiplying DACs

c) Using monolithic DAC

d) Using hybrid DAC

46. How a triangular wave generator is derived from square wave generator?

a) Connect oscillator at the output

b) Connect Voltage follower at the output

c) Connect differential at the output

d) **Connect integrator at the output**

47. The increase in the frequency of triangular wave generator.

a) **Ramp the amplitude of triangular wave**

b) Increase the amplitude of triangular wave

c) Decrease the amplitude of triangular wave

d) None of the mentioned

48. Which among the following op-amp is chosen for generating triangular wave of relatively higher frequency?

a) LM741 op-amp

b) **LM301 op-amp**

c) LM1458 op-amp

d) LM3530 op-amp

49. Triangular wave form has

a) Rise time < fall time

b) **Rise time = fall time**

c) Rise time  $\geq$  fall time

d) None of the mentioned

50. Output of an integrator producing waveforms of unequal rise and fall time are called

a) Triangular waveform

b) Sawtooth waveform

c) Pulsating waveform

d) Spiked waveform

## **Operating Systems**

1. Process 1 and Process 2 are executing at the same time.

Let the value of counter be 3.

Process 1:

```
register1 = counter
register1 = register1 + 1
counter = register1
```

Process 2:

```
register2 = counter
register2 = register2 - 1
counter = register2
```

What is the value of the counter after the execution of Process 1 and Process 2?

- a) 4, 2
- b) 3, 3
- c) 4, 3
- d) 3, 2

**Answer: a**

2. The value of the *pid* for the child process is

- a) 1
- b) 0
- c) >1
- d) <0

**Answer: b**

3. An Operating System is an interface between the hardware and \_\_\_\_\_

- a) Interrupt
- b) Kernel
- c) Network
- d) Computer User

**Answer: d**

4. \_\_\_\_\_ are associated with the operating system but are not part of the kernel

- a) System Program
- b) Application Program
- c) Interrupt
- d) Control Program

**Answer: a**

5. \_\_\_\_\_ are not associated with the operation of the system

- a) System Program
- b) Application Program
- c) Interrupt
- d) Control Program

**Answer: b**

6. \_\_\_\_\_ is a feature for scheduling and multi-programming to provide an economical interactive system of two or more users.

- a) Time Sharing
- b) Multi-tasking
- c) Time tracing
- d) None

**Answer: a**

7. The simultaneous processing of two or more programs by multiple processors, is \_\_\_\_\_

- a) Time Sharing
- b) Multi-processing
- c) Time tracing
- d) All of the above

**Answer: b**

8. Server-Site Operating System are also known as \_\_\_\_\_

- a) Single User Operating System
- b) Network Operating System
- c) Multi-Tasking Operating System
- d) Batch Processing Operating System

**Answer: b**

9. \_\_\_\_\_ specifies the range of the memory address

- a) base
- b) limit
- c) base+limit
- d) limit-base

**Answer: c**

10. \_\_\_\_\_ register holds the smallest legal physical address

- a) base
- b) limit
- c) base+limit
- d) relocation

**Answer: a**

11. \_\_\_\_\_ code can be generated when the compile time of a process in memory is known

- a) binding
- b) absolute
- c) relocatable
- d) locatable

**Answer: b**

12. \_\_\_\_\_ code can be generated when the compile time of a process in memory is not known

- a) binding
- b) absolute
- c) relocatable
- d) locatable

**Answer: c**

13. When the CPU scheduler selects a process for execution, the dispatcher loads the relocation and \_\_\_\_\_ registers with the correct values as part of the context switch

- a) base
- b) limit
- c) base+limit
- d) none

**Answer: c**

14. \_\_\_\_\_ strategy produces largest leftover holes

- a) best fit
- b) worst fit
- c) first fit
- d) none

**Answer: b**

15. \_\_\_\_\_ strategy produces smallest leftover holes

- a) best fit
- b) worst fit
- c) first fit
- d) none

**Answer: a**

16. In \_\_\_\_\_ strategy, we stop searching as soon as we find a free hole that is large enough

- a) best fit
- b) worst fit
- c) first fit
- d) none

**Answer: c**

17. The \_\_\_\_\_ strategy suffers from external fragmentation

- a) best fit and first fit
- b) best fit
- c) first fit
- d) best fit or first fit

**Answer: a**

18. \_\_\_\_\_ permits a process's physical address space to be noncontiguous to avoid external fragmentation

- a) paging
- b) best fit
- c) first fit
- d) best fit or first fit

**Answer: a**

19. Breaking logical memory into blocks of the fixed size is called frames

- a. True
- b. False

**Answer: b**

20. Breaking physical memory into blocks of the fixed size is called frames
- a. True
  - b. False

**Answer: a**

21. The \_\_\_ table has one entry for each physical page frame, indicating whether the latter is free or allocated and, if it is allocated, to which page of which process
- a. Page Table
  - b. Frame Table
  - c. Free Frame List
  - d. None

**Answer: b**

22. Every entry in the TLB has a \_\_\_\_ and a value
- a. key
  - b. Tag
  - c. Key or Tag
  - d. None

**Answer: c**

23. If the page number is not in the TLB, its a \_\_\_\_
- a. Hit
  - b. Miss
  - c. Wired Down
  - d. Kernel Code

**Answer: b**

24. If the page number in the TLB cannot be removed, its a \_\_\_\_
- a. Hit
  - b. Miss
  - c. Wired Down
  - d. Kernal Code

**Answer: c**

25. When the bit is set to invalid, the page is found in the process's logical address space.

- a. True
- b. false

**Answer: b**

26. When the bit is set to valid, the page is found in the process's logical address space.

- a. True
- b. false

**Answer: a**

27. The pages are loaded only when they are needed is called as \_\_\_\_\_

- a. paging
- b. demand paging
- c. framing
- d. None

**Answer: b**

28. A page fault occurs when the page is marked with invalid bit.

- a. True
- b. False

**Answer: a**

29. Effective access time is indirectly proportional to the page fault rate.

- a. True
- b. False

**Answer: b**

30. Identify the Time quantum depended algorithm.

- a. multilevel queue scheduling algorithm
- b. priority disk scheduling algorithm
- c. round robin scheduling algorithm
- d. shortest job scheduling algorithm

**Answer: c**

31. Identify the deadlock avoidance algorithm?
- a. Priority scheduling algorithm
  - b. Resource allocation graph
  - c. Bankers algorithm
  - d. Bankers algorithm and Resource allocation graph

**Answer: c**

32. When a process is continuously deprived of required resources, it is known as
- a. aging
  - b. deadlock
  - c. starvation
  - d. dead lock prevention

**Answer: c**

33. The strategy to select a free hole from a set of available holes can be applied to
- a. first fit
  - b. best fit , worst fit and best fit
  - c. best fit
  - d. worst fit

**Answer: b**

34. By adding the number of page frames in RAM using FIFO page replacement will
- a. No changes in page fault
  - b. Now and then there is an increase in no of page faults
  - c. Every time rise the no of page faults
  - d. Every time reduce the no of page faults

**Answer: b**

35. readcount = 0 ,mutex=1 and write= 1 belongs to
- a. producer and consumer problem
  - b. dinning philosopher problem
  - c. **readers writers problem**
  - d. bankers algorithm

**Answer: c**

36. Which thread cannot be scheduled by kernel

- a) ULT
- b) KLT
- c) Both ULT and KLT cannot be scheduled
- d) Both ULT and KLT

**Answer: a**

37. Find the page fault count using optimal page replacement. The reference values are 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3 and frame size is 3.

- a. 9
- b. 8
- c. 7
- d. 10

**Answer: b**

37. Which of the following statements about semaphores is false?

- a. A thread performs the P operation after it enters its critical section.
- b. A thread performs the V operation before exiting its critical section.
- c. Initializing a semaphore sets the value of a protected variable to indicate that no thread is executing its critical section.
- d. Initializing a semaphore creates a queue that stores references to threads waiting to enter their critical sections protected by that semaphore.

**Answer: a**

38. Which of the following is NOT true of deadlock prevention and deadlock avoidance schemes?

- a. In deadlock prevention, the request for resources is always granted if the resulting state is safe
- b. In deadlock avoidance, the request for resources is always granted if the result state is safe
- c. Deadlock avoidance is less restrictive than deadlock prevention
- d. Deadlock avoidance requires knowledge of resource requirements a priori

**Answer: a**

39. In one of the deadlock prevention methods, impose a total ordering of all resource types, and require that each process requests resources in an increasing order of enumeration. This violates the \_\_\_\_\_ condition of deadlock

- a. Mutual exclusion
- b. Hold and Wait
- c. Circular Wait
- d. No Preemption

**Answer: c**

Q1. A linear time invariant system is said to be

- A) Stable if its response of any bounded input is bounded
- B) Unstable if its response of any bounded input is bounded
- C) Stable if its response of any unbounded input is said to be bounded
- D) Unstable if its response of any bounded input is said to be unbounded

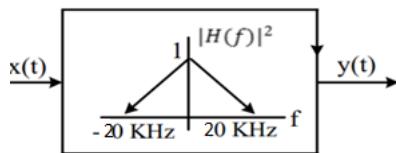
ANSWER: A

Q2. A narrowband noise exhibits

- A) both amplitude and frequency modulation
- B) phase modulation
- C) amplitude modulation
- D) frequency modulation

ANSWER: A

Q3. A white noise process  $X(t)$  with two-sided power spectral density  $1 \times 10^{-12} \text{ W/Hz}$  is input to a filter whose magnitude squared response is shown below. The power of the output process  $y(t)$  is given by



- A)  $10 \times 10^{-9}$
- B)  $5 \times 10^{-12}$
- C)  $20 \times 10^{-9}$
- D)  $40 \times 10^{-6}$

ANSWER: C

Q4. A white noise with power density  $N(t)$  has  $R_x(\tau) = [0.2 e]^{-|4\tau|}$ . Find its power density spectrum

- A)  $1.6/(16+\omega^2)$
- B)  $0.8/(16+\omega^2)$
- C)  $1.6/(4+\omega^2)$
- D)  $0.8/(4+\omega^2)$

ANSWER: A

Q5. A zero-mean white gaussian noise is passed through an ideal lowpass filter of bandwidth 10KHz. The output is then uniformly sampled with sampling period  $t_s = 0.03\text{msec}$ . The samples so obtained would be

- A) Correlated
- B) Uncorrelated
- C) Statistically independent
- D) Orthogonal

ANSWER: B

Q6. Find the effective noise temperature given the standard noise figure as 2.8

- A) 812K
- B) 522K
- C) 232K
- D) 542K

ANSWER: B

Q7. Find the noise bandwidth of the system have power transfer function  $\left[|H(\omega)|\right]^2=1/\left[\left[1+(\omega/W)\right]^2\right]^2$  considering  $|H(0)|=1$

- A)  $\pi W/2$
- B)  $\pi W/4$
- C)  $\pi W/8$
- D)  $\pi W/2\sqrt{2}$

ANSWER: B

Q8. For a three stage cascade amplifier, calculate the overall noise figure when each stage has a gain of 12 DB and noise figure of 8dB.

- A) 12
- B) 24
- C) 13.55
- D) 8

ANSWER: C

Q9. If  $x[n]=Ae^{jn\omega_0}$  is the input of an LTI system and  $h[n]$  is the response of the system, then what is the output  $y[n]$  of the system?

A)  $H(-\omega)x[n]$

B)  $-H(\omega)x[n]$

C)  $H(\omega)x[n]$

D) None

ANSWER: C

Q10. If  $X(t)$  and  $Y(t)$  are jointly WSS, find the relationship between autocorrelation and cross-correlation function as

A)  $R_{YY}(\tau)=R_{YX}(\tau)*h(\tau)$

B)  $R_{YX}(\tau)=R_{XX}(\tau)*h(\tau)$

C)  $R_{XY}(\tau)=R_{XX}(\tau)*h(\tau)$

D)  $R_{YY}(\tau)=R_{XX}(\tau)*h(\tau)$

ANSWER: A

Q11. If  $X(t)$  and  $Y(t)$  are jointly WSS, find the relationship between autocorrelation and cross-correlation function as

A)  $R_{YY}(\tau)=R_{YX}(\tau)*h(\tau)$

B)  $R_{YX}(\tau)=R_{XX}(\tau)*h(\tau)$

C)  $R_{XY}(\tau)=R_{XX}(\tau)*h(\tau)$

D)  $R_{YY}(\tau)=R_{XX}(\tau)*h(\tau)$

ANSWER: A

Q12. Noise factor for a system is defined as the ratio of

A) Input noise power ( $P_{ni}$ ) to output noise power ( $P_{no}$ )

B) Output noise power ( $P_{no}$ ) to input noise power ( $P_{ni}$ )

C) Output noise power ( $P_{no}$ ) to input signal power ( $P_{si}$ )

D) Output signal power ( $P_{so}$ ) to input noise power ( $P_{ni}$ )

ANSWER: B

Q13. Noise is added to a signal in a communication system

A) At the receiving end

- B) At transmitting antenna
- C) In the channel
- D) During regeneration of the information

ANSWER: C

Q14. \_\_\_\_\_ noise is sometimes called white noise.

- A) Thermal
- B) Atmospheric
- C) Transit-time
- D) Flicker

ANSWER: A

Q15. Noise with uniform power spectral density of  $N_0$  is passed through filter  $H(\omega) = 2$  followed by an ideal low pass filter of bandwidth 'B' Hz. The output noise power in watts is

- A)  $2N_0B$
- B)  $4N_0B$
- C)  $16N_0B$
- D)  $8N_0B$

ANSWER: B

Q16. The first central moment of a random variable is,

- A) 0
- B) 1
- C) 2
- D) 3

ANSWER: A

Q17. Which of the following second order joint moments is called the correlation of X and Y, where X and Y are random variables?

- A)  $[ m_{11} ]$
- B)  $[ m_{20} ]$
- C)  $[ m_{02} ]$

D) None of the options

ANSWER: A

Q18. Two random variables X and Y are uncorrelated if their correlation is,

A)  $E[X]E[Y]$

B)  $E[X]$

C)  $E[Y]$

D) None of the options

ANSWER: A

Q19. Two random variables are orthogonal if their correlation is

A) 0

B) 1

C) 2

D) 3

ANSWER: A

Q20. If a random process,  $X(t)$ , has a periodic component, then the autocorrelation will have

A) a periodic component with the same period.

B) a periodic component with the twice period.

C) no periodic component.

D) None of the options.

ANSWER: A

Q21. If Random process A and B are uncorrelated with the same variance then,  $X(t)$  and  $Y(t)$  are

A) Wide Sense Stationary

B) jointly Wide Sense stationary

C) All of the options

ANSWER: C

Q22. If X and Y are random variable, then

A)  $E[XY]=E[X]E[Y]$

- B)  $E[XY]=E[X]$
- C)  $E[XY]=E[Y]$
- D)  $E[XY]=0$

ANSWER: A

Q23. The normalized third central moment is known as,

- A) Skewness of the density function
- B) Mode of the density function
- C) Median of the density function
- D) None of the options

ANSWER: A

Q24. Zeroth central moment of a random variable is,

- A) 1
- B) 0
- C) 2
- D) 3

ANSWER: A

Q25. The distribution function of random variable is

- A)  $P(X \text{ less than } x)$
- B)  $P(X \text{ greater than or equal to } x)$
- C)  $P(X \text{ less than or equal to } x)$
- D)  $P(X \text{ greater than } x)$

ANSWER: C

Q26. The noise temperature at a resistor depends upon

- A) Resistance value
- B) Noise power
- C) Resistance value and noise power
- D) None

ANSWER: B

Q27. Thermal noise is also known as

- A) Shot noise
- B) white noise
- C) Flicker noise
- D) Johnson noise

ANSWER: D

Q28. The spectral density of white noise

- A) is constant
- B) varies with bandwidth
- C) varies with amplitude
- D) varies with frequency

ANSWER: A

Q29. Two different resistors  $R_1 = 4\Omega$ ,  $R_2 = 8 \Omega$  at two different temperature  $T_1=230K$  and  $T_2 = 260K$  are placed in series. Find the effective noise temperature

- A) 300K
- B) 260K
- C) 250K
- D) 245K

ANSWER: C

Q30. Two different resistors  $R_1 = 4\Omega$ ,  $R_2 = 8 \Omega$  at two different temperature  $T_1=230K$  and  $T_2 = 260K$  are placed in series. Find the effective noise temperature

- A) 300K
- B) 260K
- C) 250K
- D) 245K

ANSWER: C

Q31. Two resistor  $R_1$  and  $R_2$  (in ohms) at temperatures  $T_1*K$  and  $T_2*K$  respectively, are connected in series. Their equivalent noise temperature is -----\*K

A)  $T_e = (R_1 T_1 + R_2 T_2) / (R_1 + R_2)$

B)  $T_e = (R_1 T_1 + R_2 T_2)$

C)  $T_e = (R_1 + R_2) / (R_1 T_1 + R_2 T_2)$

D)  $T_e = (R_1 + R_2)$

ANSWER: A

Q32. Which of the following system is non-causal

A)  $h(t) = e^{-t} u(t)$

B)  $h(t) = u(t) e^{-3t}$

C)  $h(t) = u(t+3)$

D)  $h(t) = 0$

ANSWER: C

Q33. White gaussian noise is passed through a linear narrow band filter. The probability density function of the envelope of the noise at the filter output is

A) Uniform

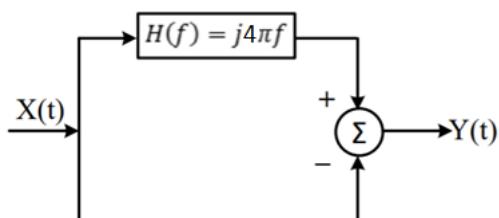
B) Gaussian

C) Poisson

D) Rayleigh

ANSWER: D

Q34.  $X(t)$  is a stationary random process with an autocorrelation function  $R_x(\tau) = e^{\alpha(-\pi|\tau|)^2}$  is passed through the system below. The power spectral density of the output process  $Y(t)$  is



A)  $(16\pi^2 f^2 + 1) e^{\alpha(-\pi f)^2}$

B)  $(16\pi^2 f^2 - 1) e^{\alpha(-\pi f)^2}$

C)  $(16\pi^2 f^2 + 1) e^{\alpha(-\pi f)}$

D)  $(16\pi^2 f^2 - 1) e^{\alpha(-\pi f)}$

ANSWER: A

Q35. Marginal distribution of one random variable can be obtained by setting the value of the other variable infinite in the Joint Distribution Function.

ANSWER: True

Q36.  $E[X]=3$ ,  $E[X^2]=11$ ,  $Y=-6X+22$ . Then X and Y are not orthogonal.

ANSWER: FALSE

Q37.  $E[X]=3$ ,  $E[X^2]=11$ ,  $Y=-6X+22$ . Then X and Y are uncorrelated.

ANSWER: FALSE

Q38. Two processes  $X(t)$  and  $Y(t)$  are called cross-correlation-ergodic, or ergodic in the correlation, if the time cross-correlation function is equal to the statistical cross-correlation function.

ANSWER: True

Q39. The auto correlation of a random variable is bounded by its value at the origin.

ANSWER: True

Q40. The autocorrelation function has odd symmetry.

ANSWER: FALSE

Q41. For two random variables X and Y, the joint probability density function or joint density function, is defined by the second derivative of the joint distribution function wherever it exists.

ANSWER: True

Q42. Two random processes X and Y are uncorrelated if their covariance is zero.

ANSWER: True

Q43. If two random processes X and Y are uncorrelated, then  $R_{XY}(t,t+\tau)=E[X(t)]E[Y(t+\tau)]$ .

ANSWER: True

Q44. If the Gaussian process is wide sense stationary, the mean will be constant.

ANSWER: True

Q45. If the Gaussian process is wide sense stationary, then the auto correlation and auto-covariance functions will depend only on time differences and not absolute time.

ANSWER: True

Q46. Two complex processes  $Z_i(t)$  and  $Z_j(t)$  are jointly wide sense stationary if each is wide sense stationary and their cross correlation function is a function of time differences only and not absolute time.

ANSWER: True

Q47. If X and Y are random variables and their probability density function is  $f_{X,Y}(x,y)$ , then  $f_{X,Y}(x,y) \geq 0$

ANSWER: True

Q48. If the distribution function of one random variable X conditioned by the fact that a second random variable Y has some specific value y. Then it is called point conditioning.

ANSWER: True

Q49. Probability Mass Function for a random variable X is denoted by

$$P_x(x)=P(Y=y)$$

Q50.  $0 \leq p(x,y) \leq \infty$

Where,  $p(x,y)$  is the joint probability mass function.

ANSWER: FALSE

### Semiconductor Fundamentals:

1. Using Fermi function, evaluate the temperature at which there is 1% probability of an electron in a solid having energy 0.5eV above EF of 5eV.
  - a. 1261K
  - b. 1355K
  - c. 1550K
  - d. 1200K

Ans: 1261K

2. For what value of voltage will the reverse current ( $I_o$ ) in a PN junction Ge diode reach 90% of its saturation value at room temperature?
  - a. 0.06V
  - b. 0.02V
  - c. 0.01V
  - d. 0.09V

Ans: 0.06V

3. A silicon PN Junction diode is doped with  $N_A = 10^{16} \text{ cm}^{-3}$  and  $N_D = 5 \times 10^{14} \text{ cm}^{-3}$ . Determine the built-in potential of this device.
  - a. 0.621V
  - b. 0.221V
  - c. 0.421V
  - d. 0.531V

Ans: 0.621V

4. A  $2 \times 2 \mu\text{m}$  area of  $n^+$  is diffused into a p-type silicon substrate doped at  $N_A = 10^{16} \text{ cm}^{-3}$  to form a p-n junction diode that has a built-in potential of 0.75V. What is the donor concentration ( $\text{cm}^{-3}$ ) in the  $n^+$  region?
  - a.  $7.085 \times 10^{16}$
  - b.  $5.055 \times 10^{16}$
  - c.  $5.485 \times 10^{15}$
  - d.  $5.585 \times 10^{16}$

Ans:  $7.085 \times 10^{16}$

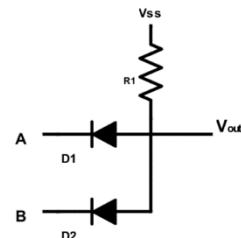
5. Consider a GaAs sample at 300K,  $N_a = 0$ ,  $N_d = 10^{16} \text{ cm}^{-3}$  with complete ionization. Calculate the drift current density ( $\text{A}/\text{cm}^2$ ) if applied electric field is 10V/cm.
  - a. 136
  - b. 121
  - c. 110
  - d. 104

Ans: 136

6. With n-type GaAs at 300K, the electron concentration varies linearly from  $1 \times 10^{18}$  to  $7 \times 10^{18} \text{ cm}^{-3}$  over a distance of 0.10cm. Calculate the diffusion current density ( $\text{A}/\text{cm}^2$ ) if  $D_n = 225 \text{ cm}^2/\text{s}$ .
- 108
  - 76
  - 54
  - 116

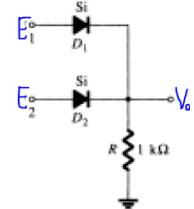
Ans: 108

7. What is the logic gate implemented in the following circuit?
- OR
  - AND
  - NOT
  - NOR



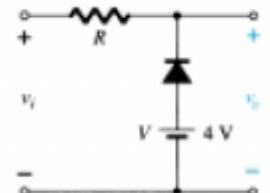
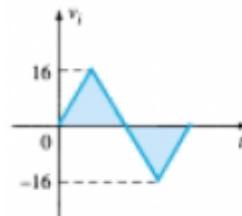
Ans: AND

8. In the given circuit, what is the ideal output  $V_0$  if  $E_1 = 10V$  and  $E_2 = 0V$ ?
- 0V
  - 0.7V
  - 10V
  - 9.3V



Ans: 10V

9. For the given input waveform to the given circuit, what is the minimum value of the output waveform?
- 4V
  - 16V
  - 12V
  - 0V



Ans: The circuit above is a parallel clipper. When the input is less than 4V, then diode is forward biased and thus output voltage is 4V. When input increases above 4V, the diode is reverse biased and output is equal to the input. Hence, minimum output is 4V.

10. Consider a silicon diode with  $\eta=1.2$ . Find the change in voltage if the current changes from 0.1mA to 10mA.
- 0.154V
  - 0.143V
  - 0.123V
  - 0.165V

Ans: 0.143V

Explanation: Equation for diode current

$I = I_0 \times (e^{(V/nV_T)} - 1)$  where  $I_0$  = reverse saturation current

$n$  = ideality factor

$V_T$  = thermal voltage

$V$  = applied voltage

$\eta = 1.2$ ,  $I_2 = 10\text{mA}$ ,  $I_1 = 0.1\text{mA}$  and take  $V_T = 0.026\text{V}$

$$\text{Change in voltage } \Delta V = \eta V_T \ln\left(\frac{I_2}{I_1}\right) = 1.2 \times 0.026 \times \ln\left(10 \times \frac{10^{-3}}{0.1 \times 10^{-3}}\right) = 0.143\text{V}$$

11. The bridge rectifier is preferred to an ordinary two diode full wave rectifier because
- it needs much smaller transformer for the same output
  - no center tap required
  - less PIV rating per diode
  - all the above

Ans: all the above

12. In a rectifier, larger the value of shunt capacitor filter
- larger the peak-to-peak value of ripple voltage
  - larger the peak current in the rectifying diode
  - longer the time that current pulse flows through the diode
  - smaller the dc voltage across the load

Ans: larger the peak current in the rectifying diode

13. The basic purpose of filter is to
- minimize variations in ac input signal
  - suppress harmonics in rectified output
  - remove ripples from the rectified output
  - stabilize dc output voltage

Ans: remove ripples from the rectified output

14. To get a peak load voltage of 40V out of a bridge rectifier. What is the approximate rms value of secondary voltage?
- 0V
  - 14.4V
  - 28.3V
  - 56.6V

Ans: 28.3V

15. Voltage multipliers are circuits best used to produce
- low voltage and low current
  - low voltage and high current
  - high voltage and low current
  - high voltage and high current

Ans: high voltage and low current

16. What is true about the breakdown voltage in a Zener diode?
- It decreases when current increases.
  - It destroys the diode.
  - It equals the current times the resistance.
  - It is approximately constant.

Ans: It is approximately constant

17. A voltage regulator is a circuit which
- Converts the ac voltage to dc voltage
  - Smoothens the ac variation in dc output voltage
  - Maintains a constant dc output voltage inspite of the fluctuations in ac input voltage or load current
  - None of the above

Ans: Maintains a constant dc output voltage inspite of the fluctuations in ac input voltage or load current

18. \_\_\_\_\_ semiconductor is less temperature sensitive.
- Silicon
  - Germanium
  - Gallium Arsenide
  - Indium Phosphide

Ans: Silicon

19. LEDs generate light only when they are \_\_\_\_\_ biased.
- Forward
  - Reverse
  - Neutral
  - Ideal

Ans: Forward

20. A tunnel diode is used in
- high-power circuits
  - circuits requiring negative resistance
  - very fast-switching circuits
  - power supply rectifiers

Ans: circuits requiring negative resistance

21. What type of diode is commonly used in electronic tuners in TVs?
- Varactor
  - Schottky
  - LED
  - Zener

Ans: Varactor

22. The Light Emitting Diode (LED) emits light of a particular color because
- It is fabricated from a fluorescent material
  - the transition between energy levels of the carriers takes place while crossing the p-n junction

- c. the heat generated in the diode is converted into light
- d. the band gap of the semiconductor material used in the fabrication of the diode is equal to the energy  $h\nu$  of the light photon

Ans: the band gap of the semiconductor material used in the fabrication of the diode is equal to the energy  $h\nu$  of the light photon

23. Which of the following is not LED material?
- a. GaAs
  - b. GaP
  - c. SiC
  - d.  $\text{SiO}_2$

Ans:  $\text{SiO}_2$

24. The I-V characteristics of a tunnel diode exhibits
- a. current-controlled negative resistance
  - b. voltage-controlled negative resistance
  - c. temperature-controlled positive resistance
  - d. current-controlled positive resistance

Ans: voltage-controlled negative resistance

25. When reverse biased, PIN diode acts as
- a. Variable resistor
  - b. Constant capacitor
  - c. Current controlled switch
  - d. Current controlled voltage regulator

Ans: Constant capacitor

26. Zener effect depends only on the
- a. High-speed minority carriers
  - b. High-speed majority carriers
  - c. Intensity of the electric field
  - d. Intensity of the magnetic field

Ans: Intensity of the electric field

27. The arrow direction in the diode symbol indicates
- a. Direction of electron flow
  - b. Direction of hole flow
  - c. Opposite to the direction of hole flow
  - d. None of the above

Ans: Direction of hole flow (Direction of conventional current flow)

28. Testing a good diode with an ohmmeter should indicate
- a. high resistance when forward or reverse biased
  - b. low resistance when forward or reverse biased
  - c. high resistance when reverse biased and low resistance when forward biased
  - d. high resistance when forward biased and low resistance when reverse biased

Ans: high resistance when reverse biased and low resistance when forward biased

29. In half-wave rectification if i/p frequency is 50 Hz, then o/p frequency is.....
- 50 Hz
  - 100 Hz
  - 250 Hz
  - 25 Hz

Ans: 25 Hz

30. A forward potential of 10V is applied to a Si diode. A resistance of  $1\text{ K}\Omega$  is also in series with the diode. The current is.....
- 10 mA
  - 9.3 mA
  - 0.7 mA
  - 0 mA

Ans: 9.3 mA

---

- Which of the following BJT terminal controls the current flow?
  - Base**
  - Collector
  - Emitter
  - Drain
- In which of the following region do BJT operates in reverse bias?
  - a.Active
  - b.Cut-off**
  - c.saturation
  - d.both a & c
- Which of the following is the highest value of current ?
  - I<sub>Sat</sub>**
  - I<sub>Cutoff</sub>
  - I<sub>active</sub>
  - All the above
- The emitter follower amplifier is also known as
  - Common collector**
  - Common base
  - Common emitter
  - Differential amplifier
- The approximate value of the current gain of a simplified CB amplifier is
  - 1
  - $\beta$
  - infinity
  - 0

6. The basic purpose of coupling capacitors in CE amplifier is
- blocks dc
  - pass ac
  - reduce distortion
  - pass ac & blocks dc**
7. Consider a CB amplifier configuration with  $V_{CC} = 12V$ ,  $R_1 = 25k\Omega$  and  $R_2 = 6k\Omega$ . The value of  $V_B$  is
- 2.84V
  - 13.03V
  - 2.45V
  - 2.32V**
8. The disadvantages of collector emitter feedback bias circuits is
- Requires few resistors
  - Provides a lot of stability
  - Provides negative feedback**
  - Provides positive feedback
9. In a NPN transistor operating at cut off region, the following is true
- Potential difference between the emitter and the base is smaller than 0.5V
  - Potential difference between the emitter and the base is smaller than 0.4V**
  - The collector current increases with the increase in the base current
  - The collector current is always zero and the base current is always non zero
10. MOSFET has greatest application in digital circuit due to
- Low power consumption**
  - Less noise
  - Small amount of space it takes on a chip
  - All of the above
11. MOSFET is a \_\_\_\_\_ device.
- Tri-terminal
  - Unipolar
  - Voltage-controlled**
  - All as mentioned earlier
12. Choose the correct statement(s)
- The gate circuit impedance of MOSFET is higher than that of a BJT**
  - The gate circuit impedance of MOSFET is lower than that of a BJT
  - The MOSFET has higher switching losses than that of a BJT
  - The MOSFET has same switching losses as that of a BJT
13. Choose the correct statement
- MOSFET is a unipolar, voltage controlled, two terminal device
  - MOSFET is a bipolar, current controlled, three terminal device
  - MOSFET is a unipolar, voltage controlled, three terminal device**
  - MOSFET is a bipolar, current controlled, two terminal device

14. In CMOS logic circuit the n-MOS transistor acts as:

- a) Load
- b) Pull up network
- c) **Pull down network**
- d) Not used in CMOS circuits

15. In CMOS logic circuit, the switching operation occurs because:

- a) Both n-MOSFET and p-MOSFET turns OFF simultaneously for input '0' and turns ON simultaneously for input '1'
- b) Both n-MOSFET and p-MOSFET turns ON simultaneously for input '0' and turns OFF simultaneously for input '1'
- c) **N-MOSFET transistor turns ON, and p-MOSFET transistor turns OFF for input '1' and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input '0'**
- d) none of the above

16. When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is:

- a) 1 or Vdd or HIGH state
- b) 0 or ground or LOW state
- c) **High impedance or floating(Z)**
- d) None of the mentioned

17. The enhancement type basically termed as normally-OFF MOSFET works only with \_\_\_\_\_.

- a. **large positive gate voltage**
- b. large negative gate voltage
- c. large positive drain voltage
- d. large negative drain voltage

18. The depletion mode of MOSFET resemble semantically in the behaviour of JFET due to copious increase in \_\_\_\_\_.

- a. **negative gate voltage by reducing its conductivity level**
- b. negative gate voltage by enhancing its conductivity level
- c. negative source voltage by reducing its conductivity level
- d. negative source voltage by enhancing its conductivity level

19. The passage of majority charge carriers from source to drain terminal takes place through the channel only after an application of

- a. **Drain to Source Voltage ( $V_{DS}$ )**
- b. Gate to Source Voltage ( $V_{GS}$ )
- c. Gate to Gate Voltage ( $V_{GG}$ )
- d. Drain to Drain Voltage ( $V_{DD}$ )

20. Which action plays a significant role in enhancing the conductivity of channel by inducing the free electrons especially in enhancement mode of N-channel MOSFET?

- a. Inductor action
- b. **Capacitor action**
- c. Resistive action
- d. Filter action



1. The type of systems which are characterized by input and the output quantized at certain levels are called as

- a) analog
- b) discrete
- c) continuous
- d) digital

Ans: b)

2. An example of a discrete set of information/system is

- a) the trajectory of the Sun
- b) data on a CD
- c) universe time scale
- d) movement of water through a pipe

Ans: b)

3. A system which is linear is said to obey the rules of

- a) scaling
- b) additivity
- c) both scaling and additivity
- d) homogeneity

Ans: c)

4. A time invariant system is a system whose output

- a) increases with a delay in input
- b) decreases with a delay in input
- c) remains same with a delay in input
- d) vanishes with a delay in input

Ans: c)

5. A system is said to be defined as non causal, when

- a) the output at the present depends on the input at an earlier time

- b) the output at the present does not depend on the factor of time at all
- c) the output at the present depends on the input at the current time
- d) the output at the present depends on the input at a time instant in the future

Ans: d)

6. When we take up design of systems, ideally how do we define the stability of a system?

- a) A system is stable, if a bounded input gives a bounded output, for some values of the input
- b) A system is unstable, if a bounded input gives a bounded output, for all values of the input
- c) A system is stable, if a bounded input gives a bounded output, for all values of the input
- d) A system is unstable, if a bounded input gives a bounded output, for some values of the input

Ans: c)

7. Fourier series is not true in case of discrete time signals

A. True

B. False

Ans: Fasle

8. Fourier Series represents which domain representation of Signals?

a. Time domain

b. Frequency Domain

c) Both

D) Neither

Ans: b)

9. How is it that Fourier Series help represent periodic signals

a. Harmonically related

b. Periodically related

c. Sinusoidally related

d. Exponentially related

Ans: a)

10. What is the Fourier Transform  $X(\omega)$  of the signal  $x(n)$ ?

- a.  $\text{Pi}$
- b.  $1$
- c. Non-periodic
- d.  $2\pi$

Ans: a.

11. The oscillatory behaviour of the approximation of  $X_N(\omega)$  to the function  $X(\omega)$  at a point of discontinuity of  $X(\omega)$  is known as Gibb's phenomenon.

- a. true
- b. false

Ans: True

12. Which of the following relationships is true if the  $x(n)$  is real?

- a.  $X^*(\omega) = X(\omega)$
- b.  $X^*(\omega) = X(-\omega)$
- c.  $X^*(\omega) = -X(\omega)$
- d. None of the above

Ans: b)

13. Which of the following condition is to be satisfied for the Fourier Transform of the sequence to be equal as Z transform of the same sequence?

- a.  $|Z| = 1$
- b.  $|Z| > 1$
- c.  $|Z| < 1$
- d. Cannot be equal

Ans: a)

14. If a power signal has its power concentrated about zero frequency, the signal is known as

- a. Low frequency signal
- b. Middle frequency signal
- c. High frequency signal

d. None of the above

Ans. a)

15. If the ROC of the system function is the exterior of the circle of radius  $r < \infty$ , including the point  $z = \infty$ , then the system is said to be

- a. Stable
- b. Causal
- c. Non-causal
- d. None of the above

Ans: b)

16. A linear time-invariant system is said to be BIBO stable if and only if the ROC of the system function

- a. Includes unit circle
- b. Excludes unit circle
- c. Is a unit circle
- d. None of the mentioned.

Ans. a)

17. The Fourier series for the signal  $x(n) = \cos\sqrt{2\pi}n$  exists

- a. True
- b. False

Ans. b)

18. Which of the following is true when the sampling time is less than Nyquist interval?

- a. Original signal cannot be recreated
- b. Bandwidth decreases
- c. Bandwidth increases
- d. Channel capacity decreases

Ans: a)

19. Consider a noise channel with a bandwidth of 4000 Hz transmitting a signal with two signal levels. What can be the maximum bit rate?

1. 1000 bps
2. 4000 bps
3. 8000 bps
4. 2000 bps

Ans: c)

20. A signal of maximum frequency  $f_0$  10 kHz is sampled at Nyquist rate. The time interval between two successful samples is

- a. 50 microseconds
- b. 100 microseconds
- c. 500 microseconds
- d. 1000 microseconds

Ans: a)

21. The spectrum of a bandpass signal spans from 20 kHz to 30 kHz. The signal can be recovered ideally from the sampled value the sampling rate is atleast

- a. 20 kHz
- b. 60 kHz
- c. 50 kHz
- d. 40 kHz

Ans. a)

22. To satisfy the sampling theorem, a 100 Hz sine wave must be sampled at

- a. 10 Hz
- b. 100 Hz
- c. 200 Hz
- d. 50 Hz

Ans: c)

23. If  $x(n)$  is a stable sequence so that  $X(z)$  converges on a unit circle, then the complex spectrum signal is given by

- a.  $X(\ln X(Z))$
- b.  $\ln X(Z)$
- c.  $X^{-1}(\ln X(Z))$
- d. None of the above

Ans: c)

24. What are the main characteristics of anti-aliasing filter?

- a. **Ensures that bandwidth of signal to be sampled is limited to frequency range**
- b. To limit the additive noise spectrum and other interference which corrupts the signal
- c. Both a) and b)
- d. None of the above.

25. If all the poles of  $H(Z)$  are inside the unit circle, then the system is said to be

- a. Only causal
- b. Only BIBO causal
- c. **BIBO stable and causal**
- d. None of the mentioned

26. If  $DFT[x(n)] = X(k)$ , then  $DFT[x((-n))N]$  is

- A.  $X(N-k)$
- B.  $X(N+k)$
- C.  $X(N)$
- D.  $X(k)$

ANSWER: A

27. The third sample  $X(2)$  of the DFT for a sequence  $x(n) = \{1,1,-2,-2\}$

- A. 0
- B. 1
- C. j

D. 2

ANSWER: A

28. Find second sample  $x(1)$  of the IDFT of  $Y(k) = \{1,0,1,0\}$

A. 1

B. 0

C. 2

D. 3

ANSWER: B

29. If 5 and 6 are the orders of numerator and denominator of rational system function respectively, then how many additions are required in direct form-I realization of that IIR filter?

A. 10

B. 13

C. 11

D. 12

ANSWER: C

30. If M and N are the orders of numerator and denominator of rational system function respectively, then how many memory locations are required in direct form-I realization of that IIR filter?

A.  $M+N$

B.  $M+N+1$

C.  $M+N-1$

D.  $M+N+2$

ANSWER: A

31. If 8 and 10 are the orders of numerator and denominator of rational system function respectively, then how many memory locations are required in direct form-II realization of that IIR filter?

A. 8

B. 11

C. 14

D. 10

ANSWER: D

32. What is the general system function of an FIR system?

A. Summation of  $b_k x(n-k)$  ( $k$  varies from 0 to  $M-1$ )

B. Summation of  $b_k z^{-k}$  ( $k$  varies from 0 to  $M$ )

C. Summation of  $b_k z^{-k}$  ( $k$  varies from 0 to  $M-1$ )

D. None of the mentioned

ANSWER: C

33. By combining two pairs of poles to form a fourth order filter section, by what factor we have reduced the number of multiplications?

A. 50 percentage

B. 30 percentage

C. 20 percentage

D. 40 percentage

ANSWER: A

34. How many memory locations are used for storage of the output point of a sequence of length 11 in direct form realization of FIR system?

A. 11

B. 12

C. 13

D. 10

ANSWER: B

What is the use of zero padding?

A. better time resolution

- B. Non-linear filtering
- C. none
- D. Better display of the frequency spectrum

ANSWER: D

35. Which of the following is used in the realization of a digital system?

- A. Delay elements
- B. Multipliers
- C. Adders
- D. All of the mentioned

ANSWER: D

36. In bilinear transformation, the left-half s-plane is mapped to which of the following in the z-domain?

- A. Entirely outside the unit circle mod of  $z=1$
- B. Partially outside the unit circle mod of  $z=1$
- C. Partially inside the unit circle mod of  $z=1$
- D. Entirely inside the unit circle mod of  $z=1$

ANSWER: D

37. If  $s=\sigma+j\Omega$  and  $z=r\exp(j\omega)$ , then what is the condition on  $\sigma$  if  $r$  is less than 1?

- A.  $\sigma$  greater than 0
- B.  $\sigma$  less than 0
- C.  $\sigma$  greater than 1
- D.  $\sigma$  less than 1

ANSWER: B

38. The incorrect statement about the Impulse Invariant method is

- A. No warping effect
- B. It can easily convert discrete filters into analog filters
- C. Absence of many-to-one mapping
- D. It preserves the frequency characteristics

ANSWER: C

39. The number of multiplications needed in the calculation of DFT with 64-point sequence is

- A. 4000
- B. 4094
- C. 192
- D. 4096

ANSWER: D

40. The number of additions needed in the calculation of FFT with 64-point sequence is

- A. 192
- B. 194
- C. 384
- D. 380

ANSWER: C

41. The bit reversal index for a binary representation 1101 is

- A. 4
- B. 7
- C. 2
- D. 11

ANSWER: D

42. Find the number of block of the processed data with the input samples 16000 and the filter length 100. Assume the block size of FFT be 1024

A. 34

B. 17

C. 14

D. 25

ANSWER: B

43. The number of butterflies per stage for the flow graph of 16-point DIT-FFT is

A. 4

B. 8

C. 7

D. 6

ANSWER: B

44. The number of input samples for 4th stages DIF-FFT algorithm is

A. 8

B. 16

C. 32

D. 4

ANSWER: B

45. Which of the following rule is used in the bilinear transformation?

A. Simpson's rule

B. Backward difference

C. Forward difference

D. Trapezoidal rule

ANSWER: D

46. Which of the following substitution is done in Bilinear transformations?

- A.  $s = 2/T[1+z-1/1-z]$
- B.  $s = 2/T[1+z-1/1-z-1]$
- C.  $s = (2/T)[1-z-1/1+z-1]$
- D. None of the mentioned

ANSWER: C

47. What is the value of integration of  $x(t)dt$  according to trapezoidal rule? ( $t$  varies from  $(n-1)T$  to  $nT$ )

- A.  $[x(nT)-x((n-1)T)/2]T$
- B.  $[x(nT)+x((n-1)T)/2]T$
- C.  $[x(nT)-x((n+1)T)/2]T$
- D.  $[x(nT)+x((n+1)T)/2]T$

ANSWER: B

48. Which of the following methods are used to convert analog filter into digital filter?

- A. Approximation of Derivatives
- B. Bilinear transformation
- C. Impulse invariance
- D. All of the mentioned

ANSWER: D

49. What is the relation between  $h(t)$  and  $H_a(s)$ ?

- A.  $H_a(s)=\text{integration of } h(t)e^{-stdt} \text{ (limit varies from -infinity to + infinity)}$
- B.  $H_a(s)=\text{integration of } h(t)e^{stdt} \text{ (limit varies from zero to + infinity)}$
- C.  $H_a(s)=\text{integration of } h(t)e^{stdt} \text{ (limit varies from -infinity to + infinity)}$
- D. None of the mentioned

ANSWER: A

50. What is the kind of relationship between  $\Omega$  and  $\omega$ ?

- A. Many-to-one
- B. One-to-many
- C. One-to-one
- D. Many-to-many

ANSWER: C

51. In inverse DTFT, the limits of the integral is defined between  $-\pi$  to  $\pi$  because of the following property:

- (a) Time Invariance
- (b) Convolution
- (c) Periodicity**
- (d) Linearity

52. Which among the following assertions represents a necessary condition for the existence of Fourier Transform of discrete time signal (DTFT)?

- a. Discrete Time Signal should be absolutely summable**
- b. Discrete Time Signal should be absolutely multipliable
- c. Discrete Time Signal should be absolutely integrable
- d. Discrete Time Signal should be absolutely differentiable

53. What is the DTFT of unit impulse function?

- a. 1
- b.  $\pi$
- c.  $\pi/2$
- d. None of the above

54. What is the discrete time Fourier Series of a periodic impulse train with period 'N'?

- (a)  $1/N$
- (b) N
- (c) Impulse train**
- (d) None of the above

55. What is the DTFT of the sequence given:  $x[n]=\alpha^n u[n]$ ?

With  $\alpha < 1$

(a)  $\frac{1}{(1+\alpha e^{j\omega n})}$

(b)  $\frac{1}{1-\alpha e^{j\omega}}$

(c)  $\frac{\alpha}{1-\alpha e^{j\omega}}$

(d)  $\frac{1}{1-\alpha e^{-j\omega}}$

56. Given a discrete time signal  $x[k]$  defined by  $x[k] = 1$ , for  $-2 \leq k \leq 2$  and 0, for  $|k| > 2$ . Then,  $y[k] = x[3k-2]$  is \_\_\_\_\_

(a)  $y[k] = 0$ , for  $k = 0, 1$  and 1 otherwise

**(b)  $y[k] = 1$ , for  $k = 0, 1$  and 0 otherwise**

(c)  $y[k] = -1$ , for  $k = 0, 1$  and 0 otherwise

(d)  $y[k] = 1$ , for  $k = 0, 1$  and -1 otherwise

57. A discrete time signal is as given below

$X[n] = \cos(\pi n/2) - \sin(\pi n/8) + 3 \cos(\pi n/4 + \pi/3)$  The period of the signal  $X[n]$  is

(a) 19

**(b) 16**

(c) 4

(d) 2

58. A Discrete signal is said to be even or symmetric if  $X(-n)$  is equal to

(a)  $X(-n)$

(b)  $-X(-n)$

**(c)  $X(n)$**

(d)  $-X(n)$

59. The Z transform of  $\delta(n - m)$  is \_\_\_\_\_

- a)  $z^{-n}$
- b)  $z^{-m}$**
- c)  $1/z^{-n}$
- d)  $1/z^{-m}$

60. Which basic property of DFT is not valid?

- (a) Linearity
- (b) Periodicity
- (c) Circular Symmetry
- (d) Summation**

61. Which of the following is true regarding the number of computations required to compute an N-point DFT?

- a)  **$N^2$  complex multiplications and  $N(N-1)$  complex additions**
- b)  $N^2$  complex additions and  $N(N-1)$  complex multiplications
- c)  $N^2$  complex multiplications and  $N(N+1)$  complex additions
- d)  $N^2$  complex additions and  $N(N+1)$  complex multiplications

62. Which of the following is true regarding the number of computations required to compute DFT at any one value of 'k'?

- a)  $4N-2$  real multiplications and  $4N$  real additions
- b)  $4N$  real multiplications and  $4N-4$  real additions
- c)  $4N-2$  real multiplications and  $4N+2$  real additions
- d)  $4N$  real multiplications and  $4N-2$  real additions**

63. Divide-and-conquer approach is based on the decomposition of an N-point DFT into successively smaller DFTs. This basic approach leads to FFT algorithms.

- a) True**
- b) False
- c) Can be true or false
- d) None of the above

64. How many complex multiplications are performed in computing the N-point DFT of a sequence using divide-and-conquer method if  $N=LM$ ?

- a)  $N(L+M+2)$
- b)  $N(L+M-2)$**

c)  $N(L+M-1)$

**d)  $N(L+M+1)$**

65. FFT may be used to calculate

i) DFT, ii) IDFT, iii) Direct Z transform, iv) In direct Z transform

a. i, ii and iii are correct

**b. i and ii are correct**

c. i and iii are correct

d. All the four are correct

66. In Overlap-Add Method with linear convolution of a discrete-time signal of length L and a discrete-time signal of length M, for a length N, zero padding should be of length

a.  $L, M > N$

b.  $L, M = N$

**c.  $L, M < N$**

d.  $L, M < N^2$

67. What is the set of all values of z for which  $X(z)$  attains a finite value?

**a) Radius of convergence**

b) Radius of divergence

c) Feasible solution

d) None of the mentioned

68. What is the z-transform of the following finite duration signal?

$$x(n)=\{2, 4, 5, 7, 0, 1\}$$

↑

a)  $2 + 4z + 5z^2 + 7z^3 + z^4$

b)  $2 + 4z + 5z^2 + 7z^3 + z^5$

c)  $2 + 4z^{-1} + 5z^{-2} + 7z^{-3} + z^{-5}$

**d)  $2z^2 + 4z + 5 + 7z^{-1} + z^{-3}$**

69. What is the ROC of the signal  $x(n)=\delta(n-k)$ ,  $k>0$ ?

a)  $z=0$

b)  $z=\infty$

**c) Entire z-plane, except at  $z=0$**

d) Entire z-plane, except at  $z=\infty$

70. What is the z-transform of the signal  $x(n)=(0.5)^n u(n)$ ?

**a)  $1/(1-0.5z^{-1})$ ; ROC  $|z|>0.5$**

b)  $1/(1-0.5z^{-1})$ ; ROC  $|z|<0.5$

c)  $1/(1+0.5z^{-1})$ ; ROC  $|z|>0.5$

d)  $1/(1+0.5z^{-1})$ ; ROC  $|z|<0.5$

71. What is the ROC of the z-transform of the signal  $x(n) = a^n u(n) + b^n u(-n-1)$ ?

- a)  $|a| < |z| < |b|$
- b)  $|a| > |z| > |b|$
- c)  $|a| > |z| < |b|$
- d)  $|a| < |z| > |b|$

72. What is the ROC of z-transform of finite duration anti-causal sequence?

- a)  $z=0$
- b)  $z=\infty$
- c) Entire z-plane, except at  $z=0$
- d) Entire z-plane, except at  $z=\infty$**

73. What is the ROC of the system function  $H(z)$  if the discrete time LTI system is BIBO stable?

- a) Entire z-plane, except at  $z=0$
- b) Entire z-plane, except at  $z=\infty$
- c) Contain unit circle**
- d) None of the mentioned

74. The ROC of z-transform of any signal cannot contain poles.

- a) True**
- b) False
- c) cannot be commented
- d) can be true for some cases

75. The transfer function of the system defined by the difference equation

$y(n) = x(n) + y(n - 1)$  is:

- a)  $z/z + 1$
- b)  $z/2z$
- c)  $z/z - 1$**
- d)  $z - 1/z$