For this checkpoint, you’ll demonstrate correctly reading an input trace file and maintaining simulation time, inserting memory requests into the queue at the appropriate time and (for the purposes of the demo) removing items from the queue once they’ve been present for 100 clock cycles.     Display the current simulation time and the information from the request (request time, read/write, address — and bank/bankgroup/row/col if you want to impress us) whenever something is inserted into the queue.   Display the current simulation time and the information you kept in the queue (ideally the read/write and address or at least it’s components) whenever you remove anything from the queue.   Note that you should be "smart" about advancing simulation time.   As long as there’s anything in the queue, you should advance simulation time by 1 clock tick (then do potentially do something if appropriate (e.g. read file/insert into queue, remove from queue).   However, if the queue is empty you can simply advance simulation time to the time of the next request in the trace file.