Midterm Report
ECE437

Team: Cong Ku, Zhiyang Lin
Teaching Assistant: Pranav
Due date: March 6, 2015

Overview

In the past 7 weeks, We have successfully built two versions of processors based on MIPS: Single-Cycle version and Pipelined version.

Each design have their own benefits. Single-cycle version is a more easy and understandable design compare with Piplined version. Everything is completed within one clock cycle. There are less combination logic in this design, so the power consumption will be lower. Int the other hand, Pipelined version is harder to design and need more combination logic to be able to prevent hazard and work correctly. The power consumption will be higher. The big benefit Pipelined version have over Single-cycle cycle is the low latency for each stage. This make Piplelined version a so much faster design.

The test bench selected to test processors is mergesort.asm. Mergesort.asm have lots of branches , jumps and R-type instructions. The complexity and long execution period make it a good test bench for comparing our two designs.

The performance of each CPU design is represented by their mips (Million instructions per second). To calculate mips, we need the total execution time of program and the total instructions program have run.

After the test, we found Pipelined version is the winner. It have better clock cycle and better mips.

Processor Design

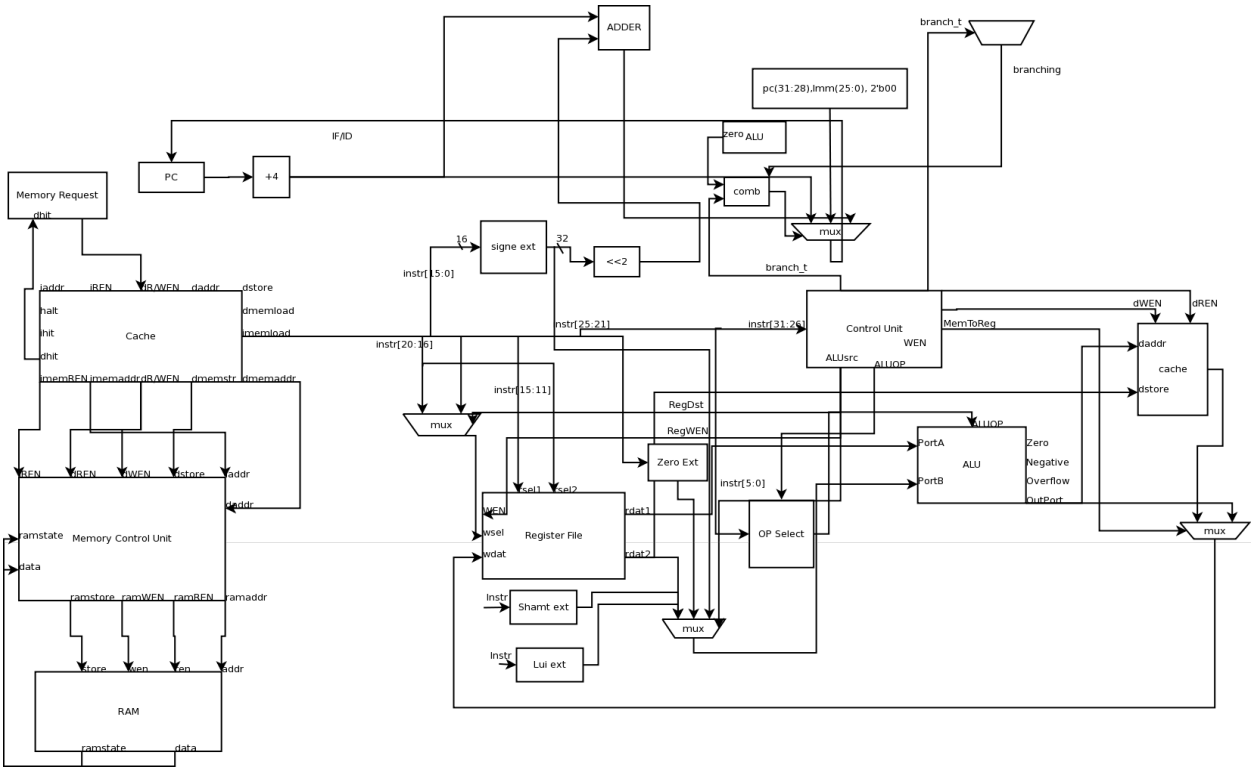

figure.1 Single-cycle

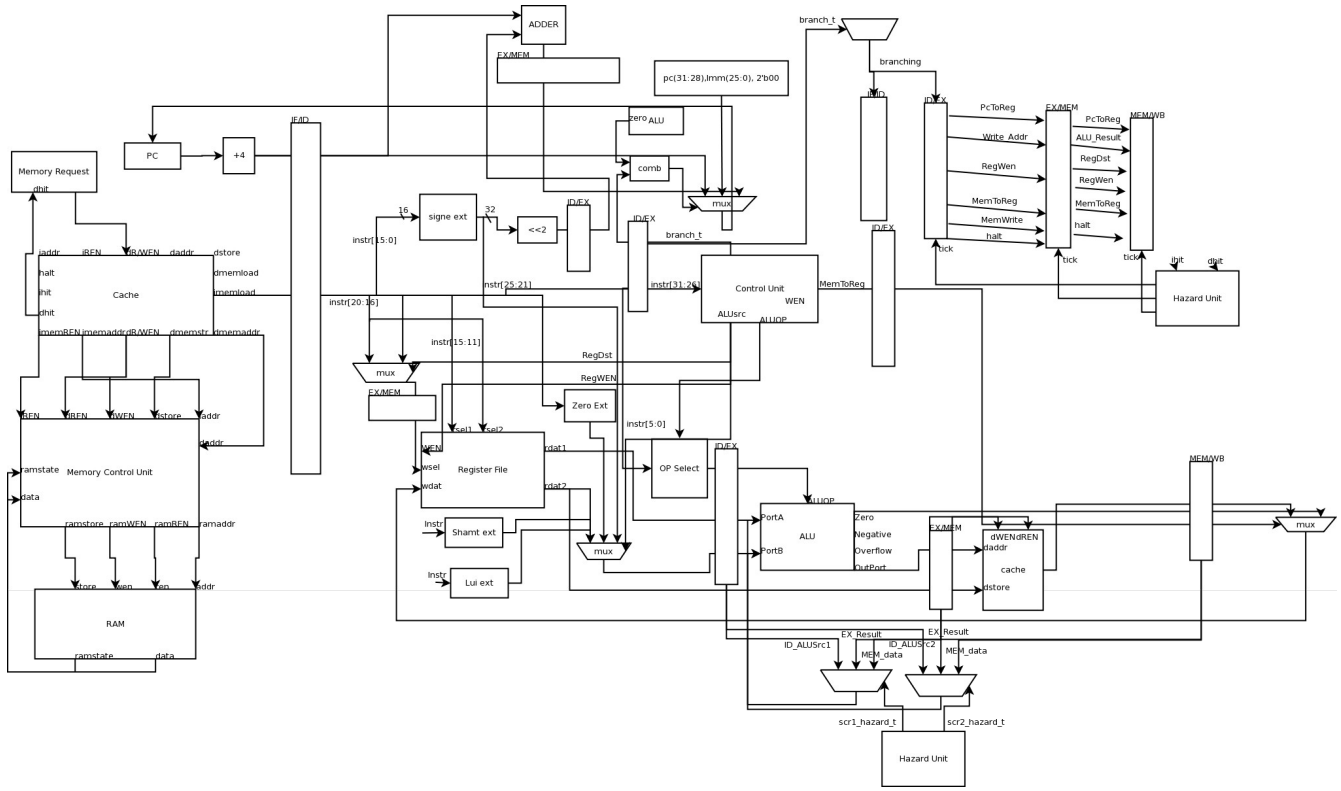

figure.2 Pipleline

Results

Test case: mergesort.asm

	SC(20ns)	PIPE(12ns)
FMAX	33.29	41.67
LAT	20ns	60ns
mips	1.03E+000	1.45E+000
setup slack	-6.765	-18.692
critical path	26.765	38.692
IPC	0.782	0.676
FPGA (regs)	1624	1311

Conclusions

The Pipelined design is significantly better than Single-cycle. The frequency for Piplelined design is higher than Single-cycle, but not a lot higher. The possible reason for that could be the combination logic part for branching. I may added some wasteful (unnecessary) logic gates without trying to optimize it. For the mips, Pipelined design is about 37% better than the Single-cycle design.

As space usage, Pipelined design uses more registers than the Single-cycle design since it uses lots of registers to split stages. The space is trade out for speed and I think it's a good trade since the FPGA board is big enough to hold the Pipelined design.