Rakesh Reddy Kachana

Email: rakeshkachana27@gmail.com**Phone**:+91-9177766875

CAREER OBJECTIVE

Self-motivated and hardworking fresher seeking for an opportunity to work in a challenging environment to prove my skills and utilize my knowledge & intelligence in the growth of organization.

EDUCATIONAL CREDENTIALS

- **Master of Science in Information Technology(MSIT)** 2013-2015
  IIIT-Hyderabad **7.25 CGPA**
- **B-Tech (ECE)** 2008-2012
  Yogi Vemana University **7.5 CGPA**
- **Intermediate (MPC)** 2006-2008
  Sir Rabindranath Tagore junior college **82.50%**
- **SSC** 2005-2006
  Keshava Reddy (E.M) High School, Panyam **79.33%**

TECHNICAL SKILLS

- **Programming Languages:** C, JAVA
- **Operating Systems:** UNIX, Windows
- **Networking:** HTML, JSP, JavaScript
- **Databases:** MySQL
- **Server:** Apache Tomcat 7.0
- **Framework:** Android

STRENGTHS

- Ability to grasp the new skills quickly
- Excellent knowledge of Core subjects
- Coordination
- Hardworking

GRADUATION PROJECT

Internship ***TARA MOBILE TECHNOLOGIES***

Worked under guidance of Prof. Raj Reddy as researcher for Personal Activity Recognition using smart phone sensors in Android platform.

Duration: 3 months

COURSE PROJECTS

C projects

- Store Management System - *using file system*

Java Projects

- Pay Pal System - *using file system*
- Mini Google Search Engine - *using data structures, web crawler*
- Low Fair Routing System - *using Dijkstra's algorithm*
- Employee Pay Role System - *using MySQL Database*

Network Projects

- Online Chess Game - *using Jsp, HTML, Ajax, JavaScript , Tomcat 7.0*
- Download Manager - *using java, Socket programming*

UNDER GRADUATION PROJECT

Title: Radix-4 based high speed multiplier for ALU'S using minimal partial products

Description: A high speed and high performance parallel complex number multiplier.Designs are structured using Radix-4 Modified Booth Algorithm and Wallace tree. These two techniques are employed to speed up the multiplication process as their capability to reduce partial products generation and compress partial product term by a ratio of 3:2. The system has been designed efficiently using VHDL codes for 8x8-bit signed numbers and successfully simulated and synthesized using Xilinx.

Team Size: 4
Duration: 3 months

EXTRA CIRCULARS

- Presented a paper on "**SILENT SOUND TECHNOLOGY**" **ELOQUENCE-*11***national level student technicalsymposium at SREE VIDYANIKETHAN ENGINEERING COLLEGE.
- Presented a paper on "**HAND GESTURE RECOGNITION**" ***ELICITE 2K11*** national level student technical symposium at K.S.R.M COLLEGE OF ENGINEERING.
- Presented a paper on "**Augmentation Of Network Routing Protocols**"in ***YOGI-TECH 2K12***
- **SECRETARYFOR COLLEGE ALUMNI** for the year 2012-13.

DECLARATION

I do here by confirm that the information given in this form is true to do the best of my knowledge and belief.

Date:
Place:

(RAKESH REDDY KACHANA)