Uniprocessor Virtual Memory without TLBs

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The paper is about a study done on the performance of a uniporcessor system that achieves virtual memory without specific harwarde componenets. *The paper was written to explore the performance gains (and losses) of such a system. One major benefit is increased flexibility over hardware state machines.* The paper used simulated memory management systems to measure the perforance of both traditional hardware-based TLBs, and software-based TLBs.

The paper often refers to acronyms that are introduced formally the first time. When jumping around the paper, it can be difficult to know what an acronym stands for. A table of acronyms and their meanings would be helpful for readers to quickly reference. Table 1 refers to an 'I-Side' and 'D-Side', and an 'I-TLB' and 'D-TLB' respectively, though it is not clear what these terms mean.