

IUST
Iran University of
Science and Technology

Department of
Computer Engineering

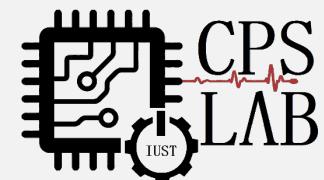
Computer Architecture Laboratory

INTRODUCTION

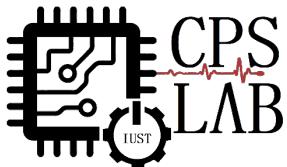
Lecturer: Ali Javadi

Javadi_ali@comp.iust.ac.ir

1st session

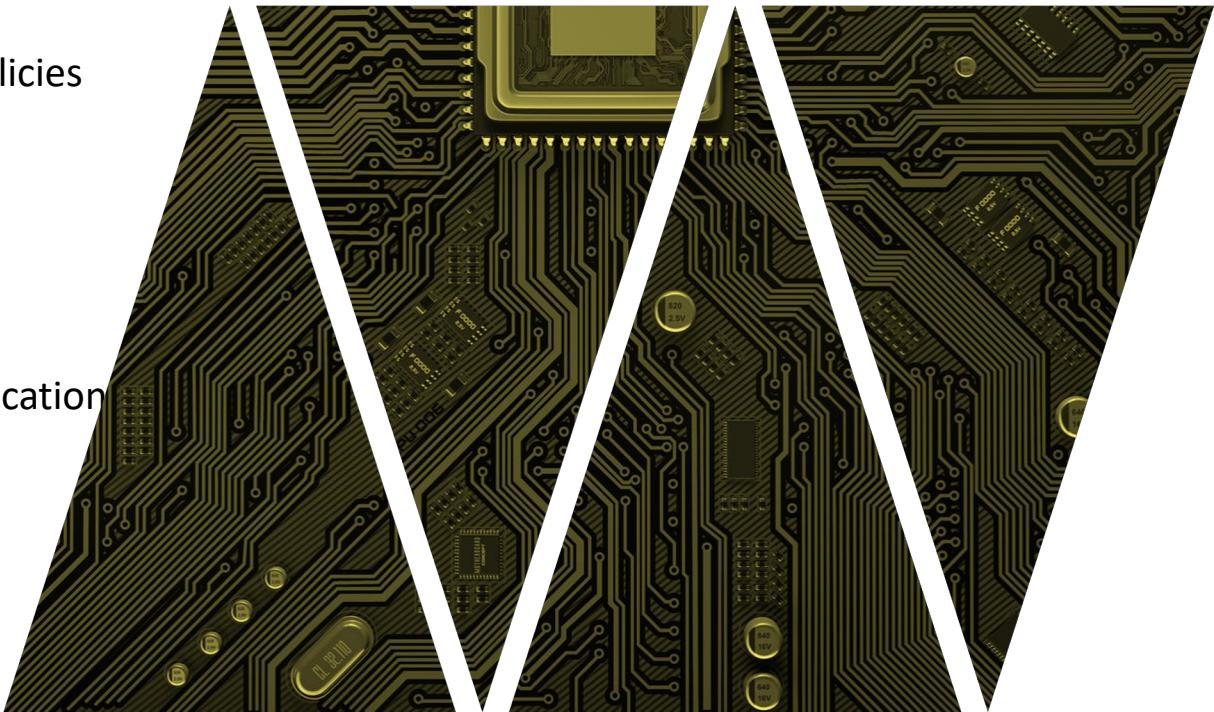
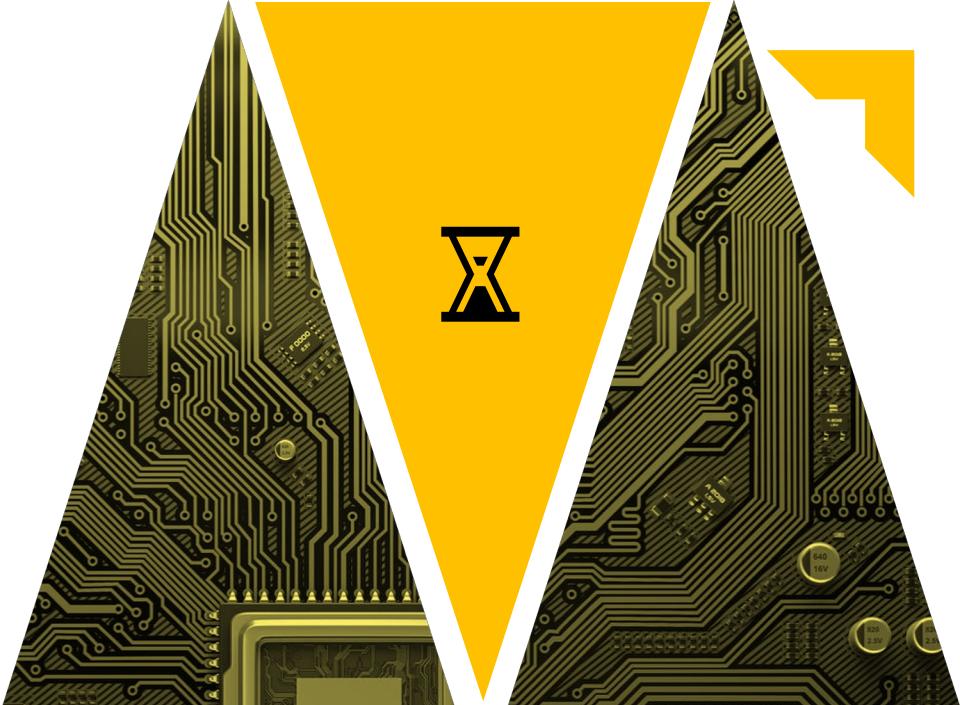


Cyber-Physical Systems Laboratory



Overview

- Introduction
 - Meeting the Lecturer
 - Students Self-Intro
- Teaching Philosophy
 - Expectations and Policies
 - Grouping
 - Grading
- Course outline
 - History
 - Technologies Classification
 - HDL Intro



Meeting the Lecturer

Ali Javadi

PhD Student (Computer Architecture)

Research Interests:

- Fog *Computing Infrastructures*
- Internet of things
- Embedded systems
- *Low-power design*
- *Fault-tolerant systems design*
- Reinforcement learning



Students

Self-Introduction

- Name
- Background
 - Educational Background
 - Previous Degrees or Institutions Attended
- Interest
- Experience
 - Relevant Work Experience or Internships
- Goals



Expectations and Policies

- Attendance
- Arriving on Time
- Participation
- Assignments Submission
 - Deadline
 - Preferred File Formats
- Academic Integrity
- Honesty
- Consequence of Plagiarism and Cheating



Grouping

- Purpose of Grouping
- Group Formation
 - Groups of Two Persons
- Student Preferences



Grading

- Grading scale
 - Numerical grades (out of 100)
 - Experiments 60%
 - Report
 - Synthesizable Code
 - Team Work
 - Simulation/Origination Result
 - Final Project 20%
 - Final Exam 20%
 - Participation 10% (Additional Score)



History



The Rammig Machine

1959

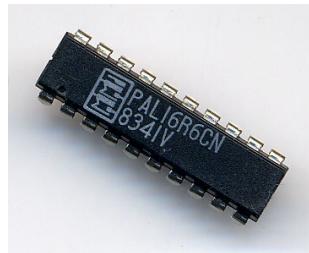
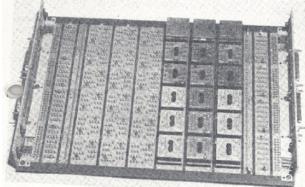
1977

1977

1980

1980

The Estrin Fix-plus
machine



PLDs

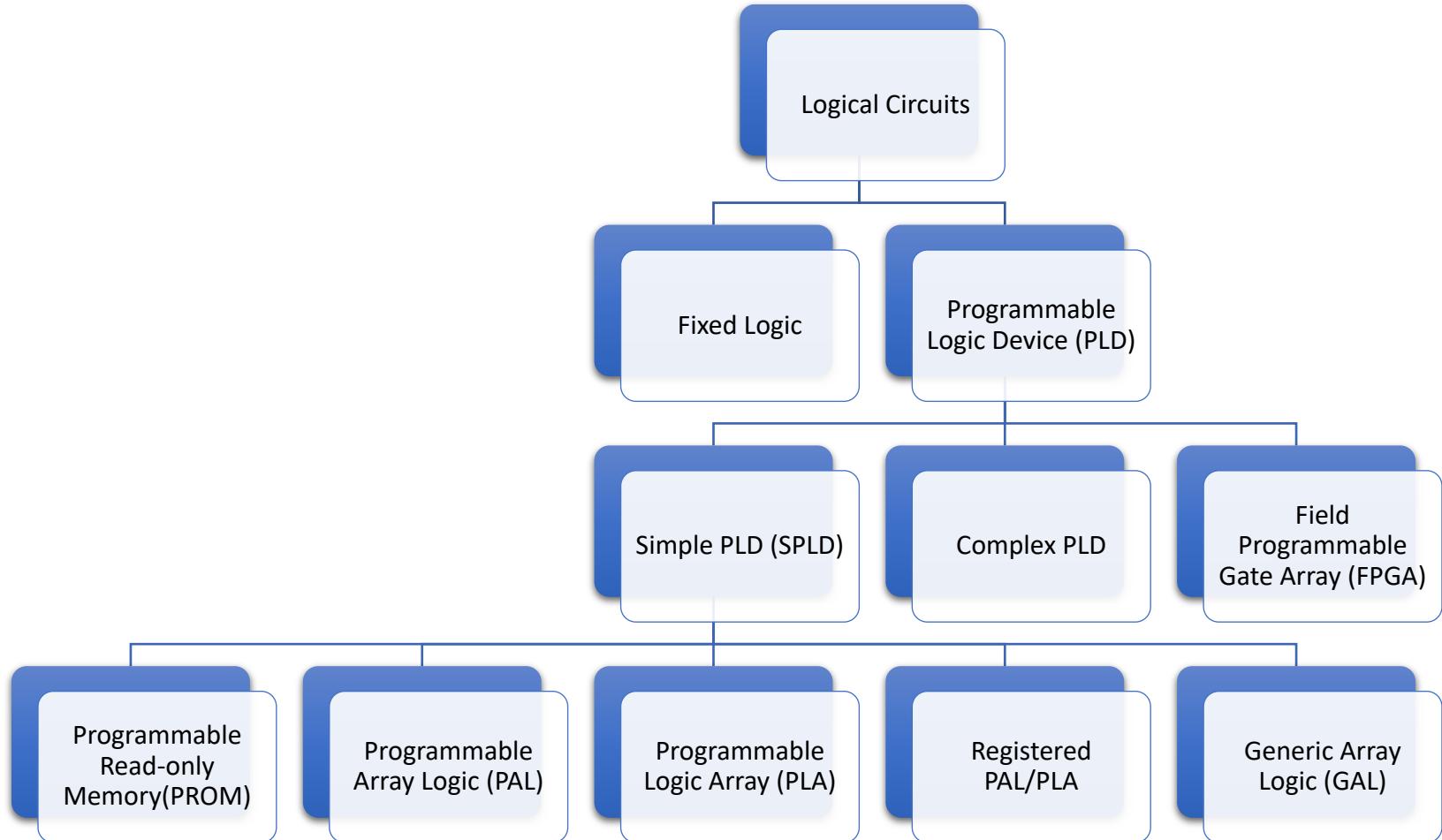


FPGA

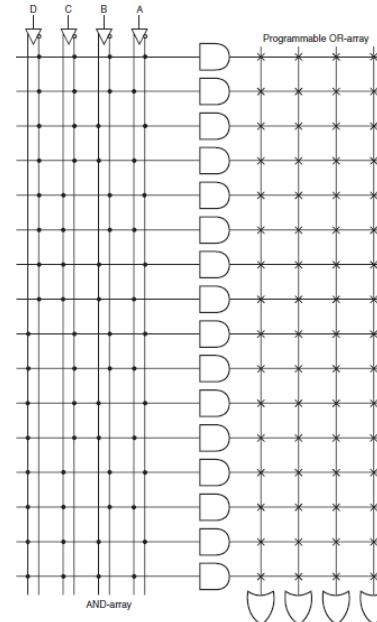
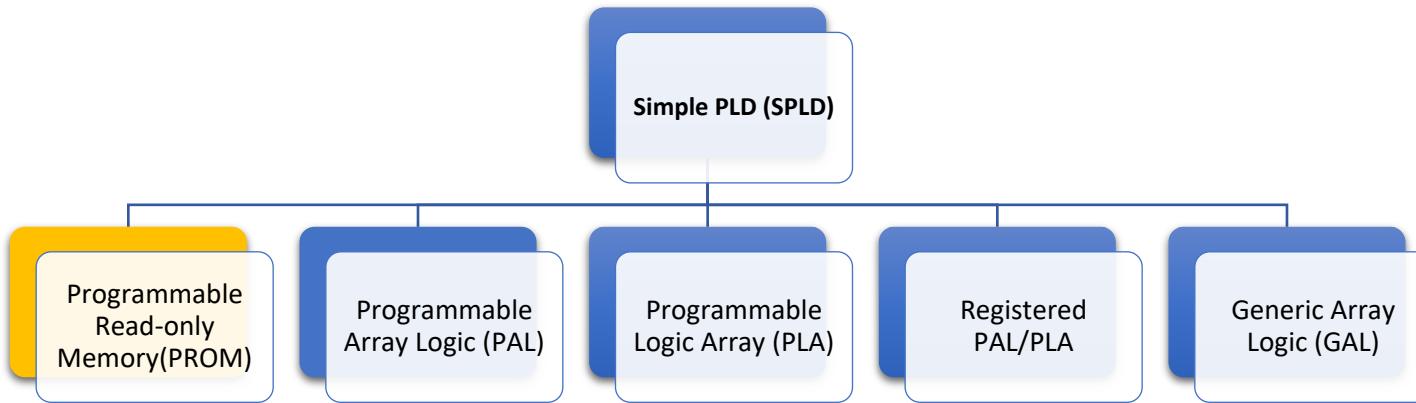


CPLDs

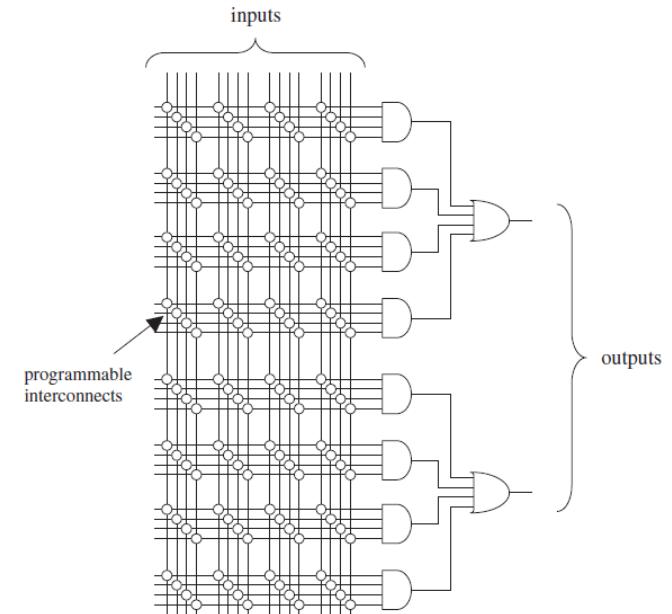
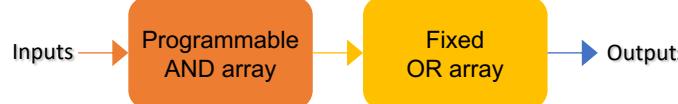
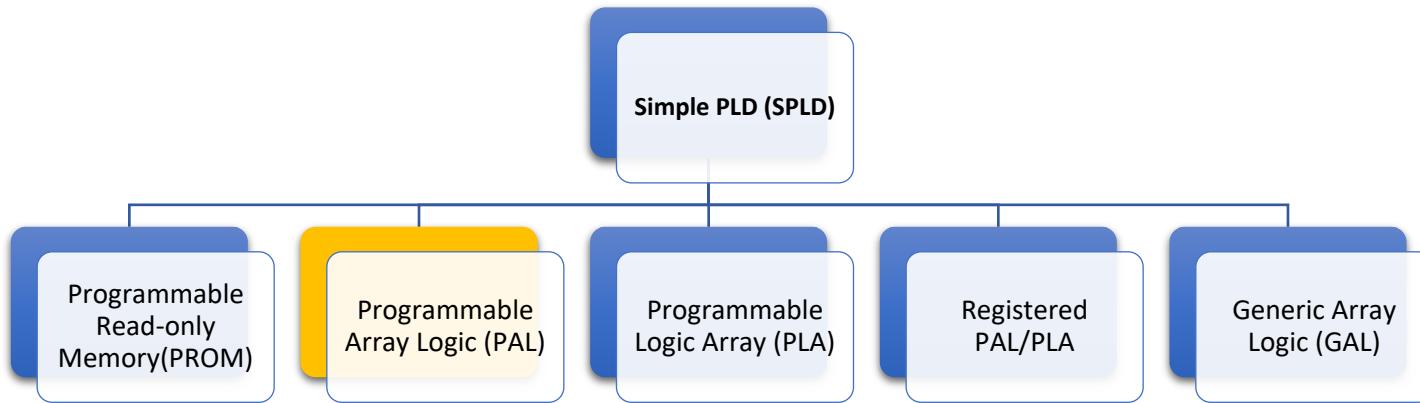
Technologies Classification



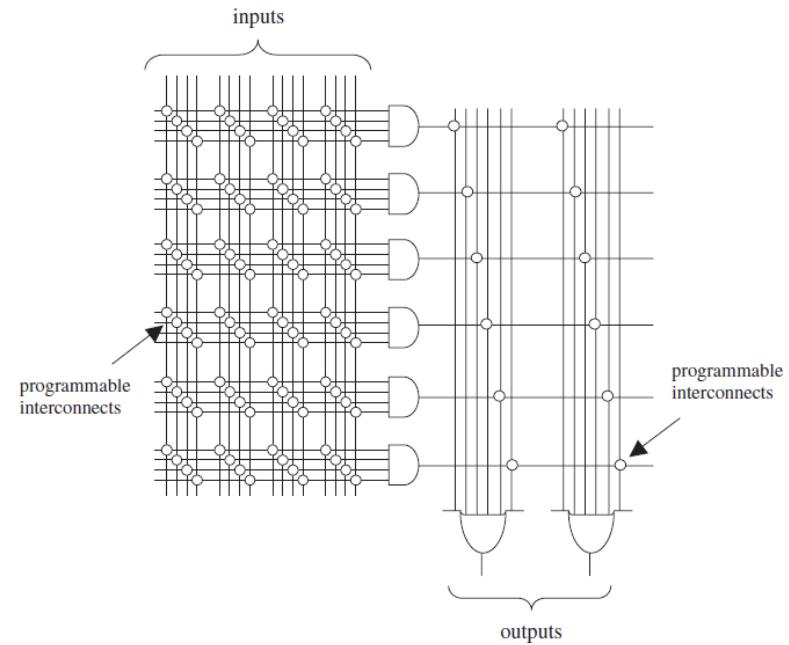
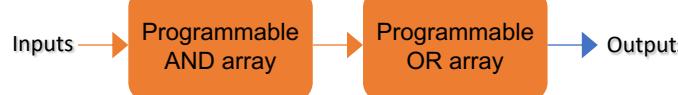
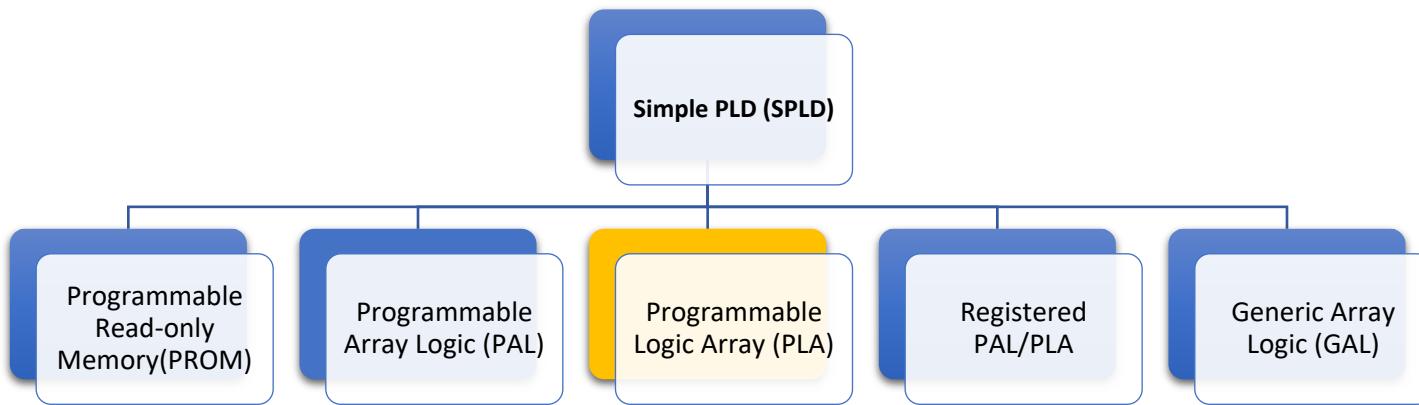
Technologies Classification



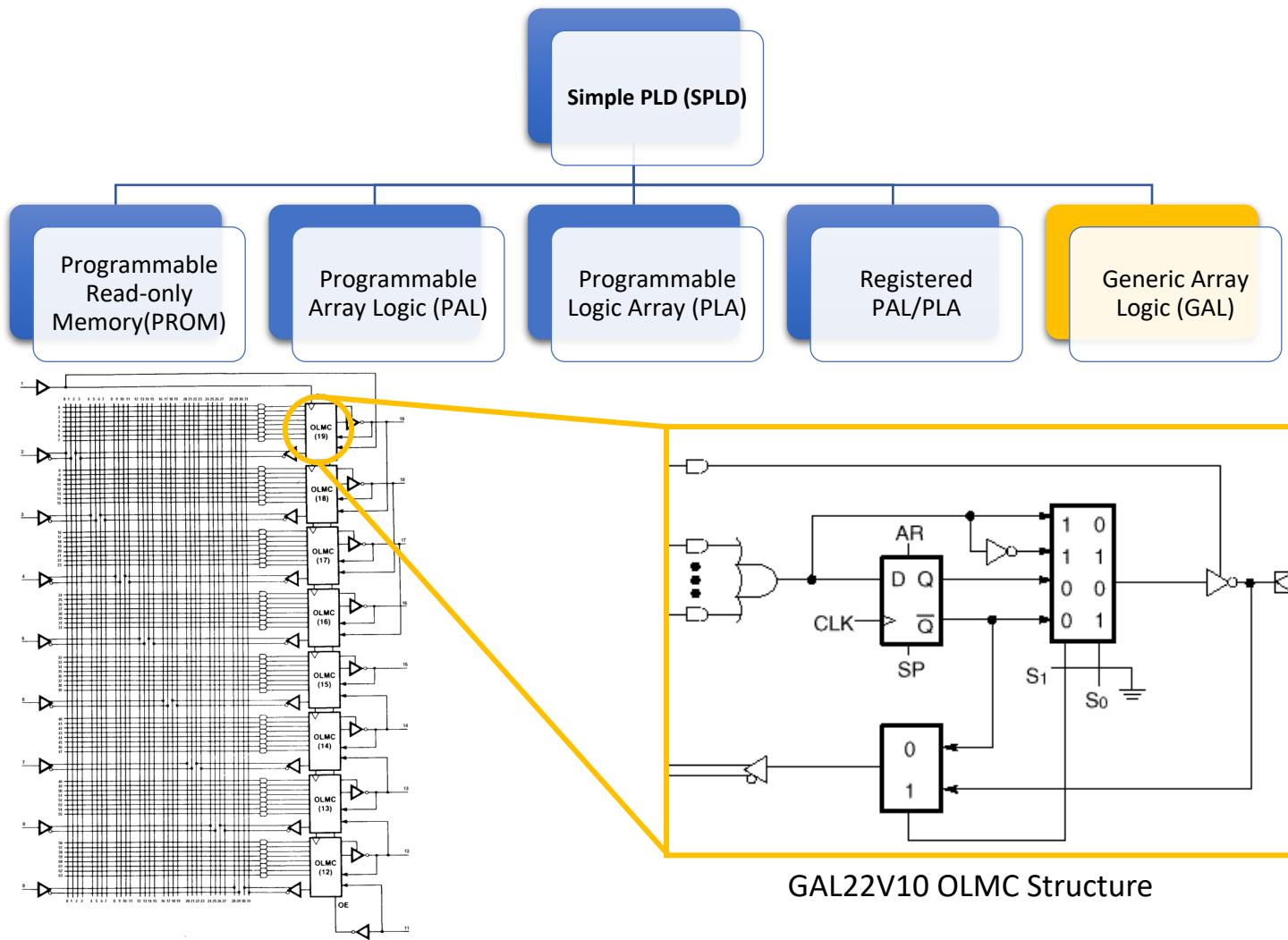
Technologies Classification



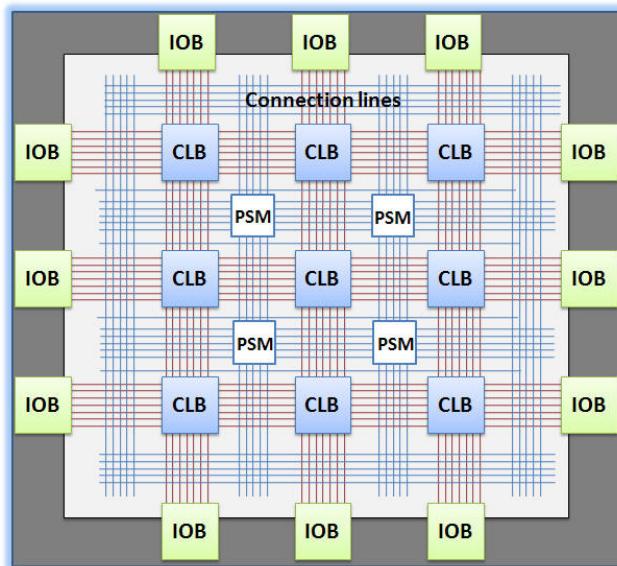
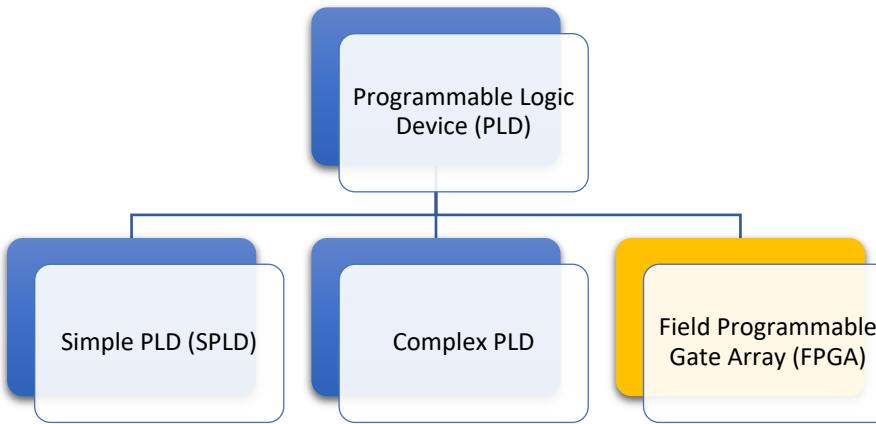
Technologies Classification



Technologies Classification



Technologies Classification

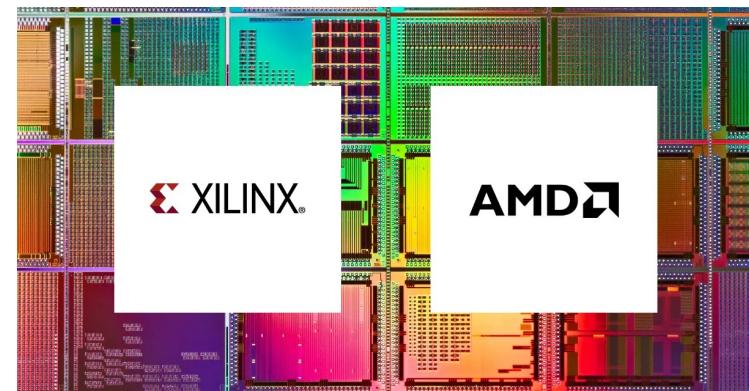


IOB
Input Output Block

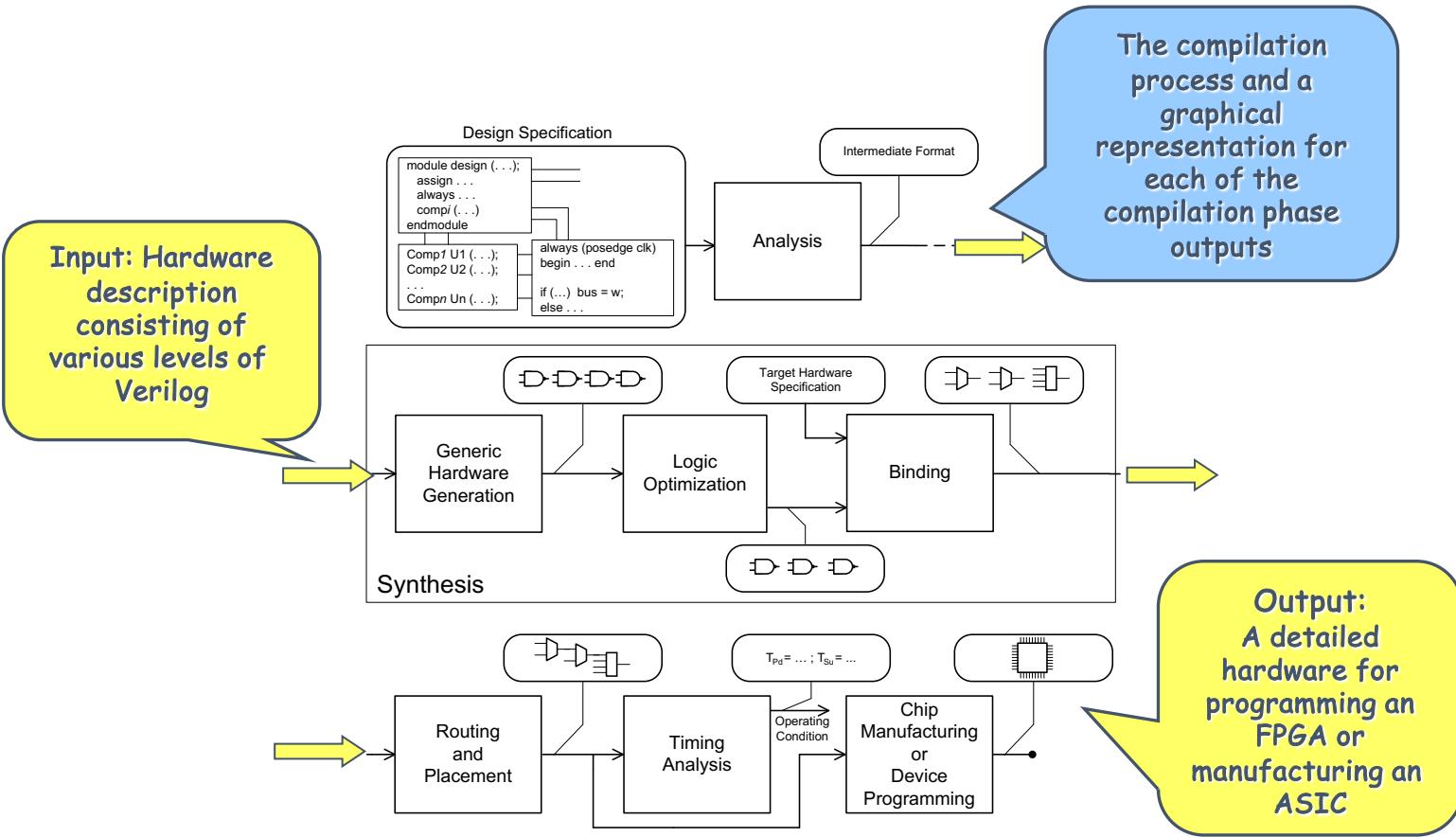
CLB
Configurable Logic Block

PSM
Programmable Switch Matrix

Connection lines
Single, Long
Double, Direct



Technologies Classification



Hardware Description Language (HDL)

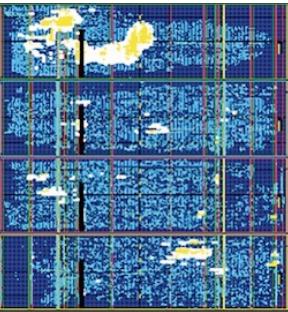
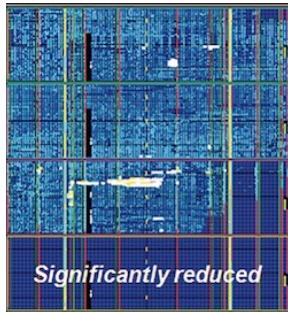
| VHDL | Verilog |
|---|---|
| Commissioned in 1981 by Department of Defense; now an IEEE standard | Created by Gateway Design Automation in 1985; now an IEEE standard |
| Initially created for ASIC synthesis | Initially an interpreted language for gate-level simulation |
| Strongly typed; Potential for verbose code | Less explicit typing (e.g. Compiler will pad arguments of different widths) |
| Strong support for package management and large designs | No special extensions for large designs |

CAD Tools



ISE Design Suite 14.7

ISE™ design suite supports the Spartan™ 6, Virtex™ 6, and CoolRunner™ devices, as well as their previous generation families.

| | ISE | Vivado |
|----------------------------|---|---|
| P&R Runtime | 13 hrs. | 5hrs. |
| Memory Usage | 16 GB | 9GB |
| Wire Length and Congestion |  |  <i>Significantly reduced</i> |

std_logic type

- U** uninitialized. This signal hasn't been set yet.
- X** unknown. Impossible to determine this value/result.
- 0** logic 0
- 1** logic 1
- Z** High Impedance
- W** Weak signal, can't tell if it should be 0 or 1.
- L** Weak signal that should probably go to 0
- H** Weak signal that should probably go to 1
- Don't care.

VHDL Architecture

Architecture behavioral of adder is

```
... //Declaration
```

```
begin
```

```
...
```

```
process
```

```
begin
```

```
...
```

```
//Sequential
```

```
end process;
```

```
...
```

```
//Concurrent
```

```
end Architecture;
```

VHDL Operators

- **miscellaneous operators**
 - ****** exponentiation
 - **abs** absolute value
 - **not** complement
- **multiplying operators**
 - ***** multiplication
 - **/** division
 - **mod** modulo
 - **rem** remainder
- **sign operators**
 - **+** unary plus
 - **-** unary minus
- **adding operators**
 - **+** addition
 - **-** subtraction
 - **&** concatenation

VHDL Operators (Cont.)

- **Shift Operator**
 - **sll** shift left logical
 - **srl** shift right logical
 - **sla** shift left arithmetic
 - **sra** shift right arithmetic
 - **rol** rotate left
 - **ror** rotate right
- **Relational Operator**
 - **=** test for equality
 - **/=** test for inequality
 - **<** test for less than
 - **<=** test for less than or equal
 - **>** test for greater than
 - **>=** test for greater than or equal

VHDL Operators (Cont.)

- **Logical Operator**
 - **and** logical and
 - **or** logical or
 - **nand** logical complement of and
 - **nor** logical complement of or
 - **xor** logical exclusive or
 - **xnor** logical complement of exclusive or



Cyber-Physical Systems Laboratory

THANK YOU

Cyber-Physical Systems Laboratory

 cps.iust.ac.ir

 +98 (21) 73225350

 Javadi_ali@comp.iust.ac.ir



Room 120, Department of Computer Engineering, Iran University of Science and Technology, University Road, Hengam Street, Resalat Square, Narmak, Tehran, IRAN 16846-13114.