```vhdl
entity ALU_4bit is
  Port (
    A, B : in std_logic_vector(3 downto 0);
    Sel : in std_logic_vector(1 downto 0);
    Y   : out std_logic_vector(3 downto 0)
  );
end ALU_4bit;


architecture Behavioral of ALU_4bit is
  constant DELAY : time := 10 ns;
begin
  process(A, B, Sel)
    variable result : std_logic_vector(3 downto 0);
  begin
    case Sel is
      when "00" =>  -- Increment
        Y <= std_logic_vector(unsigned(A) + 1) after DELAY;
      when "01" =>  -- Subtract
        Y <= std_logic_vector(unsigned(A) - unsigned(B)) after DELAY;
      when "11" =>  -- Multiply
        Y <= std_logic_vector(unsigned(A) * unsigned(B))(3 downto 0);
      when others =>
        null;
    end case;
  end process;


  -- Concurrent NAND
  Y <= A nand B when Sel = "10";
end Behavioral;
```