



Just Verification of Mutual Exclusion Algorithms

Rob van Glabbeek, Bas Luttik, and Myrthe Spronck

28 August 2025

Mutual exclusion

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The problem

- $N \geq 2$ threads, code divided in *critical* and *non-critical* sections
- Leaving non-critical section is optional

Algorithm Mutex

repeat

 non-critical section

 critical section

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Properties

- Mutual exclusion
- Deadlock freedom
- Starvation freedom

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entry protocol

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~~$T_i \wedge T_j$~~ →

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T_i leaves non-critical section \rightarrow eventually T_i enters critical section

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T_i ↘ non-critical section
entry protocol
critical section ↙ T_i
exit protocol

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Verification

Goal: verify many mutual exclusion algorithms

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Method: model checking with mCRL2

- Model algorithms and environment in process-algebra
- Capture properties in modal μ -calculus

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Verification

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- Model algorithms and environment in process-algebra
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Abstraction leads to unrealistic executions → must disregard

Which?

Example: starvation freedom violation of Dekker's algorithm

Example violation

Algorithm Dekker's for T_0

```
1: non-critical section
2:  $flag[0] \leftarrow 1$ 
3: while  $flag[1] = 1$  do
4:   if  $turn = 1$  then
5:      $flag[0] \leftarrow 0$ 
6:     await  $turn = 0$ 
7:    $flag[0] \leftarrow 1$ 
8: critical section
9:  $turn \leftarrow 1$ 
10:  $flag[0] \leftarrow 0$ 
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$flag[0] = 0$
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Algorithm Dekker's for T_1

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Example violation

Is this execution realistic?

Example violation

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It depends on our *memory model*

Example violation

Is this execution realistic?

It depends on our *memory model*

Goal: verify many mutual exclusion algorithms under **6 different memory models**

Memory models

Memory models

Memory: only read/write registers

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Memory model

- Operations *blocking* each other
- Register behaviour when operations *overlap*

Memory models

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- ~~weak memory models, caching, operation reordering, etc.~~

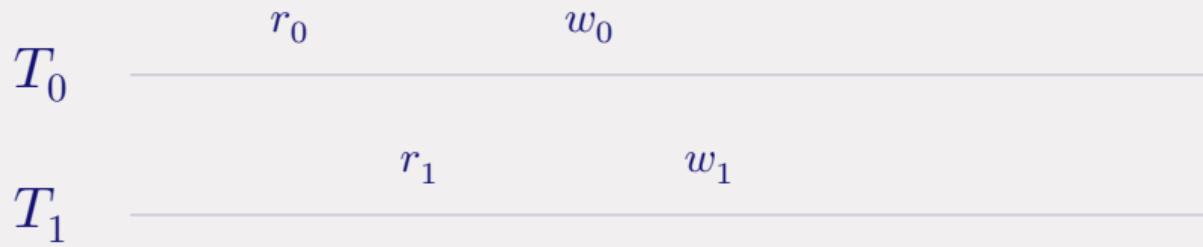
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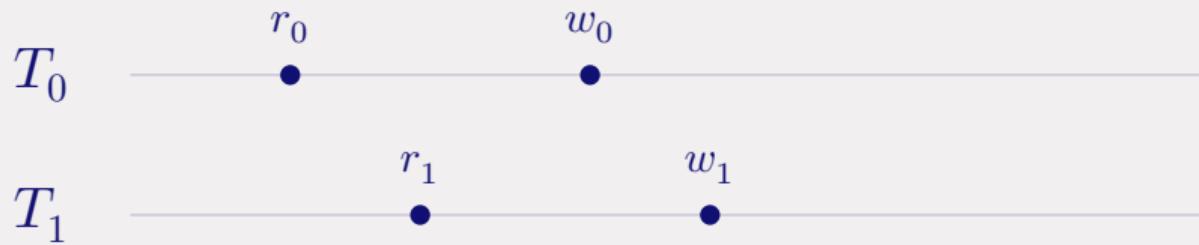
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Memory models - blocking



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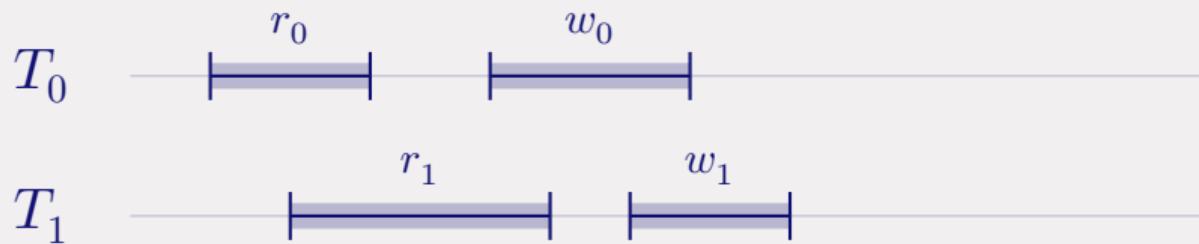
Original problem assumes *atomicity*: operations cannot overlap



Memory models - blocking

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Operations have *duration*

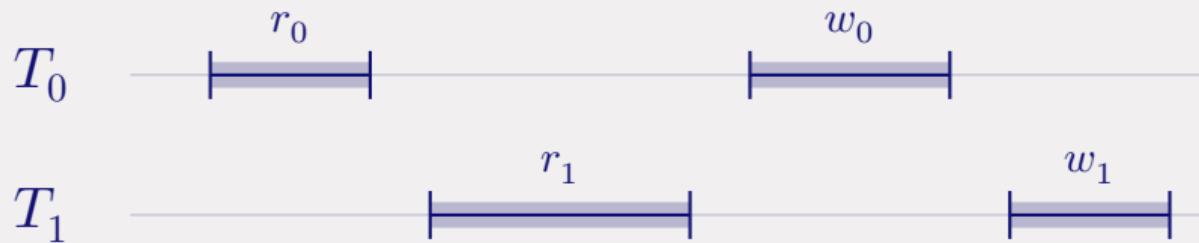


Memory models - blocking

Original problem assumes *atomicity*: operations cannot overlap

Operations have *duration*

Duration + no overlap = operations **block** each other



Memory models - blocking

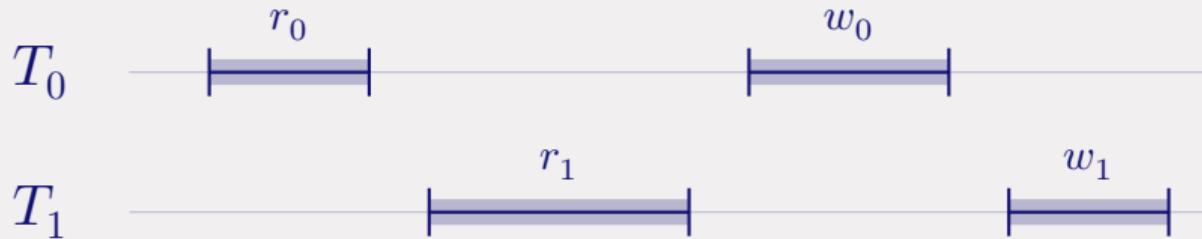
4 reasonable views on blocking

- 1.
- 2.
- 3.
- 4.

Memory models - blocking

4 reasonable views on blocking

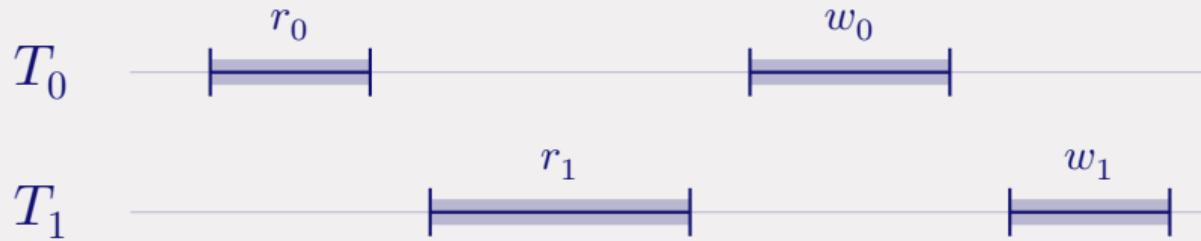
- 1.
- 2.
- 3.
4. Atomicity assumption: no overlap at all



Memory models - blocking

4 reasonable views on blocking

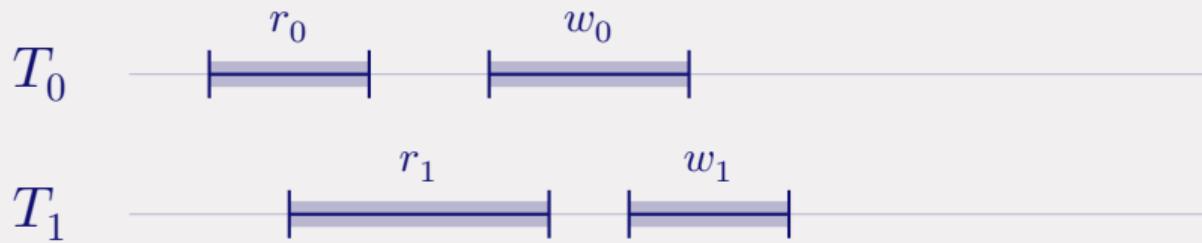
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4. **Blocking reads and writes**



Memory models - blocking

4 reasonable views on blocking

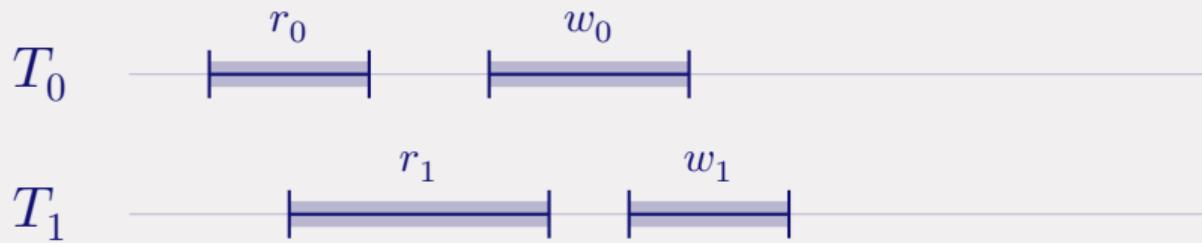
1. Drop the atomicity assumption: all overlap allowed
- 2.
- 3.
4. **Blocking reads and writes**



Memory models - blocking

4 reasonable views on blocking

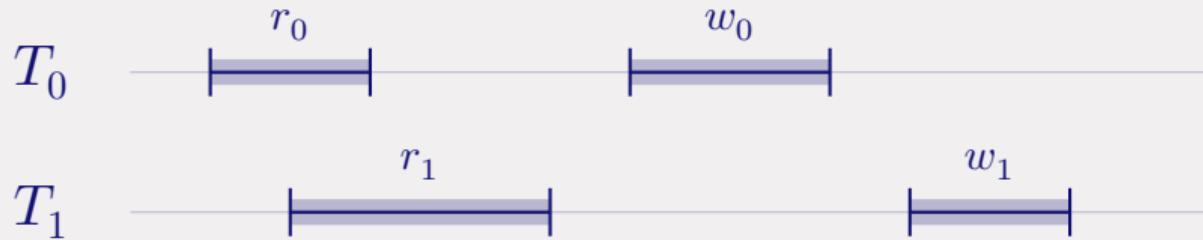
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Memory models - blocking

4 reasonable views on blocking

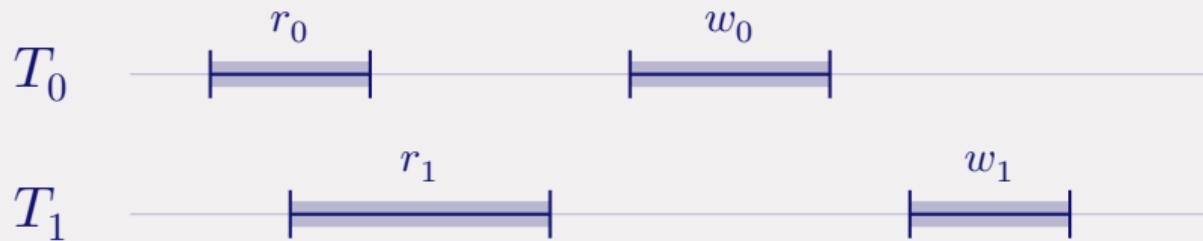
1. **Non-blocking reads and writes**
2. Writes cannot overlap anything + prioritize writes
3. Writes cannot overlap anything
4. **Blocking reads and writes**



Memory models - blocking

4 reasonable views on blocking

1. Non-blocking reads and writes
2. Blocking writes and non-blocking reads
3. Blocking model with concurrent reads
4. Blocking reads and writes



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Memory models - blocking

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	r block $r'?$	r block $w?$	w block $r?$	w block $w'?$
1	X	X	X	X
2	X	X	✓	✓
3	X	✓	✓	✓
4	✓	✓	✓	✓

Memory models - overlap

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Behaviour in case of overlap

- Based on Lamport's work

safe registers
regular registers
atomic registers

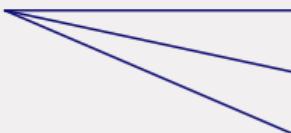
Memory models - overlap

Behaviour in case of overlap

- Based on Lamport's work
- Only overlapping writes matter

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blocking writes and non-blocking reads
blocking model with concurrent reads
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Memory models - overlap

Behaviour in case of overlap

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Modelling memory models

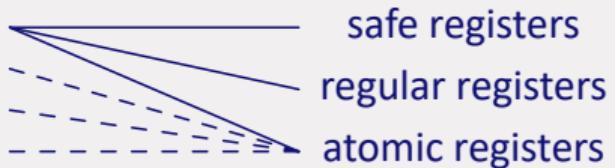
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The diagram illustrates the mapping of four memory models to three types of registers. Four arrows originate from the text on the left and point to the right. The first arrow (solid line) points to 'safe registers'. The second arrow (dashed line) points to 'regular registers'. The third arrow (dash-dot line) points to 'atomic registers'. The fourth arrow (long dashed line) points to 'atomic registers'.

safe registers
regular registers
atomic registers
atomic registers

Modelling memory models

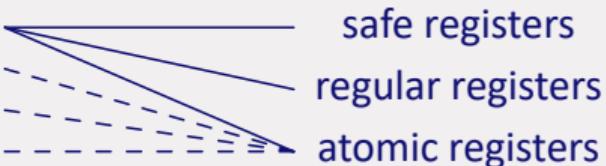
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Capture in two dimensions:

Modelling memory models

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Capture in two dimensions:

- Register types via models

Process-Algebraic Models of Multi-Writer Multi-Reader Non-Atomic Registers

Myrthe S. C. Spronck 

Eindhoven University of Technology, The Netherlands

Bas Luttik 

Eindhoven University of Technology, The Netherlands

Abstract

We present process-algebraic models of multi-writer multi-reader safe, regular and atomic registers. We establish the relationship between our models and alternative versions presented in the literature. We use our models to formally analyse by model checking to what extent several well-known mutual exclusion algorithms are robust for relaxed atomicity requirements. Our analyses refute correctness

Modelling memory models

non-blocking reads and writes
blocking writes and non-blocking reads
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Capture in two dimensions:

- Register types via models
- Blocking behaviour via formulas

Blocking in formulas

Leverage the *justness* assumption

Completeness criteria: disregard “incomplete” executions

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Justness: an enabled event must eventually occur or be “interfered with”

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Depends on a *concurrency relation* \curvearrowright

- Encodes knowledge of real system
- Interference given by $\not\curvearrowright$

Blocking in formulas

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- Interference \approx blocking

Blocking via concurrency relation

Blocking via concurrency relation

	r block r' ?	r block w ?	w block r ?	w block w' ?
1	X	X	X	X
2	X	X	✓	✓
3	X	✓	✓	✓
4	✓	✓	✓	✓

Blocking via concurrency relation

	$r' \not\sim r?$	$w \not\sim r?$	$r \not\sim w?$	$w' \not\sim w?$
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Incorporate justness + concurrency relations into formulas

Blocking via concurrency relation

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Incorporate justness + concurrency relations into formulas

Progress, Justness and Fairness in Modal μ -Calculus Formulae

Myrthe S. C. Spronck 

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Bas Luttik 

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Tim A. C. Willemse 

Eindhoven University of Technology, The Netherlands

Results - Dekker's algorithm

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<i>Algorithm</i>	<i># threads</i>	<i>Safe</i>	<i>Regular</i>	<i>Atomic</i>		
		\curvearrowleft_1	\curvearrowleft_1	\curvearrowleft_1	\curvearrowleft_2	\curvearrowleft_3
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
Dekker	2	M	M	S	D/S	M
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots

Results - Dekker's algorithm

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		\curvearrowleft_1	\curvearrowleft_1	\curvearrowleft_1	\curvearrowleft_2	\curvearrowleft_3	\curvearrowleft_4
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Starvation freedom counterexample

- Recall: repeated writes prevent read

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Starvation freedom counterexample

- Recall: repeated writes prevent read
- Easily fixed

Results - full

Algorithm	# threads	Safe	Regular	Atomic			
		• ₁	• ₁	• ₁	• ₂	• ₃	• ₄
Anderson	2	S	S	S	S	M	M
Aravind BLRU	3	S	S	S	M/S	M	M
Attiya-Welch (orig.)	2	D/S	S	S	D	M	M
Attiya-Welch (var.)	2	M/S	M/S	S	D	M	M
Burns-Lynch	3	D	D	D	D	M	M
Dekker	2	M	M	S	D/S	M	M
Dekker RW-safe	2	S	S	S	D	M	M
Dekker RW-safe (DFtoSF)	2	S	S	S	S	M	M
Dijkstra	3	M	D	D	M	M	M
Kessels	2	X	X	S	S	M	M
Knuth	3	M	S	S	M	M	M
Lamport 1-bit	3	D	D	D	D	M	M
Lamport 1-bit (DFtoSF)	3	S	S	S	S	M	M
Lamport 3-bit	3	S	S	S	S	M	M
Peterson	2	X	X	S	S	M	M
Szymanski flag (int.)	3	X	X	S	S	M	M
Szymanski flag (bit)	3	X	X	X	X	X	X
Szymanski 3-bit lin. wait	3/2	X/S	X/S	X/S	X/S	X/M	X/M

Conclusion

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Contributions

- 4 blocking behaviours captured
- Many mutual exclusion algorithms verified
 - 3 properties
 - 6 memory models

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Future work

- Other properties, e.g. bounded bypass
- Impact of busy waiting
- Arbitrary numbers of threads?



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(Im)possibility of liveness

Starvation freedom is *impossible* with I and A

- Reads interfere with writes
- Observation made previously
- In short: repeated reads prevent communicating interest

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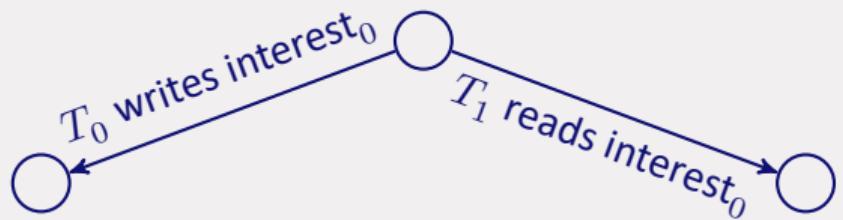
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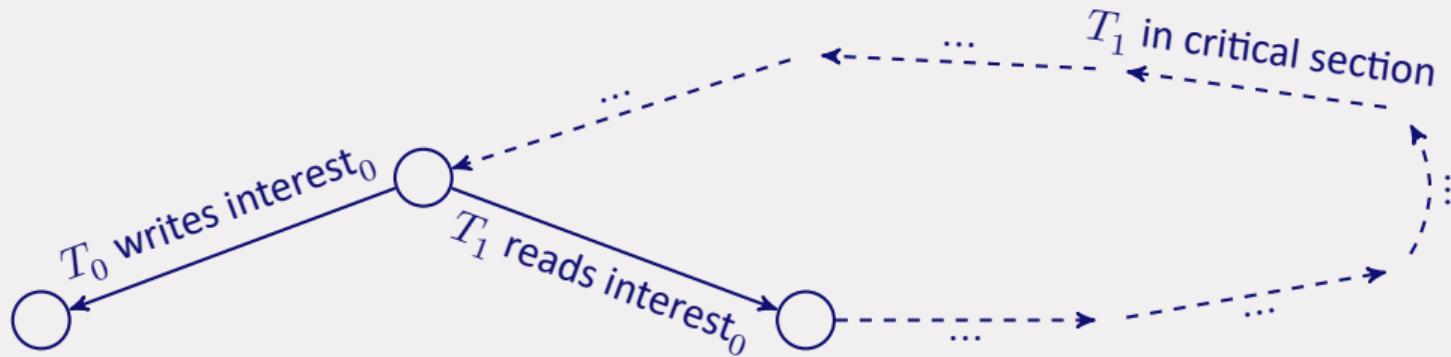
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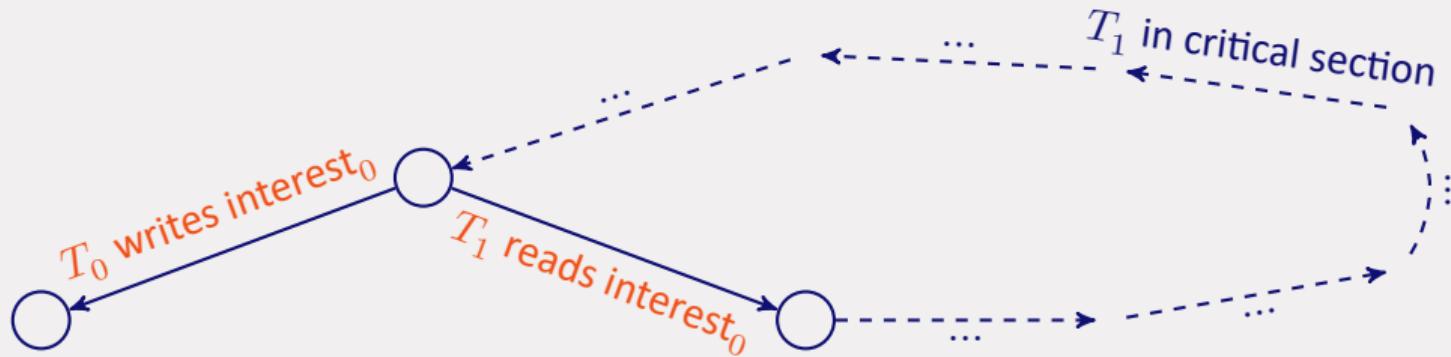
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Deadlock freedom *always observed to be violated* with I and A

- Might not be impossible
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- Both stuck in entry or one stuck in exit

Algorithm Peterson's algorithm

- 1: $flag[i] \leftarrow true$
 - 2: $turn \leftarrow i$
 - 3: **await** $flag[j] = false \vee turn = j$
 - 4: **critical section**
 - 5: $flag[i] \leftarrow false$
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An interesting violation

- Dekker with safe-T: M

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Algorithm Dekker's for T_0

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5:      $flag[0] \leftarrow 0$ 
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7:    $flag[1] \leftarrow 1$ 
8: critical section
9:  $turn \leftarrow 0$ 
10:  $flag[1] \leftarrow 0$ 
```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2:  $flag[0] \leftarrow 1$ 
3: while  $flag[1] = 1$  do
4:   if  $turn = 1$  then
5:      $flag[0] \leftarrow 0$ 
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9:  $turn \leftarrow 1$ 
10:  $flag[0] \leftarrow 0$ 
```

$flag[0] = 1$
 $flag[1] = 0$
 $turn = 0$

Algorithm Dekker's for T_1

```
1: non-critical section
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Algorithm Dekker's for T_1

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```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2:  $\text{flag}[0] \leftarrow 1$ 
3: while  $\text{flag}[1] = 1$  do
4:   if  $\text{turn} = 1$  then
5:      $\text{flag}[0] \leftarrow 0$ 
6:     await  $\text{turn} = 0$ 
7:    $\text{flag}[0] \leftarrow 1$ 
8: critical section
9:  $\text{turn} \leftarrow 1$ 
10:  $\text{flag}[0] \leftarrow 0$ 
```

$\text{flag}[0] = ?$

$\text{flag}[1] = 0$

$\text{turn} = 1$

new-old
inversion

old = 1

new = 0

Algorithm Dekker's for T_1

```
1: non-critical section
2:  $\text{flag}[1] \leftarrow 1$ 
3: while  $\text{flag}[0] = 1$  do
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```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2: flag[0] ← 1
3: while flag[1] = 1 do
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6:     await turn = 0
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8: critical section
9: turn ← 1
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```

flag[0] = ?

flag[1] = 1

turn = 1

new-old
inversion

old = 1

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Algorithm Dekker's for T_1

```
1: non-critical section
2: flag[1] ← 1
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An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2: flag[0] ← 1
3: while flag[1] = 1 do
4:   if turn = 1 then
5:     flag[0] ← 0
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7:   flag[0] ← 1
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9: turn ← 1
10: flag[0] ← 0
```

flag[0] = ?

flag[1] = 1

turn = 1

new-old
inversion

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Algorithm Dekker's for T_1

```
1: non-critical section
2: flag[1] ← 1
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An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

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Algorithm Dekker's for T_1

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An interesting violation

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Algorithm Dekker's for T_0

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new-old
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Algorithm Dekker's for T_1

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- Dekker with safe-T: M

Algorithm Dekker's for T_0

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$flag[1] = 0$

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new-old
inversion

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Algorithm Dekker's for T_1

```
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An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2:  $flag[0] \leftarrow 1$ 
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```

$flag[0] = ?$

$flag[1] = 0$

$turn = 0$

new-old
inversion

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Algorithm Dekker's for T_1

```
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10:  $flag[1] \leftarrow 0$ 
```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2: flag[0] ← 1
3: while flag[1] = 1 do
4:   if turn = 1 then
5:     flag[0] ← 0
6:     await turn = 0
7:     flag[0] ← 1
8: critical section
9: turn ← 1
10: flag[0] ← 0
```

flag[0] = ?

flag[1] = 1

turn = 0

new-old
inversion

old = 1

new = 0

Algorithm Dekker's for T_1

```
1: non-critical section
2: flag[1] ← 1
3: while flag[0] = 1 do
4:   if turn = 0 then
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```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2: flag[0] ← 1
3: while flag[1] = 1 do
4:   if turn = 1 then
5:     flag[0] ← 0
6:     await turn = 0
7:     flag[0] ← 1
8: critical section
9: turn ← 1
10: flag[0] ← 0
```

flag[0] = ?

flag[1] = 1

turn = 0

new-old
inversion

old = 1

new = 0

Algorithm Dekker's for T_1

```
1: non-critical section
2: flag[1] ← 1
3: while flag[0] = 1 do
4:   if turn = 0 then
5:     flag[1] ← 0
6:     await turn = 1
7:     flag[1] ← 1
8: critical section
9: turn ← 0
10: flag[1] ← 0
```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2:  $flag[0] \leftarrow 1$ 
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9:  $turn \leftarrow 1$ 
10:  $flag[0] \leftarrow 0$ 
```

$flag[0] = ?$

$flag[1] = 1$

$turn = 0$

new-old
inversion

old = 1

new = 0

Algorithm Dekker's for T_1

```
1: non-critical section
2:  $flag[1] \leftarrow 1$ 
3: while  $flag[0] = 1$  do
4:   if  $turn = 0$  then
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6:     await  $turn = 1$ 
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9:  $turn \leftarrow 0$ 
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```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2: flag[0] ← 1
3: while flag[1] = 1 do
4:   if turn = 1 then
5:     flag[0] ← 0
6:     await turn = 0
7:   flag[0] ← 1
8: critical section
9: turn ← 1
10: flag[0] ← 0
```

flag[0] = ?

flag[1] = 0

turn = 0

new-old
inversion

old = 1

new = 0

Algorithm Dekker's for T_1

```
1: non-critical section
2: flag[1] ← 1
3: while flag[0] = 1 do
4:   if turn = 0 then
5:     flag[1] ← 0
6:     await turn = 1
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8: critical section
9: turn ← 0
10: flag[1] ← 0
```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2: flag[0] ← 1
3: while flag[1] = 1 do
4:   if turn = 1 then
5:     flag[0] ← 0
6:     await turn = 0
7:   flag[0] ← 1
8: critical section
9: turn ← 1
10: flag[0] ← 0
```

flag[0] = ?

flag[1] = 0

turn = 0

*new-old
inversion*

old = 1

new = 0

Algorithm Dekker's for T_1

```
1: non-critical section
2: flag[1] ← 1
3: while flag[0] = 1 do
4:   if turn = 0 then
5:     flag[1] ← 0
6:     await turn = 1
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8: critical section
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10: flag[1] ← 0
```

An interesting violation

- Dekker with safe-T: M

Algorithm Dekker's for T_0

```
1: non-critical section
2:  $flag[0] \leftarrow 1$ 
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9:  $turn \leftarrow 1$ 
10:  $flag[0] \leftarrow 0$ 
```

$flag[0] = 0$

$flag[1] = 0$

$turn = 0$

new-old
inversion

old = 1

new = 0

Algorithm Dekker's for T_1

```
1: non-critical section
2:  $flag[1] \leftarrow 1$ 
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7:    $flag[0] \leftarrow 1$ 
8: critical section
9:  $turn \leftarrow 1$ 
10:  $flag[0] \leftarrow 0$ 
```

$flag[0] = 0$

$flag[1] = 0$

$turn = 0$

new-old
inversion

old = 1

new = 0

infinite

non-critical

Algorithm Dekker's for T_1

```
1: non-critical section
2:  $flag[1] \leftarrow 1$ 
3: while  $flag[0] = 1$  do
4:   if  $turn = 0$  then
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7:    $flag[1] \leftarrow 1$ 
8: critical section
9:  $turn \leftarrow 0$ 
10:  $flag[1] \leftarrow 0$ 
```

An interesting violation

- Dekker with safe-T: **M**
- RW-safe variant: **S**

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²*Oracle Labs, Burlington, MA, USA*

³*Department of Computing Science, University of Groningen, 9700 AK Groningen, The Netherlands*

SUMMARY

Dekker's algorithm was thought to be safe in an environment *without* atomic reads or writes where bits flicker or scramble during simultaneous operations. A counter-example is presented showing Dekker's algorithm is unsafe without atomic read. A modification to the original algorithm is presented making it RW-safe, allowing threaded systems to be built on low cost/power hardware without atomic read/write. Correctness is verified by means of invariants and UNITY logic. A performance comparison is made for several two-thread software mutual-exclusion algorithms to see if the RW-safe Dekker is competitive. A subset of the two-thread solutions are then compared in two N -thread tournament algorithms. The performance results show that the additional checks in the RW-safe Dekker do not disadvantage the algorithm in comparison with other two-thread algorithms. The RW-safe N -thread tournament algorithms are competitive with the hardware-assisted Mellor-Crummey and Scott algorithm. Copyright © 2015 John Wiley & Sons, Ltd.



Just Verification of Mutual Exclusion Algorithms

Rob van Glabbeek, Bas Luttik, and Myrthe Spronck

28 August 2025